Development of interconnected silicon micro-evaporators for the on-detector electronics cooling of the future ITS detector in the ALICE experiment at LHC

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Abstract The design of the future High Energy Physics (HEP) particle detectors for the upgrade of the LHC (Large Hadron Collider) experiments at CERN (European Organization for Nuclear Research) is pushing technological frontiers to the limit trying to reach unprecedented accuracy in particles identification and particle production dynamics in ultra-relativistic hadron collisions.
The thermal management of the on-detector electronics and the development of low mass integrated cooling systems have become a crucial task in the design of silicon tracking detectors for HEP applications.
In this paper, we present a novel concept of low mass interconnected silicon microchannel devices for the future Inner Tracking System of the ALICE (A Large Ion Collider Experiment) detector at LHC. This innovative design achieves the requirements of the detector while minimizing the total material budget.

Keywords: Micro-channels, Flow boiling, Micro-fabrication, Electronics cooling, Particle detectors

1. Introduction

Flow boiling in microchannels has received considerable attention in the past decade for the thermal management of electronic components (e.g. computer CPU's) [1]. Agostini [2] presented a comprehensive state-of-the-art review of high heat flux cooling technologies and showed that two-phase flow boiling in microchannels is a very promising solution for maintaining the Moore's law trend for Integrated Circuits (IC) in the next years. Taking advantage of the latent heat absorbed during the boiling process allows operating at low mass flow rates with minimum temperature gradients. On the other hand, silicon microfabrication technologies can provide very precise devices, with low mass and reduced dimensions.
Most of the studies so far addressed the cooling of a single electronic component, but in recent years many efforts were involved in the development of 3D-IC chips with several high power-density logic layers interconnected with Trough Silicon Vias and embedded microchannels for the removal of 100-150 W/cm^2 per layer in 15x15 mm^2 chips [3].
When cooling the on-detector electronics in High Energy Physics (HEP) experiments, different constraints complicate the design of the system. The minimization of the total mass introduced and strict dimensional constraints for the integration of the detector in the experiments, together with challenging thermal requirements are the main guidelines in the design of the on-detector cooling system [4].
Vertex detectors for HEP experiments are usually composed by silicon detection chips assembled in a row called "stave" (Fig. 1). Staves are installed in a barrel geometry surrounding the interaction point of the two colliding beams, composing a detection layer.
In this paper we present a novel prototype of interconnected low mass silicon microchannel devices for the next generation silicon vertex detectors at the CERN (European Organization for Nuclear Research) Large Hadron Collider (LHC). After introducing the case study and presenting the concept of the proposed

solution, we focus on the microfabrication and the assembly of the final prototype concluding with the main results from the thermal characterization of the system.

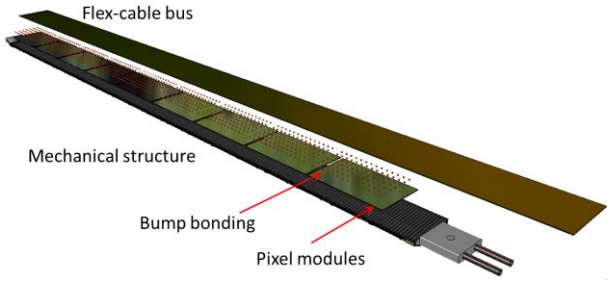

Figure 1 The Inner layer stave assembly of the future ALICE Inner Tracking System.

2. The ALICE Inner Tracking System upgrade

The Inner Tracking System (ITS) is the ALICE's innermost detector surrounding the beam pipe. It plays a key role in the reconstruction of the primary and secondary vertices, low momentum particle identification and tracking [5].

In order to improve the physics capabilities, the ALICE collaboration will replace the existing tracker with seven new layers of pixel detectors. Monolithic Active Pixel Sensors (MAPS) implemented using the 0.18 μm CMOS technology of TowerJazz have been selected as the technology for all layers. The MAPS chip consists of a single silicon die of 15x30 mm^2, which incorporates a high-resistivity silicon epitaxial layer (sensor active volume), a matrix of charge collection diodes (pixels) with a pitch of the order of 30 μm, and the on-detector electronics [6].

The staves of the three innermost layers composing the ITS Inner Barrel (Fig. 2) will be composed by 9 chips in a row for an active are of 15x270 mm^2 per stave.

The on-detector electronics is expected to exhibits a power dissipation of 0.1-0.3 W/cm^2 over the chip surface. For the Inner Barrel, this turns to a total dissipation ranging from 200 to 600 W. This power must be efficiently removed in order to ensure proper working conditions of the detector. The maximum working temperature for the chip is set to 30°C while the minimum temperature allowed is 15°C in order to avoid condensation on the electronics surface. During operation, the maximum temperature difference allowed over the chip surface is 5°C. In order to fulfil these requirements, a dedicated on-detector cooling system based on flow boiling inside silicon microchannels has been proposed and developed. The high heat transfer rate achieved with flow boiling at the micro-scale promotes the removal of the heat dissipated by the electronics and guarantees the temperature uniformity required for the detector operation.

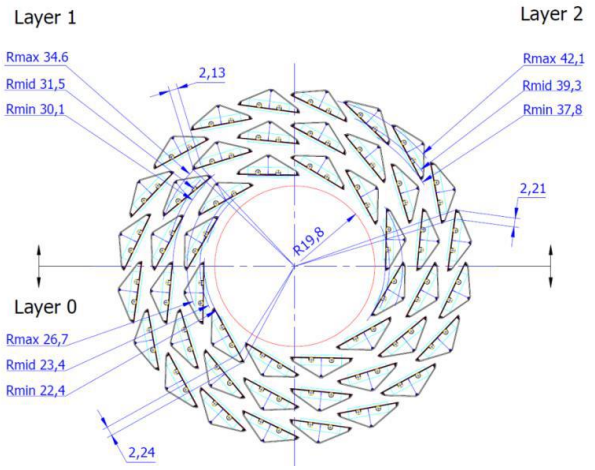

Figure 2 Cross sectional view of the three layers composing the ITS inner barrel surrounding the beam pipe (in red). Dimensions are reported in mm.

For the future ITS, a big effort was devoted to the minimization of the total material budget of the detector. The material budget is a parameter considering the materials composing the detector and in particular their interaction with incident particles. In order to ensure an optimal particle detection and tracks reconstruction, the total material budget of the detector must be minimized.

3. Interconnecting silicon micro-channel devices

In order to minimize the material budget of the on-detector cooling system, a special frame

design was investigated: this design presents silicon microchannels only at the edges of the chip, avoiding any additional material in its inner region.

Figure 3 First prototype of low material budget silicon frame with embedded microchannels.

A first prototype of a silicon frame with embedded microchannels has been fabricated (Fig. 3) and tested under nominal chip power dissipation showing good performance [7]. This device is limited in dimensions by the silicon wafer used for the microfabrication. At this stage of the development 4" wafers are used to validate the concept and fabrication of prototypes on 6" wafers has already started. However, even using 8" wafers still it would not be possible to reach the length of the ITS inner layers stave (270 mm) while using larger wafers would lead to a device very hard to handle during the assembly and integration phase. The interconnection of several silicon microchannel devices is therefore necessary.
For this purpose, a novel design of low material budget interconnected silicon micro-evaporators was developed (Fig. 4). In this design, a supply line providing refrigerant to different devices and a return line collecting the vapor from the outlet manifolds to the outlet port are embedded in the silicon frame alongside the microchannels where the fluid, evaporating, removes the power dissipated by the on-detector electronics. Inlet and outlet ports are located on the same side of the stave as for design requirement in order to guarantee a fast extraction of the barrel from the experiment for maintenance.

The fluid, after entering the prototype from the inlet port through a pipe glued on the Pyrex cover, in part fills the inlet manifold of the first prototype and in part flows along the inlet distribution line running alongside the first silicon frame. The fluid then reaches the inlet manifold of the second prototype providing refrigerant to it. From the inlet manifolds, the fluid is distributed to the 12 microchannels located on each side of the frame with a cross section of 100x100 μm^2.
Restrictions designed at the inlet of each channel force the evaporation of the fluid and prevent backflows and flow misdistribution.

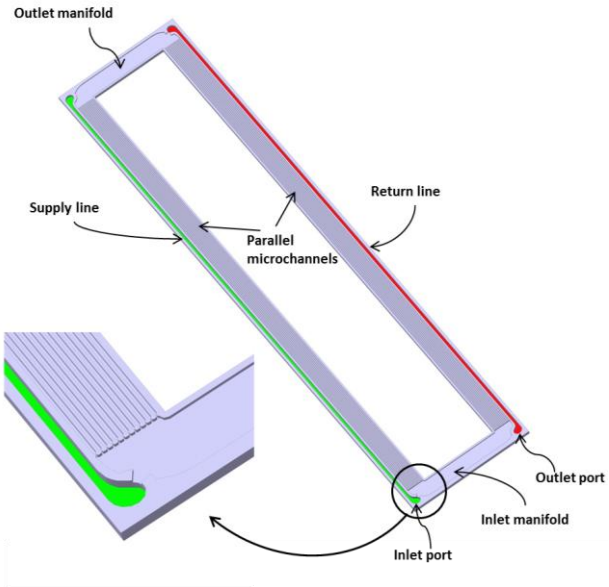

Figure 4 CAD model of the frame prototype (left) where inlet (green) and return (red) distribution lines are showed.

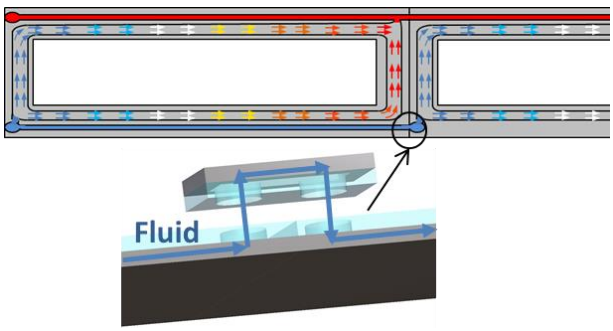

Figure 5 Fluidic path of the interconnected frames (top) and the micro-bridge concept for the fluidic interconnection (bottom).

From the outlet manifolds, the vapor exiting from the microchannels is brought to the outlet port along the return line. Before the end of each device, the distribution line stops and the fluid is forced to exit orthogonally the silicon plane through a hole realized in the Pyrex plate; the fluid then enters a microfabricated bridge installed with precise alignment on top of the device (Fig. 5). At the interface between the two frames, the fluid runs along the bridge and then enters the distribution line of the following frame prosecuting its path.

4. Fabrication of interconnected silicon micro-evaporators

The silicon microchannel devices realized for this study have been fabricated in the CMi (Centre of MicroNano Technology) class 100 MEMS clean room at EPFL (Ecole Polytechnique Fédérale de Lausanne) using microfabrication techniques.

The process starts with a p doped 380 µm thick silicon wafer where a 2 µm SiO_2 layer is grown on the silicon surface and 200 nm of Low Stress Si_3N_4 layer is then deposited by LPCVD (Low Pressure Chemical Vapour Deposition) (Fig. 6a). These layers will be later used as a hard mask during plasma etching allowing the realization of channels at two different depths.

With photolithography and plasma etching on the wafer backside, the pattern of the central pools is transferred to the oxide layer, together with dicing and alignment marks (Fig. 6b).

The same process is used on the front side to pattern the complete fluidic circuitry (distribution lines, microchannels and manifolds) (Fig. 6c). A third photolithography is then used to mask the microchannels and manifolds leaving only the distribution lines exposed to the plasma (Fig. 7 left) since they have to be etched deeper than the microchannels (Fig. 6d). After a first step of plasma etching of the distribution lines (Fig. 6e), the Photolithographic Resist (PR) is stripped and the SiO_2 layer patterned with the second photolithography is used as hard mask for the final etching of the micro-channels and the distribution lines (f).

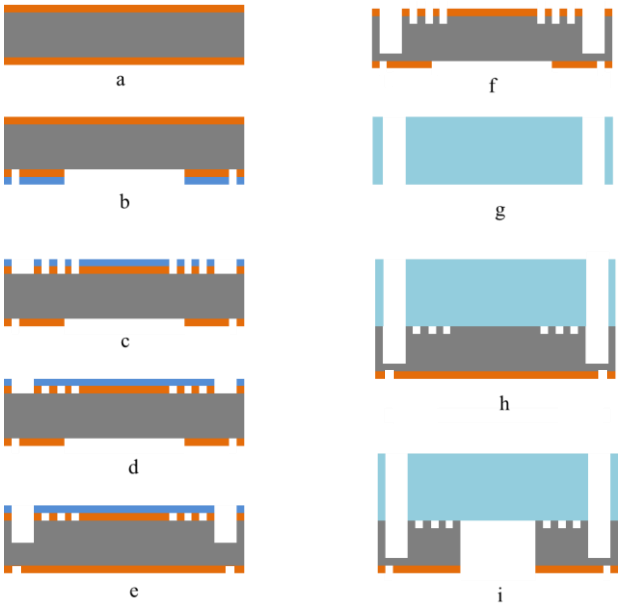

Fig. 6 Simplified Process Flow of the microfabrication
a) SiO_2/SiN thin film deposition; b) Patterning of the back side hard mask (SiO_2/SiN); c) Patterning of the front side hard mask (SiO_2/SiN); d) Photolithography of the distribution lines; e) Partial etching of the distribution lines; f) Complete etching of microchannels, manifolds and distribution lines; g) Etching of fluidic inlets on the Pyrex wafer by sand blasting; h) Anodic bonding; i) Etching of the pools in the silicon.

At this point the SiO_2 layer on the wafer front side is stripped and the surface is prepared for the anodic bonding with a Pyrex plate (g) that ensures the sealing of individual channels.

The Pyrex plate is used only at this stage of the development for the visualization of the two-phase fluid dynamics inside the channels. For the final device, a direct silicon-silicon bonding will be performed.

Inlet and outlet holes of the microfluidic circuit are obtained on the Pyrex plate by sand blasting. Before the bonding, the Pyrex and the silicon wafers must be aligned in order to precisely position the inlets/outlets holes with respect to the microchannels (Fig. 7 right).

After the bonding, the silicon in the inner region is removed (Fig. 8) with a last step of plasma etching using the SiO_2 layer patterned with the first photolithography as mask (h).

At this point, the four devices and the micro bridges in a wafer are diced and the process continues with the assembly of the prototype.

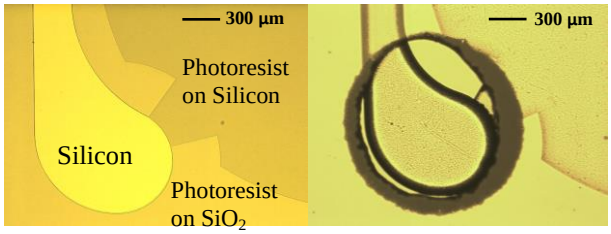

Figure 7 Third photolithography on the previously patterned silicon oxide (left) and alignment of the inlet hole in the cover wafer in respect of the distribution line (right).

The frames are first glued head-to-head with epoxy glue. Then, with a precise positioning tool, the micro-bridge is aligned at the interface between the two frames with respect to the inlet/outlet holes of the devices (Fig. 9). The interface is then sealed using epoxy glue.

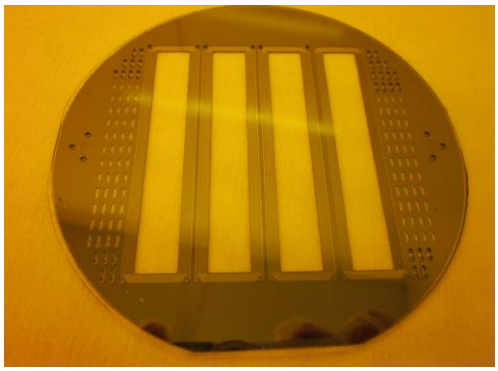

Figure 8 The silicon wafer after the removal of the central pools by silicon plasma etching for material minimization.

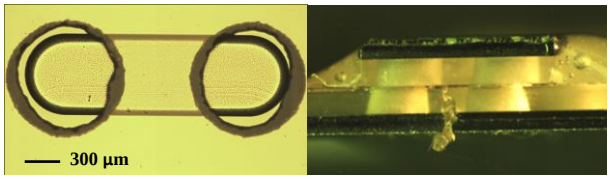

Figure 9 The machined Pyrex wafer aligned with respect of the channel forming the bridge (left) and installation of the micro-bridge at the interface between two frames (right).

For simulating the power dissipation of the ITS pixel chips, silicon dummy chips have been fabricated. They consist of a 15x30 mm^2 silicon die 100 µm thick, where a 200 nm Platinum film is deposited by sputtering with a 20 nm Titanium intermediate layer for adhesion enhancement. Since this prototype simulates only half ITS stave, 4 and a half dummy chips with the actual MAPS chip dimensions are installed (Fig. 10).
Tin lines guarantee electrical interconnection of the Platinum film on different chips and two thin electrodes soldered at the two extremities are used for the power input.

Figure 10 The final prototype equipped with silicon dummy chips. The tin soldering lines for the electrical interconnection of the Platinum film and the two electrodes at the extremities are also visible.

5. Characterization of the prototype

5.1 Single-phase tests

Single-phase tests were performed on the prototype using Perfluorobutane (C_4F_{10}) as the refrigerant fluid. Single-phase pressure drops of the full prototype in the range of mass flow rate of interest for the application are shown in Fig. 11. The Experimental data are compared with analytical calculations assuming an equal distribution of the fluid within the two frames. Contraction and expansion loss coefficients K_c and K_e are derived from Kays and London [8] while for the 90 degree bends it was assumed K_{90}=1.2 as suggested by Phillips [9].

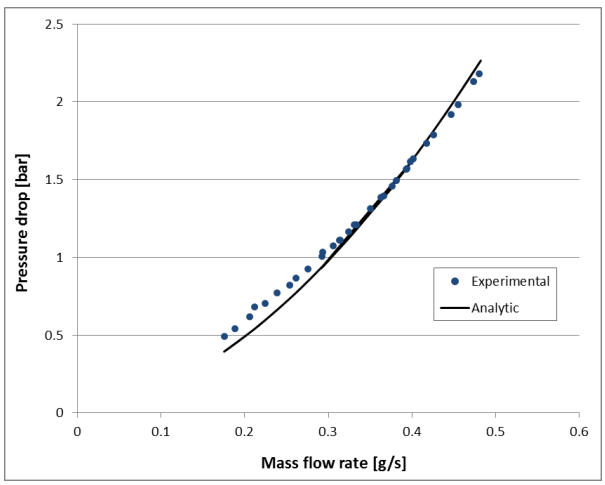

Figure 11 Single-phase pressure drop characteristics of the prototype.

The IR map of the chip surface during single-phase flow is shown in Fig. 12 for a uniform

power dissipation q_{chip}=0.1 W/cm^2 over the chip surface and a mass flow rate of $\dot{m}$=0.4 g/s. The fluid enters the test section from the bottom left corner in subcooled condition: therefore at the left side of the prototype the surface temperature is dominated by the inlet manifold where the fluid is distributed to the microchannels. The fluid running inside the microchannels warms up because of the high HTC while the remaining fluid flows inside the supply line to reach the inlet manifold of the second frame: at the interface between the two frames, the surface temperature drops because of the cold liquid filling the inlet manifold of the second prototype.

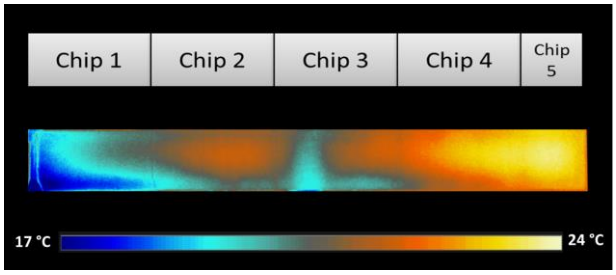

Figure 12 Infrared temperature map of the chips' surface for a power dissipation of q_{chip}=0.1 W/cm^2 and a mass flow rate $\dot{m}$=0.4 g/s of C_4F_{10} single-phase liquid flow.

The longitudinal temperature profiles along three different lines (supply line, centre of the prototype and return line) are shown in Fig.13 where the temperature drop at the inlet manifold of the second frame is visible.

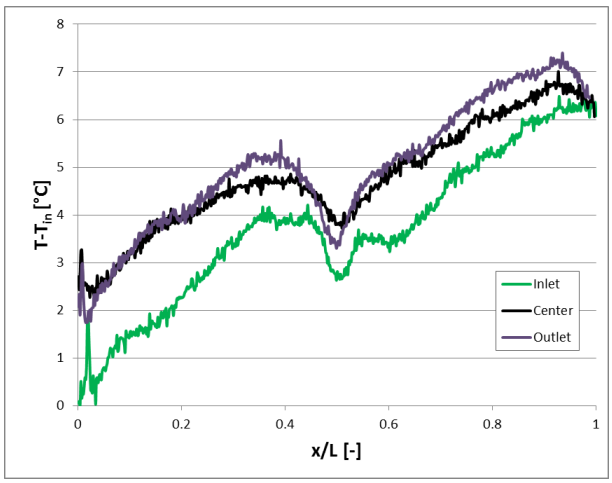

Figure 13 Longitudinal temperature profiles on the chips surface along three different lines.

Transversal temperature profiles in Chip 2 for different heat fluxes are presented in Fig. 14a. The experimental results obtain from the IR image of the chip surface temperature (dotted lines) are compared with numerical results (solid line). Steady state conduction simulations were performed on a cross section of the prototype (Fig. 14b). Heat flux was imposed at the chip surface and analytical heat transfer coefficients for fully developed single-phase laminar flow and three side heating condition were imposed at the walls of the channels.

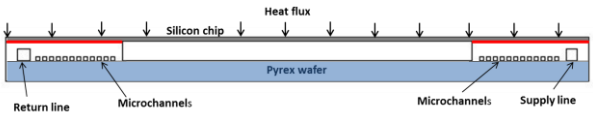

Figure 14 (a) Cross section of the prototype used for the numerical calculations of the chip surface temperature.

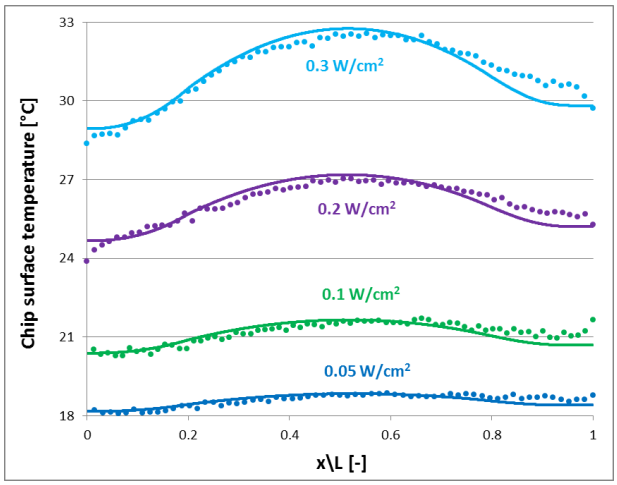

Figure 14 (b) Transversal temperature profile obtained from the IR measurements at different power dissipations (dotted lines) compares with numerical results (bold lines).

5.2 Two-phase tests

During flow boiling tests, at the low heat flux expected for the ITS pixel chips with the fluidic design realized for this prototype it was not possible to obtained the Onset of Nucleate Boiling at the beginning of the microchannels as required for a proper operation of the device. Axial conduction into the inlet header was sufficient to initiate boiling, creating a

two-phase entrance of the fluid rather than the desired liquid only flow at the inlet. For this reason, the tests were carried out with two-phase conditions at the entrance of the prototype.
This caused oscillations of the mass flow rate measured by a Coriolis Mass Flow Meter ranging from 0.03 to 0.07 g/s for a nominal mass flow rate of 0.05 g/s. The effect of these oscillations on the surface temperature of the chips is addressed below.
The temperature map for C_4F_{10} flow boiling ($\dot{m}$=0.05 g/s) in the test section for a uniform power dissipation q_{chip}=0.1 W/cm^2 on the chip surface is reported in Fig. 15. The longitudinal temperature profiles along three different lines (supply line, centre of the prototype and return line) are shown in Fig.16. The total temperature difference in the prototype is ΔT_{tp}=3 °C, while a ΔT_{sp}=7 °C was recorded in single-phase flow for the same heat flux on the chip surface but with a higher flow rate ($\dot{m}$=0.4 g/s). The temperature decrease associated with the pressure drop is visible along the return line and it is emphasized in the return line of the left prototype, where the total mass flow rate is flowing in the return line increasing the pressure drop.
Temperature oscillations caused by the intermittent flow inside the device are reported in Fig. 17. The amplitude of the oscillation is within 0.5 °C and therefore acceptable for the application.

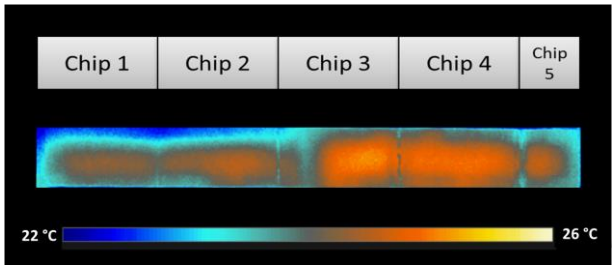

Figure 15 Infrared image of the surface of the chips during flow boiling C_4F_{10} ($\dot{m}$=0.05 g/s) at a uniform power dissipation q_{chip}=0.1 W/cm^2 on the chip surface.

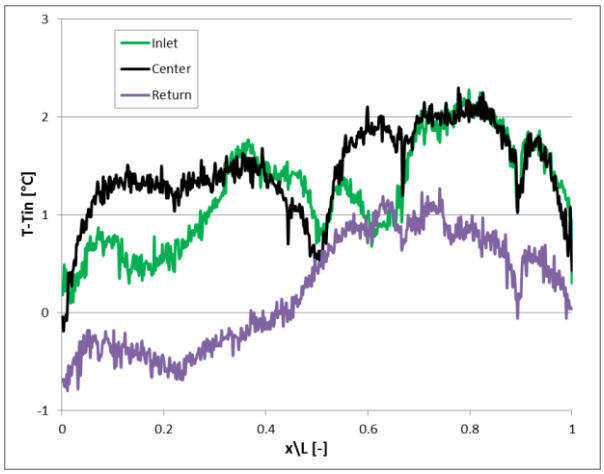

Figure 16 Longitudinal temperature gradients with respect of the inlet temperature (Tin=23.2 °C) for flow boiling ($\dot{m}$=0.05 g/s) with q_{chip}=0.1 W/cm^2 uniform heat flux on the chip surface.

For certain operating conditions unequal distribution of the refrigerant within the two frames was observed. This caused only a small fraction of the total mass flow to reach the second frame. In this case, a dryout condition is observed starting from the middle of the second frame (Fig. 18) while stable two-phase flow is established on the rest of the prototype.

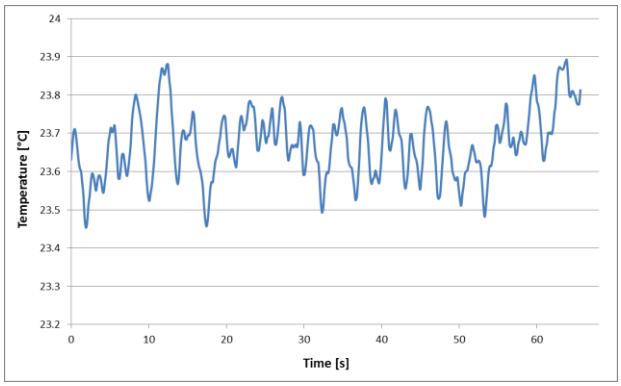

Figure 17 Temperature oscillations on the surface of the chip.

The causes of this misbehaviour and their relations with the operating conditions will be addressed in a new dedicated test campaign.

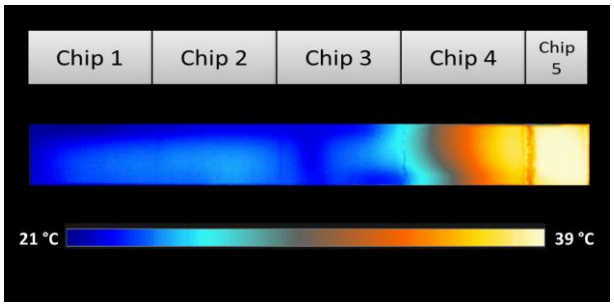

Figure 18 Infrared image of the surface of the chips with dryout conditions in the middle of the second frame.

6. Conclusions

A novel concept of interconnected silicon microchannel evaporators for the cooling of the on-detector electronics in vertex detectors for High Energy Physics experiments was presented. This study has been carried out for the upgrade of the ALICE Inner Tracking System at the CERN LHC. Very strict requirements for the minimization of the total material budget of the device, together with large active areas to be cooled and challenging integration constraints pushed the development of innovative solutions for the interconnection of silicon micro-evaporators and their operation. The fabrication and the assembly of the prototype were described in detail. Single-phase and flow boiling tests with C_4F_{10} refrigerant confirm the successful interconnection of two silicon frames and show good thermal performance in the operational range expected for the future ITS detector. A new design of the fluidic circuitry is under study aiming to overcome some misbehaviours observed with the current design. Long capillaries at the entrance of each microchannel would force phase-change, providing evaporative flow at the beginning of each channel and guaranteeing single phase-liquid flow in the supply line for a better distribution of the refrigerant within interconnected devices.

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