High Efficiency Smart Voltage Regulating Module for Green Mobile Computing

A thesis submitted in partial fulfilment of the requirements for the degree of Doctor of Philosophy (PhD) to:
Electronic and Computer Engineering
School of Engineering and Design
Brunel University
United Kingdom

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B.Sc. (Hons), M.Sc. (Hons)

Supervised by:
Prof. Hamed S. Al-Raweshidy

March
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Declaration

This is to certify that:

i. The thesis comprises only my original work towards the PhD except where indicated.

ii. Due acknowledgement has been made in the text to all other material used.

Monaf Sabri Tapou

ABSTRACT

In this thesis a design for a smart high efficiency voltage regulating module capable of supplying the core of modern microprocessors incorporating dynamic voltage and frequency scaling (DVS) capability is accomplished using a RISC based microcontroller to facilitate all the functions required to control, protect, and supply the core with the required variable operating voltage as set by the DVS management system.

Normally voltage regulating modules provide maximum power efficiency at designed peak load, and the efficiency falls off as the load moves towards lesser values.

A mathematical model has been derived for the main converter and small signal analysis has been performed in order to determine system operation stability and select a control scheme that would improve converter operation response to transients and not requiring intense computational power to realize. A Simulation model was built using Matlab/Simulink and after experimenting with tuned PID controller and fuzzy logic controllers, a simple fuzzy logic control scheme was selected to control the pulse width modulated converter and several methods were devised to reduce the requirements for computational power making the whole system operation realizable using a low power RISC based microcontroller. The same microcontroller provides circuit adaptations operation in addition to providing protection to load in terms of over voltage and over current protection.

A novel circuit technique and operation control scheme enables the designed module to selectively change some of the circuit elements in the main pulse width modulated buck converter so as to improve efficiency over a wider range of loads. In case of very light loads as the case when the device goes into standby, sleep or hibernation mode, a secondary converter starts operating and the main converter stops. The secondary converter adapts a different operation scheme using switched capacitor technique which provides high efficiency at low load currents. A fuzzy logic control scheme was chosen for the main converter for its lighter computational power requirement promoting implementation using ultra low power embedded controllers. Passive and active components were carefully selected to augment operational efficiency. These aspects enabled the designed voltage regulating module to operate with efficiency improvement in off peak load region in the range of 3% to 5%. At low loads as the case when the computer system goes to standby or sleep mode, the efficiency improvent is better than 13% which will have noticeable contribution in extending battery run time thus contributing to lowering the carbon footprint of human consumption.

Dedication

TO my dear beloved father Sabri Tapou who deserves all my love, gratitude, and admiration for he is behind all the success I've accomplished in my life.

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Monaf Sabri Tapou

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LIST OF SYMBOLS

Symbol	Definition
α	Activity factor related to logical transitions during device operation
ε_o	Free space permittivity
ε_r	Relative permittivity
ζ	Damping factor
μ_o	Free space permeability
μ_r	Relative permeability
τ	Time constant
ω_n	Natural frequency
C	Capacitance in Farad
C_{Ah}	Battery Cell Capacity in Ampere
C_e	Capacitance in Farad
C_{eff}	Total capacitance of the nodes weighted
D	Duty cycle of PWM signal
E	Energy in Jules
E_g	Energy required to transfer Q_g
f_{clk}	Clock frequency
f_s	Switching frequency
$I_{g\text{-}ox}$	Get oxide leakage current
I_{leak}	Leakage current
$I_{l\text{-}weak}$	Weak inversion induction current
L	Inductance in Henries
P	Power in watt
$P_{Dynamic}$	Dynamic power consumed by processor
P_G	Gating power dissipation
P_{leak}	Leakage Power
Q	Charge Coulomb
Q_G	Total gating charge required to turn the MOSFET device on in Coulomb
Q_g	Gate charge
$R_{DS(ON)}$	MOSFET drain source channel on-resistance
T	Temperature
V_{dd}	MOSFET circuit supply voltage
V_{th}	Threshold voltage
W	MOSFET device gate width

LIST OF ABBREVIATIONS

Abbreviation	Definition
ADC	Analog to Digital Convertor
AI	Artificial Intelligence
CCM	Continuous Conduction Mode
CCV	Closed Circuit Voltage
CMOS	Complementary Metal Oxide Semiconductors
CPU	Central Processing Unite
DCM	Discontinuous Conduction Mode
DCR	Direct Current Nominal Resistance
DOD	Depth of Discharge
DSP	Digital Signal Processing
DVS	Dynamic Voltage and Frequency Scaling
EMC	Electro Magnetic Compliance
EOD	End of Discharge
ESR	Effective Series Resistance
FLC	Fuzzy Logic Controller
FOM	Figure of Merit
FPGA	Field Programmable Gate Array
HW	Hardware
IGBT	Insolated Gate by Polar Transistor
I^2C *or* IIC	Inter Integrated Circuit
ITRS	International Technology Roadmaps for Semiconductors
LDO	Low Drop Out Regulator
LNR	Line Regulation
LOR	Load Regulation
MLCC	Multi Layer Ceramic Capacitor
MTBF	Mean Time Between Failure
NMOS	N-channel Metal Oxide Semiconductors
OCV	Open Cell Voltage
PD	Proportional Derivative
PDA	Personal Digital Assistant
PFM	Pulse Frequency Modulation
PI	Proportional Integral
PID	Proportional Integral Derivative
PLL	Phase Locked Loop
PMI	Power Management Integrated Circuit
PMOS	P-channel Metal Oxide Semiconductors
PWM	Pulse Width Modulation
rms	Root mean square
SCL	Serial Clock
SDA	Serial Data

Abbreviation	Definition
S0C	System on Chip
SW	Software
VRM	Voltage Regulating Module

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Chapter One

Introduction to Improving Mobile Computing & Communication Systems Energy Efficiency

1.1. Introduction

Mobile Computing and communication systems have gained a massive popularity among general consumer items, these include: Smartphones, Portable gaming consoles, Tablets, E-readers, Laptops and netbooks. The number of these as was indicated by a study conducted on techcrunch website on February-13-2012 stating that there are mobile devices in use as much as there are people on Earth [1]. The reduction of power consumption for these devices will have a noteworthy contribution on reducing the carbon footprint of human consumption which will in turn reduce the green house effect from which the global environment is suffering.

Designing Energy efficient mobile computing systems involves introducing improvements in several key systems elements. These key system elements include the architecture of the processing elements, the wireless communication elements, and the power control and management elements. In mobile computing and communication systems, the most power consuming element is the central processing unit which stands for about 58% of the total power consumed [2]. While this figure varies according to the application under processing, still it indicates that reducing the amount of energy expended inside the central processing unit has the largest impact on the overall energy consumption of a mobile computing and communication device.

Applications that run on a certain computing system require different performance index requirements from the processing unit or units [3], this means that the processor for a

certain computing system is not required to operate at maximum performance all the time, so if it were possible for the computer processor to have a variable clock speed, which in turn will change the performance index, it would be possible to operate the processor at a clock rate that will produce the performance required to run the given application rather than running it at a clock frequency that yields peak performance as the power expended inside the processor is directly related to its clock rate [4] as will be further clarified in chapter two in details.

A consequential outcome of operating the processor at lower clock frequencies is the possibility for the processor core to be operated at a lower voltage without compromising its functionality because it would be possible to operate the switching transistors at a lower voltage which would lead to larger junction capacitances resulting in longer delays, this will result in lowering the maximum clock operating frequency and as the power is proportional to the square of the operating voltage, there would be a significant gain in energy conservation when the running application does not require the full performance of the processor.

Processors that can be operated at various clock frequencies should also posses the capability of operating its core and or other sections at lower voltage levels without compromising its functionality. Modern processor manufacturing firms have encompassed this feature in several of their products; for instance, Intel Corporation have several of their processors incorporated with *speed step* technology, these were processor families that have the capability to work at different clock frequencies and core voltages to permit for better power efficiency and cooler operation.

1.2. Motivations

Since the dawn of mobile computing and communication systems and equipment, there were numerous investigations on coming up with a computing system that would have high computational performance and at the same time would be energy efficient. Several research pathways can be pursued to reach that goal, these include advances in processor architecture by adapting improved circuit techniques, interconnect optimizations, improved materials and production processes. In addition to that modern software designers are more inclined toward energy efficient programming by using energy aware

compilers and programming techniques and designing operating systems that are energy aware. Modern processors are designed to operate to provide a variable computing power index that can be utilized to set processor's operating parameters to provide the computational power required by the currently running application. This means operating the processor's core at different clock frequencies and core operating voltages and this yields huge energy savings that some researchers predict a 15% to 60% energy saving in CPU [5]. This technique is termed as "Dynamic Voltage and frequency scaling" or DVS [4,5,6,7].

DVS technique is implemented in the operation of modern microprocessor units. It requires a specially designed power source capable of supplying the required operating voltages which are behind the real gain in energy saving.

For the power supply to be suitable for DVS system ready requirements it needs to have special features [7], the most important is to be capable of supplying the required processor core voltage to suit the current operating clock frequency as recommended by the processor manufacturer. Again when observing the use of mobile computing devices especially the smart phones as indicated by a recent study that the average American adult uses the smart phone for about 58 minutes daily [8] and the number of smart phones has hit one billion units as of late 2012 and this number is expected to reach two billions by the year 2015 [9]. These figures indicate that maintaining high efficiency for the VRM while supplying low voltage and current levels will have a notable contribution in prolonging battery usage thus extending the time between recharging which will result in lower carbon footprint from the operation of the given devices.

According to what has been mentioned, the fundamental essence of the motivation for this work is to design a smart high efficiency voltage regulating module that can maintain high efficiency while supplying a DVS ready processor core with the required operating voltage that suits all its operation conditions.

1.3. Aim and Objectives of the Research

The aim of this research is to design a high efficiency smart voltage regulating module for the core of PXA270 a dynamic voltage scaling compatible microprocessor. For this aim to be realized the following objectives were pursued:

- To develop a design criterion that focuses on high efficiency with respect to circuit topology, component selection and control Scheme.

- To develop a simulation module for the primary converter that will be used to aid the process of selecting the controller type that will suit its implementation on a low power microcontroller, then this control scheme will be tuned, tested and its performance compared against other popular controller designs.

- To implement the selected control system using a micro power RISC based microcontroller that would be used to: generate the Pulse width modulation signal, apply the selected control scheme, regulate output voltage against load variations and battery voltage fluctuations, furnish the required load adaptive operation including selecting the primary or the secondary converter according to load current requirements. It also will provide additional functions that adds safety features to the operation of the converter like over-current, short-circuit, and over-voltage protection.

- To implement final circuit design refinements into a prototype module, test its operation and compare its performance against some state of the art devices and systems.

1.4. Contributions to Knowledge

The primary core of the contribution of this work is the development of a circuit design for a smart voltage regulating module that would provide high energy conversion efficiency throughout the voltage and current output range required by a DVS ready processor core especially at the lower power requirements of the stand by mode, the sleep mode and the hibernation mode.

1.5. Achievements

The designed smart voltage regulating module has achieved high efficiency figures that matched those obtained from several industry standard regulators like Texas Instruments TMS62040 and Intersil ISL85418. It has achieved improvements in mid load condition by 3% to 5% figure, and made a better than 13% improvement in the small load

conditions since the main converter stops, the microcontroller goes into low power mode, and the secondary low power converter starts supplying load resulting in lower losses at this load region thus improving efficiency. At the same time, by reducing the operating frequency of the converter, no serious harmonics were generated from the converter that could affect the operation of the wireless communication system incorporated inside the mobile device that will accommodate the designed VRM to power the core of its central processing unit.

1.6. Thesis Organisation

The remainder of this thesis is organised in following manner:

Chapter two includes a brief discussion on power consumption analysis and techniques that can be pursued to realize power efficient computing systems. In addition to that reviews on previous studies related to the fields covered by the conducted research are also included.

Chapter three describes the features of the dynamic voltage and frequency scaling system (DVS), the target processor specifications and power requirements throughout its DVS compatible operating modes. In addition to that, a study on the power source used to provide the operational energy requirements for most of the mobile devices namely the Lithium – Ion and Lithium polymer storage cell the operational characteristics of which has a crucial impact on the design of the control system for the designed VRM.

Chapter four covers the operation principles for the buck pulse width modulated converter (the primary converter) and its design concepts. In addition to that it will cover the operation principle for the switched capacitor or charge pump buck converter. It will also cover how to select the proper passive and active components that will ensure higher power efficiency operation of the designed converter.

Chapter five covers the mathematical analysis and the small signal system analysis to view the behavior of the system under design. It also includes discussion on a simulation module designed using Matlab/Simulink that was used to evaluate and study closed loop control of the main voltage converter in the designed VRM system.

A standard optimized PID controller was chosen to furnish the voltage regulating function. Observations were made on the control signal reaction to various source/load conditions, and the experience gained was used to design a simple fuzzy logic controller that would provide the essential performance needed to meet target load requirements. This controller will be incorporated in the designed VRM to furnish the voltage regulation function.

Chapter six covers the experimental work done on the implemented VRM design and test its various operational ranges and its performance against an industry standard VRM, in addition to manipulating the control parameter tables to provide for better operational performance.

Finally, chapter seven contains the conclusions made on the entire work scope and some suggestions for future work.

Chapter Two

Overview of Pathways to Energy Efficient Mobile Computing Systems

2.1. Introduction

The need for energy efficient mobile computing system is growing rapidly as the number of various mobile computing devices for both general consumer market and the professional applications market. There is a great demand for microprocessors that have high computing performance while being more energy efficient than their predecessors. The goal here is to come up with lighter devices that will require smaller batteries or will run for longer periods before requiring recharging. Along these benefits on energy efficient mobile computing system element will make smaller size system realization possible for the fact that the energy efficient elements will require smaller heat sinking area to dissipate the generated heat. In addition to that, power efficient computing will contribute to reducing the carbon footprint of human consumption thus becoming green or environmental friendly.

To come up with an energy efficient computing system, several research pathways must be pursued in order to fulfill this task. In general these pathways fall in one of the following categories: (1) Power aware development in computer architecture which involves implementing circuit, buses and coding techniques that lead to computing systems that can have high performance with lesser components, lower bus crosstalk and fewer bus transitions which enables lower power consumption. (2) Researches in new semiconductor production materials and processes along with technology scaling have

great contribution in lowering power consumption and improving performance. (3) Devising efficient power control and management methods and circuits can have remarkable participation in lowering the total energy expenditure of the computing system. (4) Software developers must seek methods to come up with power aware compilers and software packages. All these pathways work collectively to come up with computing systems that are energy efficient which will lead to longer run time for mobile devices and greener computing products. Figure (2.1) shows the general pathways that can lead to energy efficient computing.

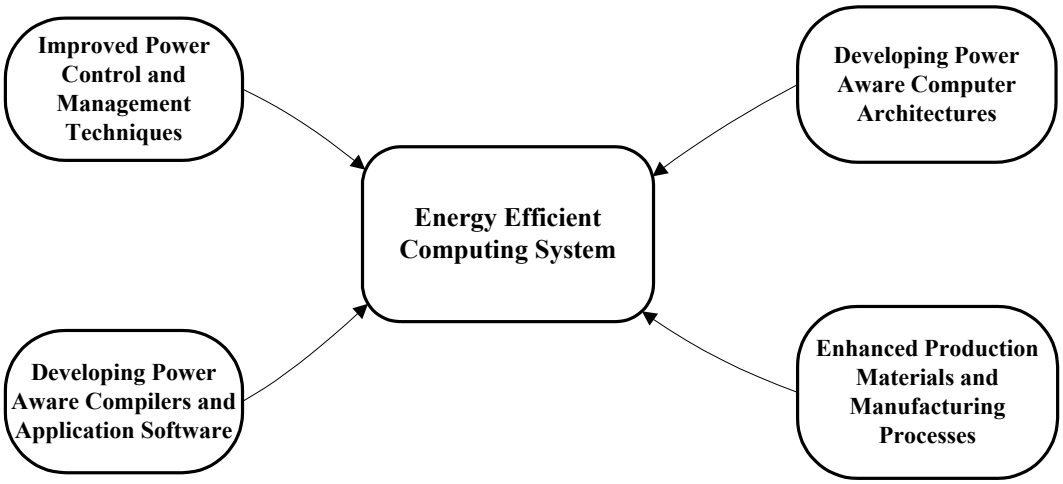


Figure (2.1) Pathways for realizing energy efficient computing system

How these pathways interact and produce the energy efficient computing system is better clarified as the energy expended by a computing system is investigated and how the improvements can be feasibly applied and realized in a given system. The following sections will deal with this issue.

2.2. Defining Power Expenditure in Digital Systems

It is necessary to investigate the issue of power consumed in the normal operation of any digital system in order to realize the impact of any technique on the subject of realizing an energy efficient digital system.

An important understanding about power expended during normal operation of modern digital systems including microprocessors is that this power consumption has these

dominant terms: namely the ***Static power consumption*** and the ***dynamic power consumption*** [10,11].

2.2.1. Static Power Consumption

Digital circuits including computer components consume static or what is termed as leakage or idle power. It can be defined as the power expended by a digital system at idle or no operation [10,11,12]. This power dissipation is related to several factors and is becoming a dominant factor in modern computing devices as their building blocks namely the transistors are becoming progressively smaller in size and their operating threshold voltage is getting increasingly lower. Figure (2.2) [11] shows that the leakage current dissipation is increasing as the technology is being scaled further.

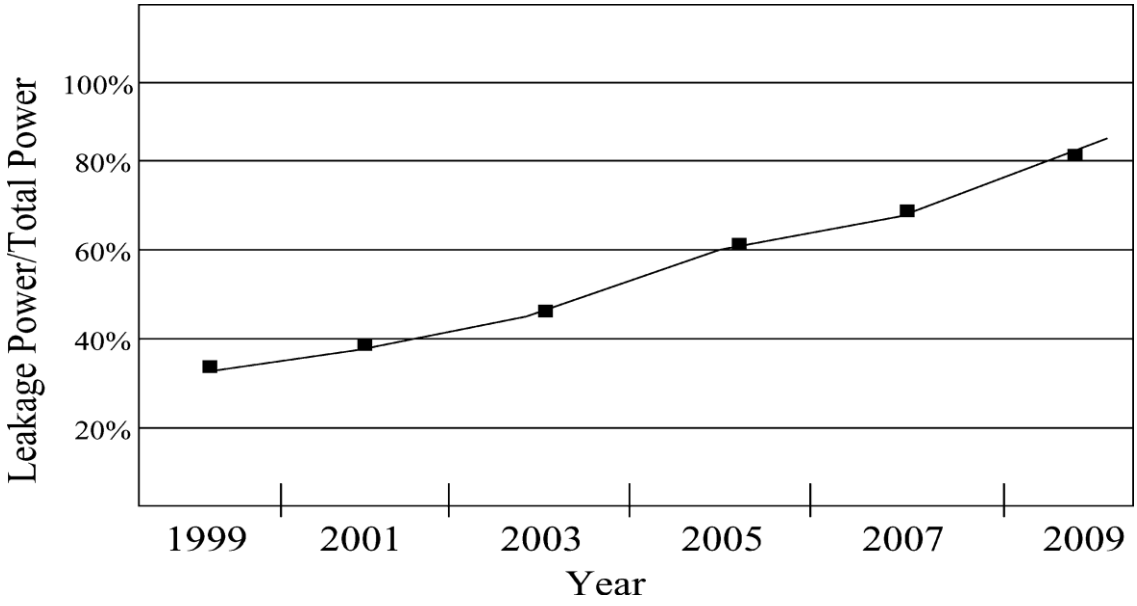


Figure (2.2) The International Technology Roadmap for semiconductors (ITRS) trends in leakage power consumption in digital and computing circuits as the manufacturing technology being scaled [11].

The leakage power (P_{leak}) can be defined as shown in the following equation:

$$P_{leak} = V \cdot I_{leak} \qquad \ldots\ldots(1)$$

Where (V) is device supply voltage, and (I_{leak}) is the leakage current of the semiconductor device.

This leakage current is the result of several components contributing to its overall value, the significant contributors are: the *reverse biased P-N junction leakage current*, the *gate induced drain leakage current*, the *sub-threshold or weak inversion conduction leakage current*, the *gate-oxide leakage current*, the *gate-leakage current*, and *the punch through leakage current* [12,13]. Of these six components the gate oxide leakage current and the sub-threshold leakage current dominate the overall value of the leakage current that contributes to the static power consumption.

The first dominant component of leakage current, the gate-oxide leakage current flows from the gate of a given transistor in the structure of a digital device into the silicon substrate. The equation below details the description of this component:

$$I_{g-ox} = K_2 W \left(\frac{V}{T_{ox}} \right)^2 \cdot e^{-\alpha \frac{T_{ox}}{V}} \qquad \text{.....(2)}$$

Where $I_{g\text{-}ox}$ is the gate-oxide leakage current, K_2,W and α are constants, V is the supply voltage, and T_{ox} is the thickness of the gate oxide material. It can be observed that the value of the gate-oxide leakage current relies upon the thickness of the oxide material layer that insulates the gate from the substrate. As modern computing devices are designed to have denser component population, this will require the thickness of the oxide layer to be minimized along with other scaled design parameters like transistor length and supply voltage. One solution to this problem will be to insulate the gates using high-K dielectric materials instead of conventional oxide materials that are commonly used. This term refers to materials having a high dielectric constant K. Modern high performance processors are manufactured using high-K insulating materials, for example Intel Corporation has introduced this concept with their 45nm manufacturing technology that was introduced with the core 2 processor series under the code name of "Penryn" in early 2007. Intel has announced the deployment of hafnium based high –k dielectrics in conjunction with a metallic gate and has shipped processors manufactured with this technology at early 2007[14].

The other major leakage current contributor is the weak inversion conduction leakage current. It flows between the drain and source of a given transistor. The value of this current depends on several components that can be related in the following equation:

$$I_{l-weak} = K_1 W \cdot e^{\frac{-V_{th}}{nT}} \left(1 - e^{\frac{-V}{T}}\right) \quad \text{..... (3)}$$

Where W is the gate width, K_1 and n are constants, V is the supply voltage and V_{th} is the threshold voltage of the transistor. It is clear that the influential parameters that affect this leakage current component are the supply voltage V, the transistor threshold voltage V_{th}, and the temperature T. As V_{th} decreases because of technology scaling along with supply voltage, the weak inversion conduction leakage current increases exponentially. This increase in leakage current will cause additional rise in substrate temperature which will lead to further increase in leakage current resulting in additional substrate temperature rise leading to a condition known as thermal runaway which leads to the destruction of the semiconductor device. This situation can be averted by taking several measures, the first is reducing supply voltage which is commonly applied to microprocessors and other digital components design. It must be noted that supply voltage reduction comes with a host of problems that must be addressed and solved in order to realize functional devices.

The other approach that can lead to reduce leakage current is by reducing circuit components statically, by designing circuits that will provide the required function with fewer components, or by dynamically reducing the effective transistor count by cutting power of idle sections in the digital device. This approach comes along with its host of implementation difficulties like how to predict when different sections of the circuit become idle and how to reduce the control overhead to address this issue.

The third method that can be implemented to reduce leakage current is reducing the operating temperature of the device using cooling techniques. And while this has been implemented since the 60s of last century, it can still provide a solution to reducing leakage current and provides additional benefits like allowing circuits to work faster, reducing chip degradation, and boosting chip life expectancy.

The fourth method is increasing transistor threshold voltage. It can be seen from equation (3) that increasing threshold voltage will reduce leakage current exponentially. This can

be achieved by using transistor stacking which effectively increases threshold voltage but at the cost of increasing component count which makes this approach inefficient. Another method is by using multiple threshold circuits with sleep transistors which is termed as "Power Gating"[15]. In this approach, the circuit elements for which the leakage current requires minimization are connected to the power supply through sleep switching transistors. When the circuit is active, its sleep transistor is turned on and when it become inactive the sleep transistor is turned off resulting in virtually very low leakage current. This method requires proper sizing of the sleep transistor to suit the drive requirement of the given part of the circuit. Moreover, it will require control overhead to address the matter of when to turn on and turn off the given sleep transistor and cannot be applied to memory devices that can lose contents when power is removed. Another method for threshold reduction is employing dual threshold circuits [16]. In this method leakage current is reduced by employing high threshold transistors on non critical paths and low threshold transistors on critical paths as non critical paths can execute instructions slower than those executed by critical paths without impacting overall performance. This technique is difficult to implement as making the choice of using the proper combination of high and low threshold transistors could lead to making the non-critical paths operate much slower to an extent that the overall performance could be compromised. Additional techniques can be pursued to reduce leakage current, one of those is by applying a method called adaptive body biasing [17]. This is a runtime technique that adjusts threshold voltages dynamically by applying body bias to the circuit sections that are inactive which will effectively increase the threshold at that section resulting in remarkable reduction in leakage current from that section but at the expense of increased delays in circuit operation. As the circuit becomes active the body biasing is reduced to lower threshold voltage to meet the required circuit performance.

All these techniques can participate in reducing static power consumption in modern computers and digital circuits.

2.2.2. Dynamic Power Consumption

This section will discuss the dynamic power consumption in modern computing and digital circuits.

The dynamic power consumption comes from the activity taking place in the computing or digital circuit. It comes from two sources, the switched capacitance and the short circuit current. The former is the most dominant participant in the dynamic power consumption. It comes from charging and discharging of the capacitance observed at circuit outputs. The latter is considered a minor participant in the dynamic power consumption and arises from the fact that modern computing and digital circuits use NMOS and PMOS transistors as building blocks. When current is switched between these two transistors in CMOS circuitries the PMOS transistor starts conducting while the NMOS transistor is still in conduction due to delay factors in transistor switching. The power consumption due to short-circuit current contributes to about 10-15% of the total power expended in digital circuits operation [18]. It can be seen from the relation showing the influencing factors on the dynamic power consumption [4]:

$$P_{Dynamic} = \alpha\, V_{dd}^2 \cdot C_{eff} \cdot f_{clk} \qquad \ldots\ldots (4)$$

Where $P_{Dynamic}$ is the dynamic power consumed by the processor, V_{dd} is the supply voltage, C_{eff} is the total capacitance of the nodes weighted, α is the activity factor which is related to how many logical transitions occur during device operation, and f_{clk} is the clock frequency at which the processor or digital circuit is operated.

On observing this relation it can be deduced that to reduce dynamic power consumption, there are four factors each of which has its impact on dynamic power consumption along with its impact on device performance.

The first factor to be discussed is the effective capacitance (C_{eff}). Reducing its value involves modifying basic architectural features of the device like transistor size and interconnecting path length. These parameters are very hard to modify and it involves making modification in the manufacturing technology of the device itself.

The second factor that influences power consumption is the activity factor (α). As modern computing chips are becoming more complex in functionality, the activity on the chip becomes increasingly larger. To address this issue, techniques must be developed to reduce any redundancy in activity and to reduce necessary logical transitions to a minimum. Several techniques have been proposed and introduced to address this problem, one of these is the clock gating [19,20]. This technique suggests a clock

topology generation heuristic based on the module activities and the sink locations in order to gate system clock from reaching idle section on the microprocessor. This technique proves to be very effective in reducing power consumption in a given microprocessor or digital device and is currently employed in a great number of commercially available systems like Intel Pentium 4, Pentium M, and X-scale microprocessors along with a lot of other microprocessor manufacturing companies.

The other two factors that influence power consumption are supply voltage (V_{dd}) and clock frequency (f_{clk}). It should be noted that for a given microprocessor, reducing clock frequency alone would reduce power consumption, but energy expended for completing a given task will remain almost the same as executing a given function will require a fixed number of clock cycles that will not change when clock frequency is varied, the only thing that will be different is the execution time. This fact can be verified from knowing the power is the rate at which the energy is expended or the rate at which the system performs a given work while energy is the total magnitude of work done within a given time frame.

$$P = \frac{W}{T} \qquad \ldots.(5)$$

$$E = W = P \cdot T \qquad \ldots.(6)$$

Where (P) is the power in Watts, (E) is Energy in Joules which also defines the work (W), and (T) is time in seconds. The concept work in the context of computing involves the execution of programs to fulfill a given task. Power is the rate at which the computing system expends energy while executing the given task. So while reducing clock frequency reduces the power the system is consuming, but to fulfill the task, the computing system will expend the same amount of energy. However, it would generate heat at half the rate it does when operating at full clock. So in order to make actual energy reduction, the fourth factor comes, the supply voltage (V_{dd}). Reducing this factor will lead to great reduction in energy consumption as the power expended is related to the square of the supply voltage. So the fourth way for reducing dynamic power consumption is by scaling supply voltage but as supply voltage decreases, the gate delay inside the processor increases making it necessary to reduce the operating clock frequency along with the

supply voltage so as to maintain error free operation of the computing system. The combination of scaling system clock frequency and supply voltage is termed as *dynamic voltage and frequency scaling* (DVFS) or as commonly used (DVS). It is the most widely adopted technique in modern computing system that can effectively reduce power consumption and heat dissipation in a given computing system. Almost all of modern mobile computing systems have their central processing units and their graphical processing units implement the DVS concept.

In a DVS ready processor clock frequency and processor supply voltage are scaled to a degree that will tailor the system performance to suit a given application. This means that it is not always possible to apply DVS when the task underhand requires maximum system performance to execute. Never the less this approach is currently providing a huge power reduction levels in several computing system applications especially the mobile computing applications. The DVS concept comes with its host of problems and special requirement for a voltage regulating module that will supply the DVS ready CPU with the voltages needed to operate its core at a given clock frequency. These issues will be explained in chapter three.

2.3. Challenges Facing VRM Design for Mobile Computing

Mobile computing and communication devices like smart phones, laptop computers, tablet computers, and personal digital assistants draw all the required energy for their operation from a battery. This limited power source must be backed by a high efficiency circuit design, power management scheme, and control system in order to extend the run time and the standby time for these devices. For this purpose switch mode regulators operated in pulse width modulation (PWM) mode are considered the prime pick for the design topology of an efficient VRM, delivering the power required by the core of a modern CPUs as other circuit designs, as can be observed in chapter 4, are lacking efficiency or the capability to deliver the required drive current to the designated load.

The main challenge in this case is the variable load nature. The core of the CPU requires a large operating current when it works at its full capacity which is the case when an application requires the full possible performance of the CPU under consideration. Again

applications executing on that CPU are different in their requirement for the minimum performance index that will deliver acceptable response from the running application. When there are no applications running on the computing device, the CPU goes to standby mode where its power requirements becomes only what will be enough to maintain registers and memory contents. The required load current is in the range of few milliamps to tens of milliamps. Several researchers have investigated this case and came up with solutions that could improve the overall efficiency of a VRM throughout a broader range of load currents. Both circuit techniques and control schemes underwent modifications that sought improving power efficiency and dynamics of the VRM supplying the CPU core.

2.3.1. Improving VRM Efficiency and performance Using Circuit Techniques

In this section a brief explanation of some circuit techniques that can be applied to current VRM designs in order to improve efficiency by reducing the effects of traditional circuit components drive methods with others that can get around the problems associated with the traditional ones. The techniques presented here can be implemented to improve the efficiency of the buck converter which is the prime converter used in the VRM design for battery operated mobile computing applications.

One of these techniques introduces a remarkable improvement in efficiency by replacing the rectifier diode with a synchronous rectifier [21]. This circuit technique involves replacing the traditional rectifier commonly found in Buck converter circuit with a synchronous switch. This modification can improve efficiency. The conventional buck converter circuit is shown in figure (2.3).

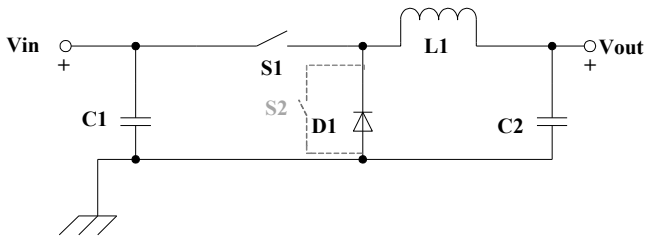


Figure (2.3) Basic buck converter circuit.

In this discussion it is considered that all other losses in the circuit like switch resistance and switching power requirements, inductor series resistance, capacitance series resistance, and power source internal resistance, are of negligible magnitude. In this case the maximum possible efficiency will be limited by the forward bias voltage of the diode ($V_{F)}$ .In a pulse width modulated converter where that main switching element (a transistor) conducts for a period (D), the diode conducts for the duration (1-D) of the switching period thus maximum efficiency obtainable from this circuit can be given by:

$$\eta_{\max}(\%) = \frac{V_{out}}{V_{out} + (1-D)\cdot V_F} \cdot 100 \qquad \text{.....(7)}$$

Where (η_{max}) is the maximum Efficiency, ($V_{out)}$ is the output voltage of the converter, (D) is the duty cycle of the PWM converter (the relative period when S1 becomes switched on) and it will be in the range 0<D<1 and due to practical circuit limitations in the form of propagation delay, rise and fall times and hysteresis, the value of the duty cycle will be narrowed from its two ends at least by 1 to 5% because in practical circuits larger or smaller values for duty cycle are unsustainable. (V_F) is the forward Bias voltage for the diode and it is about 0.7V for Silicon based P-N junction diode and about 0.3V for Shottky diode. As a mobile computing device is usually powered by a Lithium-Ion or Lithium-Polymer battery, which has a nominal cell voltage of 3.6 Volts, the maximum efficiency obtained using P-N junction diode will be 79%, and in the case of Shottky diode it will be lower than 90%. Here the introduction of a switching device that will replace the diode (shown in gray dashed line in figure 2.3), V_F can be made much smaller. In this case the switching device would operate as a synchronous rectifier that will replace the diode and will function similarly but with greater efficiency as V_F would be reduced considerably to a very small value depending on the switching device parameters thus boosting efficiency well above 90% when using the same assumption made in the beginning where all other losses are considered negligible.

While the introduction of the synchronous rectifier may seem to solve the problem of reduced efficiency, it comes with its host of problems that must be addressed and solved. The begin with, the new switching device will require its own drive signal and without careful driving of the synchronous rectifier, a temporary short circuit condition may arise during switching transients because of inherent switching device delays. This condition is

called cross current and it can be avoided by introducing a dead time period between the turning on and off of the converter switching devices. While this may come as a solution still it will tax the overall efficiency if not chosen properly and a solution to this problem would be by using adaptive dead time control as will be discussed in more details in chapter four.

Other circuit techniques are being proposed and implemented by several scholars and engineers in pursuit of higher efficiency and better performance such as using interleaved converters instead of a single converter supplying a given load as shown in figure (2.4).

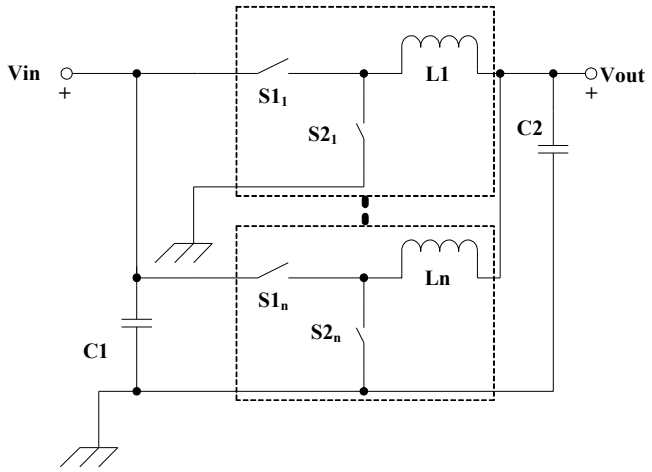


Figure (2.4) The interleaved buck converter topology

This arrangement despite its switch gating control complexity, offers several advantages, the first is reduced inductor size as the overall required inductor value is subdivided over the number of interleaved stages. The second advantage is lower ripple voltage value, and finally faster circuit dynamic resulting in better transient response, and lower losses per switch [21,22]. Additional circuit techniques will be discussed when reviewing previous work in the following sections.

2.3.2. Control Techniques Used in Buck Converter VRM Designs

In this section the various control issues associated with the operation of the buck-converter are briefly reviewed and discussed.

Normally, in a basic PWM controlled buck converter circuit when closed loop control is applied, a simple proportional controller built around analogue circuit components using voltage control feedback is shown in figure (2.5) [23].

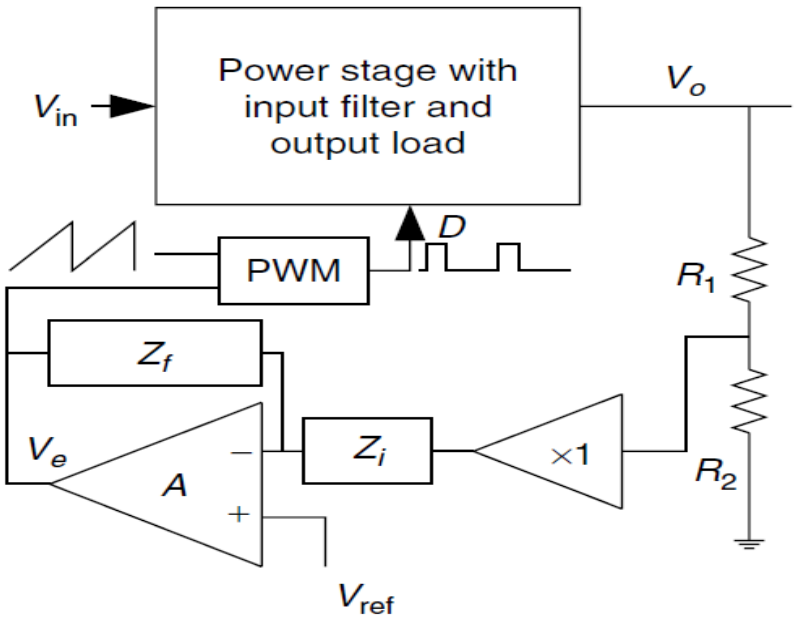


Figure (2.5) Block diagram of voltage feedback controlled PWM buck converter [23]

The analogue proportional controller that drives the buck converter consists of output voltage sample circuit which is the voltage divider consisting of R_1 and R_2. The output of the voltage divider is fed to an inverting amplifier through a buffer circuit. The inverting amplifier provides the proportional gain required to generate the error signal by subtracting the feedback signal from the reference signal (V_{ref}). The output of this stage goes directly to a PWM signal generation stage where it is fed with a saw tooth signal to a comparator circuit which will generate the drive signal for the control element in the buck converter circuit which is usually a power transistor switch. This simple approach is widely used in several analogue buck converters that supply relatively constant loads. But where more sophisticated load conditions are met, this simple voltage controlled proportional control scheme will not provide the required dynamics needed, as the case with the variable load presented by a microprocessor executing different applications. In this case other control schemes must be applied to meet load requirements. Current mode control and voltage/current feedback control schemes are applied to improve converter response. In addition to that, control methods more complicated that the proportional

controller are devised for the sake of improving system dynamic response and improve overall efficiency along the way. These control schemes include the proportional-integral (PI) controller, the proportional-derivative (PD) controller, the proportional-integral-derivative controller, and a variation on those basic controllers that will include enhancements required to modify the tune up parameters of these controllers to meet different load conditions. These improvements may include using digital techniques rather than relying on analogue techniques alone. Such control scheme may come as digital implementation of the analogue controller with variable tuning parameter modifications that are selected in accordance with feedback parameters changes. Fully digital implementation approaches for PID controllers are proposed by several researchers. These can also include artificial intelligence methods like genetic algorithms, neural-networks, and fuzzy logic controller or any combination of these techniques.

Whatever the control strategies adapted for such a system, they can be classified into two distinct sections, namely a linear control model and a nonlinear control model. Linear control strategies use linearised dynamics behaviour for a certain operating point, depending on the mathematical model of the buck converter under design. Nonlinear control strategies use the dynamic model of a buck converter to design a controller with variables parameters depending on the mathematical model of the converter system. Many researchers and designers have recently showed an active interest in the development and applications of nonlinear control methodologies in designing converter controllers [24] using a combination of neuro-fuzzy, fuzzy-neural along other control methods. While these methods are very promising in providing the response required by many converter applications, they are computing intensive and require DSP processing powers to realize.

The next sections will contain a review of previous works done in circuit and control enhancements.

2.4. Previous Works Related to VRM Efficiency and Performance Improvements

In this section a review of the past works done by scholars and researchers in improving the performance and efficiency of Buck converter based VRM. These

improvements are made by introducing novel ideas in circuit design, component selection, and control schemes implemented in the design of a VRM. The following sub sections will cover some of these innovations and developments.

2.4.1. Previous Works Related to Buck Converter Circuit Technique Improvement

The basic design techniques for a buck converter based voltage regulating module were shown in the previous section. Whether a single phase (figure 2.3) circuit or a multi phase (figure 2.4) circuit is chosen, the functioning of these circuits has been extensively investigated and their component selection scheme has been refined to deliver a state of the art performance. Still there is a need to push performance and efficiency further with regard to modern computing circuit requirements and operational behavior. In this respect researcher come up with new circuit techniques where circuit topology and/or elements were modified or additional elements installed for the purpose of improving operational efficiency and dynamics of the system under development.

A circuit modification was proposed by K. Yao et al. [25] whose addition of coupled windings to a multi-phase buck converter yielded a novel circuit topology that has improved converter efficiency without compromising its transient response. They have proposed an integrated magnetic structure in order to use the same magnetic cores previously found in the basic converter design. It is also said that these circuit improvements resulted in reduced voltage and current stresses on switching devices in addition to improved efficiency while maintaining all the usual features of the traditional buck converter such as easy system stability and remarkable dynamic response.

L. Jieli et al. [26] motivated by modern microprocessor power demand have proposed the use of coupled inductors in multi-phase buck converters for scalable design applications and claim that their approach would improve the transient response of the converter over a load range of 15% to 100% . Their approach was tested on a four-phase converter module and has shown an interesting 23% reduction in peak-to-peak current ripple over separate core circuits.

A circuit modification proposed by K. Yao et al. [27] suggests using a tapped inductor in the buck circuit topology instead of the conventional single inductor especially in the cases where V_{IN}/V_{OUT} ratio is large which will result in a small duty cycle of less that 10% driving the control switch element in the buck converter making it difficult to maintain stable control over the converter operation. The proposed topology solves this problem by extending the required duty cycle and along with it enhances the overall efficiency of the buck converter.

Another circuit enhancement proposed by P. Xu et al. [28] suggesting the use of active-clamp couple to a tapped inductor buck converter circuit would result in higher efficiency performance due to extending control switch device duty cycle by implementing the tapped converter topology and enhanced efficiency where part of the leaked energy would be recovered along with reducing voltage spikes across switching device by the active clamp thus reducing the stress on the switching device along the way. This approach delivers significantly better efficiency and performance in the case where the input / output voltage ratio is large.

Several additional circuit enhancements can also be observed in researchers work that were devised to provide additional operational safety, load protection and to improved VRM reliability by implementing short circuit protection using current limiting [29], intrinsic safety [30], or frequency foldback techniques [31].

2.4.2. Previous Works Related to Buck Converter Controller Design Enhancements

Designing a controller for the buck converter can be relatively simple as the case where the basic topology is implemented and an analogue proportional controller is used to control the operation of the buck converter. While this approach can be possible to implement for relatively constant loads and where efficiency is not of prime importance, it will not be possible to implement in cases where faster response and higher efficiency figures are required and being capable of maintaining these high levels of performance while dealing with loads that vary over a wide range. Some of these enhanced controllers may be possible to implement in analogue circuitry, others may be a hybrid of analogue and digital combination while others may be implemented using fully digital means.

The following works present the trends followed by researchers and scholars in the field of designing digital control systems for the voltage regulating modules that would yield better efficiency and performance figures.

G-Y. Wei and M. Horowitz [32] have presented a fully digitally controlled VRM that have adaptive load voltage feature suitable for supplying modern processors that have DVS capabilities. The controller devised is a digital PID and the whole system was fabricated on a single die using 0.8μm process. The resulting chip has DSP like computational power so as to facilitate for the implementation of the digital PID along with other required control functions. The use of fully digital controllers has its merits in being more immune to noise and temperature variations and flexible adaptability to varying load and source conditions and while their analogue counterpart suffers from these drawbacks, they are less power consuming and sometimes cheaper to implement.

In reference [33] V. Yousefzadeh and S. Choudhury introduced a method for designing a non-linear digital PID controller where the proportional, derivative and integral gains are selected according to input error signal value in order to improve the dynamic response of the designed converter that was implemented in a two phase buck converter for a point-of –load VRM circuit implemented in computing application. In this controller design a PID gain parameters look-up table is pre-computed for different quantized error values for error signal and stored inside the buck converter control chip, the *Ti* UCD9112, to provide for a look-up table based digital compensator for the PID controller. This approach showed improved load transient response of the designed point-of-load VRM module.

G. Feng et al. [34] proposed a digital control algorithm for DC-DC buck converter that can achieve optimal dynamic performance using the concept of capacitor charge balance by predicting the optimal transient response for a DC-DC converter during a large signal load current change, and while at steady state conditions a conventional PID control algorithm is used. This approach was implemented on an FPGA platform and the obtained results showed improved dynamic performance when compared with other classical control methods in power converters. While this control method improves system dynamic response, it has no effect on improving power efficiency of the controller. Further more, the math intensive algorithm requires high speed math capable platforms to realize, making it not applicable for mobile computing applications.

Another control approach that is suited for battery operated computing applications is a digital controller proposed by X. Zhang and D. Maximovic [35]. Their controller is intended to work in PWM mode for regular loads and switches to pulse frequency modulation (PFM) on light loads for improved efficiency. The PWM converter uses a digital input feed forward concept realized using a single comparator – counter based analogue to digital converter for sensing input voltage. The results show that implementing this method improves the dynamic response of the buck converter. The mode switching between PWM and PFM is done automatically inside the controller which is implemented using FPGA platform.

Artificial intelligence (AI) based controller designs have gained great popularity in modern controllers implemented in several application fields including voltage regulating. Neural networks and fuzzy logic in combination with other techniques have been used to design successful controllers that exhibited remarkable performance improvements over their classical counterpart. K-H. Cheng et al. [24] proposed a fuzzy-neural sliding-mode control system for power electronic converters. This controller consists of a neural-network based controller and a compensation controller. The compensation controller is used for the purpose of compensating for approximation errors between the neural controller and the ideal controller. This AI control method was applied to a forward DC-DC converter and used online parameter tuning based on Lyapunov stability theorem for guaranteed system stability. The converter under test showed fast transient response even with severe cases of load and input voltage fluctuations. This approach while effective, requires high computational power to accomplish making the resulting controller unsuitable for mobile computing applications.

Several AI based controllers are proposed with varying degree of complexity and computational power requirements. These AI based controllers are favoured over non-linear model based controllers as being less demanding in computational complexity. In addition to that they employ human experience of the plant in designing the controller which promises enhanced results without going into complex mathematical derivations. W-C. So et al. proposed a design for a fuzzy logic controller (FLC) suitable to implement in DC-DC converter [36]. The developed controller has been tested using computer simulation then was implemented on a DSP evaluation module based on *Ti* TMS320C50 DSP processor and this system was attached to a simple PWM converter where the output

was sent to drive the switching element and the feedback was the load voltage. The developed controller showed that fuzzy logic and expert system based controllers are capable of meeting the requirements of multitude of applications with high degree of success and performance.

P-Z. Lin et al. have proposed a design of an FLC for a buck converter using type-2 fuzzy set [37] which is supposed to have the capability to handle rule uncertainties and undetermined membership grades more gracefully. The designed controller was tested using a simple buck converter and the FLC was implemented on a desktop computer provided with a servo control card that has A/D and D/A channels along with digital I/O. The experimental results showed that this approach in designing fuzzy logic controllers can achieve better robust characteristics for line and load variations making it attractively suitable of DC-DC converter applications.

A.R. Ofoli and A. Rubaai [38] have demonstrated a real time implementation of an FLC for designing a DC-DC converter. A low cost general purpose controller namely the PIC16F877 from Microchips®, was used to generate the PWM drive signal for the converter. The designed controller was tested against an existing PI controller and reported that their system has yielded better dynamic performance. The fuzzy logic control operation was done on a desktop computer equipped with data acquisition system that was used to interface the control signals and feedback signal of the system under test.

A.G. Perry et al. [39] presented a novel design for PI-like FLC for a DC-DC converter. Their approach allows the small signal model of the converter along with linear control design techniques to be implemented in the early stages of the FLC design which in turn makes performance and stability assessment easier. Simulation and experimental design verification proved proposed controller design feasibility.

2.5. Chapter Summary

This chapter contained an analytical review for the power consumption in modern digital systems and some methods to make them more power efficient. It has been shown that the VRM is a vital key element in deciding the operational power efficiency of any digital device. Some circuit techniques to improve the performance and efficiency of the VRM were investigated along with a review for modern control systems adaptable for

DC-DC converters. The modern trend in designing controllers relies on AI techniques and the FLC showed great promises for implementation in VRM's designed for mobile computing device.

Chapter Three

System Components Characteristics and Selection to Design Efficient VRM for DVS Ready Processors

3.1. Introduction

This chapter, presents the dynamic voltage and frequency scaling (DVS) concept, in addition to describing the VRM system component selection after defining the processing element for which the VRM is being designed. In addition to that, the chapter contains a description of the power source which is usually a Lithium-ion battery is also investigated and its impact on VRM system design is studied.

3.2. The Concept of Dynamic Voltage and Frequency Scaling

Dynamic voltage and frequency scaling (DVS) is a technique that has been devised as a method for reducing energy consumption in modern high performance computing and digital systems [2,3,4,5]. This scaling of the voltage and operating frequency of a computing element or a digital circuit becomes possible when peak device performance is not required for the task under execution [5,6]. The reduction in energy consumption is a very important issue in all lines of modern industry, the electronic industry included, as the reduction of carbon dioxide emission became the prime influential factor that affects the changes the global environment is suffering from. Battery operated digital devices of all types gain several benefits from implementing the DVS concept as it will provide solutions for thermal problems in addition to extending battery life.

The main idea behind the DVS technique is based on the fact that power consumption is a quadratic relation with processor supply voltage as has been shown in chapter 2 section 2.2.2.

In the semiconductor devices, supply voltage and maximum operating frequency f_{clkMAX} are related through the time delay of the digital circuit as follows [5]:

$$t_d = k \frac{V_{dd}}{(V_{dd} - V_{th})^{\alpha}} \cdot \alpha \frac{1}{f_{clkMAX}} \qquad \text{……..(7)}$$

Where t_d is the time delay, k, V_{th}, and α are constants dependent on the manufacturing technology of the semiconductor device.

The benefit of implementing the DVS technique is that clock frequency of the processing unit can be varied to suit the requirement of the task being executed and as the clock frequency is varied, along with it the supply voltage can be varied as well. For any given software being executed on a certain processor, there is a minimum computational power requirement so that the program executes within the recommended time frame to suit the given application. So if during execution time the processor becomes idle, it means the associated task can be executed at a lower frequency since it requires lower performance from the processor. This can be associated with lowering the supply voltage accordingly. In this manner, a task given to the processor would be executed after modifying the processor clock frequency and operating voltage to produce the performance that suits the given application without generating slack time for the processor. Accordingly, the power consumption of the processing device is reduced as much as possible with out sacrificing system performance by reducing processor's performance to the degree where it will execute the given task throughout the entire recommended execution time frame. Figure (3.1) shows the activity of the processor during execution time.

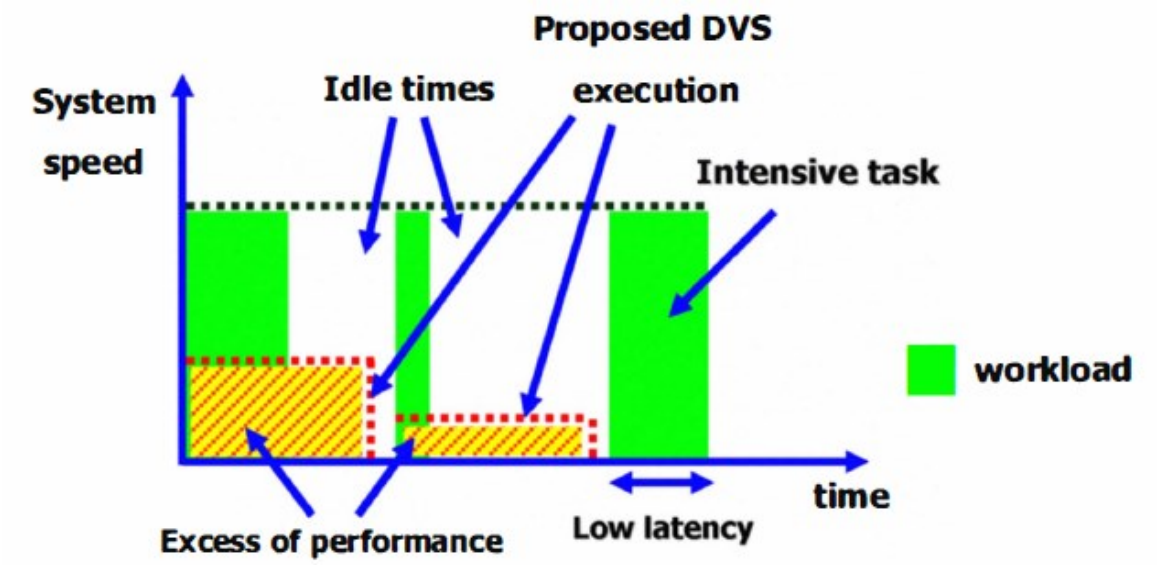


Figure (3.1) Illustration of processor activity during execution time of different applications with different performance requirements [5]

To implement the DVS system into a digital or microprocessor system, four essential elements are required: the software (SW) inclusive of operating system and application, the power supply (PS) that generates the required range of operating voltages, the system hardware (HW) that has the capability to operate over a wide voltage range, and a DVS scheduling system that will decide the required voltage and frequency that generate the performance suitable for the given task. These components are shown in figure (3.2).

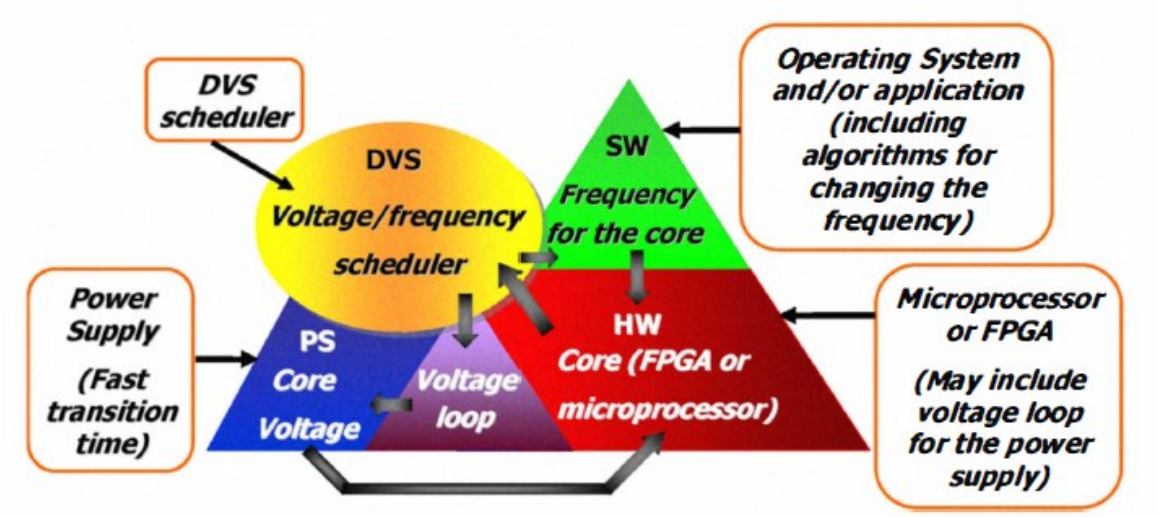


Figure (3.2) Components of a digital or computing system implementing the DVS concept [5].

The DVS system has gained wide implementation in modern computing systems especially the mobile equipments like smart phones, PDA's, portable game consoles, tablet computers, netbook computers and notebook computers. In these equipments two prime factors are required: increased performance and decreased energy consumption leading to longer running times from a given energy storage device. The DVS system addresses these requirements due to a fact that only few applications require the full performance of the processing unit or units inside the mobile device. So by varying the clock frequency the performance of the processing unit is varied and any setting below top performance allows the supply voltage to be scaled, thus making reduction in the energy required to perform the task. While processors generally are operated from a fixed voltage source and an important demand here is that the regulator must have a capacitor that is large enough to smooth down the large current spikes produced by the processor while in operation.

The voltage regulating system suitable for powering DVS ready processors is essentially unlike a conventional VRM as in addition to the voltage regulation task, it has to change that voltage to meet the demand of the DVS system. So the design of the VRM suitable for a DVS system can be directly related to the amount of power that system requires [4]. For instance for low power embedded systems built for the purpose of operating remote sensing systems will require a small size VRM with high efficiency over the entire working voltage range in addition to having fast output voltage transmission as required by the changing load conditions. As for applications where the VRM is required to supply larger amount of power as the case of desktop and laptop computers, the power consumption will vary over wide range from several tens of watts when the processor is working at peak performance levels to few milliwatts when the processor goes to sleep mode. This presents the VRM designer with the challenge of maintaining high efficiency over this wide power range. Some designers change operating mode from PWM at heavy loads to PFM under light loads to augment system efficiency at lower power levels [32,35,40]. This technique does boost the efficiency at lower power output levels to a certain limit, still there is much space to augment efficiency by implementing a more sophisticated circuit technique.

3.3. DVS Ready Processors Features and Requirements

The DVS ready processors have distinctive features that allow them to operate at several clock frequencies and supply voltages with different levels for implementing the DVS approach to improve the overall system efficiency.

Microprocessors from several manufacturing firms now support the DVS technique, even before that there was a concept emerged from Intel called Speed Step that was used to switch between two operating frequencies and voltages so when the mobile computer operates from wall outlet it adopts the maximum performance settings for frequency and processor's core supply voltage, while when operated from the internal storage cell it reduces the operating clock frequency and circuit supply voltage to a lower value to prolong system run time on the battery. DVS ready processors are widely available, they include processor from various manufacturers like the Intel processor series of Pentium M, Core, Core2, and the recent Core i series, the AMD Athlon and Opetron series, the Caruso processor form Transmeta, the cortex series from ARM, the Tegra series from nvidia and a plenty of other chip manufacturers are offering DVS ready processors for Portable applications.

In this work, the X-Scale processor PXA270 from Intel Corporation has been selected as a target processor for which the smart voltage regulating module is designed to supply its core voltage, this was partially because of the availability of all its electrical properties and power requirement documentation along with being implemented in several mobile applications. The X-Scale microprocessor series were intended to continue the series StrongARM microprocessors that were developed at Digital Equipment Corporation and later being taken for further exploitation and development by Intel Corporation and later sold to Marvell Semiconductor Inc.[41]. These processors gained large popularity due to the huge market size and rapid growth of the demand for hand held computing devices like PDAs , netbook, eBook readers, and smart phones. The applications that run on these devices can range from simple text reading or messaging to surfing web pages and streaming compressed videos. Therefore, applying DVS technique will greatly reduce the average energy consumption of the hand held device and extend the equipment battery run time and therefore extend battery life as a result of longer periods between battery charging cycles.

3.4. Description of Target Processor

The PXA270 Processor has been chosen as the target processor for which the smart voltage regulating module is designed. This choice came from the fact that the PXA270 is a highly integrated system-on-chip (SoC) that found wide application in handheld battery-powered devices such as PDAs and smart phones. It is suitable for designing mobile devices requiring substantial computing and multimedia capability with very low power consumption [42].

This processor contains a high-performance CPU along with a graphic coprocessor in addition to a large variety of integrated peripherals and functions. It has separate power supply domains for the processor core, memory, and peripherals so that designing low-power system becomes possible. The processor provides several dedicated control signals in addition to an I^2C interface to connect to an external power management system which eases the task of operating the device under DVS management [43].

In any system design, factors such as operating conditions, application workload, environmental considerations and the sophistication of the device's power management software determine the amount of power consumed during device operation. When designing a given product using the processor mentioned, it is important to take into account where the device is intended to be used (such as high temperature environments) and what it is expected to do for an end user such as playing a game, watching videos or doing simple email transactions as these will have their impact on selecting the proper operating processors core frequency and voltage for better battery energy utilization.

The Intel PXA270 processor uses a complex power management system that makes power utilization task feasible. The power management system requires designing several voltage supplies to power he different parts of the PXA270. The use of a power management integrated circuit (PMIC) has recommended by Intel [43] in order to exploit all the power saving possibilities that can be accomplished while using the PXA270 processor. But it is not necessary to incorporate a PMIC into a PXA270 processor-based system and instead, it is possible to power the processor using four separate power regulators only but this trade-off for simplicity comes with increased power consumption,

loss of flexibility in peripheral voltage selection and added requirements for battery backup.

3.4.1. Description of Target Processor Power Requirements

Most modern microprocessors especially those coming with integrated peripheral devices require complex power supplies to furnish their operating voltages/currents requirements. Table 3.1 contains a detailed description for the voltages and the allowable tolerances associated with them that are needed to power the PXA270 processor. Intel suggests a minimal power supply circuit shown in figure (3.3) that can provide all the necessary operating voltages [43]. It can be perceived that by careful selection of voltage regulating modules, three voltage regulators can supply the nine input voltages required to operate the PXA270. Using a 1.1 V, a 1.3 V, and a 3.3 V supply all regulated at ±10% as indicated in table 3.1, will satisfy all requirements for the nine voltage domains.

Table 3.1: External Power Supply Descriptions for PXA270 Microprocessor [42]

Power Domain	Enable[1]	Units	Specified Levels (Volts)	Tolerance (%)
VCC_BATT	None	Sleep-control subsystem, oscillators and real-time clock	3.0	± 25
VCC_IO	SYS_EN	Peripheral input/output	3.0, 3.3	±10 (@ 3.0 V =10%, -10.3%)
VCC_LCD	SYS_EN	LCD input/output	1.8, 2.5, 3.0, 3.3	+20,-5 (@ 1.8 V) otherwise ±10
VCC_MEM	SYS_EN	Memory controller input/output	1.8, 2.5, 3.0, 3.3	+20,-5 (@ 1.8 V) otherwise ±10
VCC_BB	SYS_EN	Baseband interface	1.8, 2.5, 3.0, 3.3	+20,-5 (@ 1.8 V) otherwise ±10
VCC_USIM	SYS_EN	USIM interface	1.8, 3.0	+20,-5 (@ 1.8 V) otherwise ±10
VCC_USB	SYS_EN	Differential USB input/output	3.0, 3.3	±10
VCC_PLL	PWR_EN	Phase-locked loops	1.3	±10
VCC_SRAM	PWR_EN	Internal SRAM units	1.1	±10
VCC_CORE	PWR_EN	CPU and other internal units	variable 0.85 – 1.55	-5 +10

A fourth voltage regulator supplies the voltage for VCC_BATT. Although the voltage supplied by this additional regulator is the same voltage as a regulator already included in the design, this separate regulator must provide the supplied voltage in order to keep the

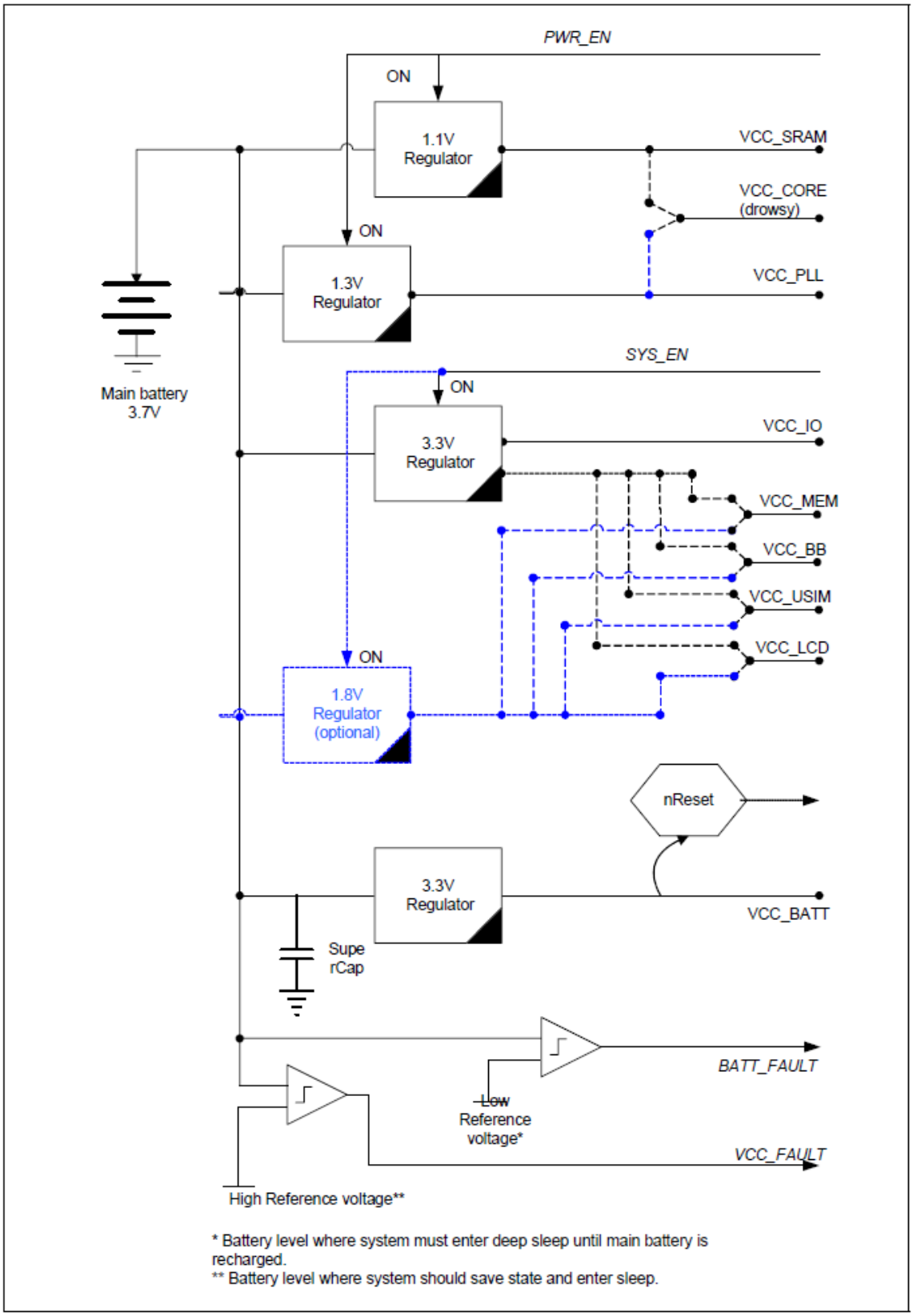


Figure (3.3) Suggested minimal power supply design for PXA 270 microprocessor [43]

voltage draw to a minimum as the current required to supply VCC_BATT is very small and the use of a regulator with very small current source capability will correspondingly draw small current from the power source of the entire system presumably a Lithium-Ion battery. The other 3.3 Volts regulator required powers the peripherals and must have a much larger current sourcing capabilities to fulfill the needs of these circuits.

In a mobile battery operated system, the power draw for the voltage supply in the manner described is not acceptable. The trade-off made for simplifying these nine supplies to three is by letting all peripherals work on a supply voltage of 3.3 V. If 3.3 V is unacceptable to the system designer, an additional fifth regulator of 1.8 V allows a margin of greater operating flexibility in the design without extensively adding extra system cost or increased complexity. The addition of a fifth regulator also allows for a mixture of 3.3 V and 1.8 V peripherals for use in the system design. Table 3.2 shows the relation between processor's core activity, core voltage, and Supply current.

Table 3.2: Power consumption expected for VCC_CORE power supply domain across differing workloads [43].

Frequency Point @ voltage V	Dhrystones 2.1 Current (mA)	Power (mW)	MPEG4 Decode current (mA)	Power (mW)	Power Stress Test Current (mA)	Power (mW)
624 MHz 1.55 V	658	1019	622	964	1006	1559
520 Mhz 1.45V	503	729	475	689	767	1112
416 MHz 1.35V	395	533	420	567	594	802
312 MHz 1.25V	297	371	333	416	436	545
208 MHz 1.15V	208	239	263	303	295	339

Table 3.2 shows the typical current consumption for the VCC_CORE power domain at room temperature, with different core supply voltage levels but with differing workloads using the Intel PXA270 Processor Development Kit processor card running low level boot code, with no operating system. The test figures obtained using the following bench marks and test conditions [43]:

- Dhrystones 2.1 - Dhrystones workload. Configured to run 20,000,000 cycles with LCD disabled.

- MPEG4 Decode – Done with unlimited frame rate on Intel® IPP Performance Suite v4.0 for the Intel PXA270 processor for Linux using QVGA LCD with frame buffer in SRAM.

- Power Stress Test Code – In the test a low level code executing a repetitive test case of back to back 64bit MAC instructions in an infinite loop. This stress code is written specifically to subject the core power domain to yield data at the higher end of usage. The figures obtained in this test do not represent a real common place application and only indicative of processors peak possible performance.

The PXA270 processor has several operating modes that can help managing power consumption to boost battery run time. Table 3.3 shows these operating modes along with a brief description.

Table 3.3: The Operating Modes of PXA270 Microprocessor [44]

Operating Modes	Description
Normal mode (Run/Turbo mode)	All external power supplies are enabled and all internal domains are powered. The CPU core and peripherals are fully functional.
Idle mode	The clocks to the CPU are disabled but context is retained. The peripherals continue normal operation. All power supplies are enabled. An interrupt assertion causes the transition back to normal mode.
Deep Idle mode	The core frequency is at 13 MHz (CCCR[CDPIS] is set) and the processor is in idle mode.
Standby mode	The clocks to the CPU are disabled and the CPU is placed in a low leakage state but context is retained. All external power supplies are enabled. Each internal SRAM bank can be independently placed in a low-power mode where the state is retained but no activity is allowed under program control. The PLLs are disabled and peripheral operation is suspended. An interrupt assertion causes the transition back to normal mode.
Sleep mode	All internal power domains except VCC_RTC and VCC_OSC are optionally powered down. All clock sources except the real-time clock (RTC) and power manager are disabled, and all external low-voltage power supplies (VCC_CORE, VCC_PLL, and VCC_SRAM) controlled by PWR_EN are disabled. Recovery is initiated by external wake-up events or select internal wake-up events. A system reboot is required because the program counter is invalid.
Deep sleep mode	All internal power domains except VCC_RTC and VCC_OSC are powered down. All clock sources except the real-time clock (RTC) and power manager are disabled, and the external low-voltage supplies (VCC_CORE, VCC_PLL, and VCC_SRAM) controlled by PWR_EN are disabled. The high-voltage power supplies (VCC_IO, VCC_MEM, VCC_LCD, VCC_BB and VCC_USIM) controlled by SYS_EN are disabled. The active internal power domains are powered from one of three internal regulators driven from the backup battery signal, VCC_BATT. Recovery is initiated by external or select internal wake-up events and requires a system reboot, because the program counter is invalid.

3.4.2. Description of Dynamic Core Voltage Management and VRM Required Specifications.

The PXA270 processor supports dynamic management of power consumption, which is based on the computing performance required to run an application at a given time. These features enable the processor to modify processor's core frequency and core supply voltage during operation. Thus dynamically modifying computing performance to suit the current computing workload with minimum slack time. This is a DVS system combining the operation of the PXA270 processor with a power management circuit under the control of a DVS scheduling software can run a wide range of applications using only a fraction of the battery power that would be required if the system would run at a fixed frequency and voltage value that delivers the peak computing workload.

The VRM that can deliver the voltages needed must have these minimum features to be capable of supplying the required core voltage (VCC_CORE) to support DVS power management for the Intel PXA270 [44]:

• High-efficiency I^2C programmable buck converter output providing VCC_CORE in the voltage range 0.85-1.55 V (-5%/10%) with a default/reset output in the same range.

- I^2C programmable output voltage ramp rate with a default/reset ramp rate of 10mV/S.
- The VCC_CORE regulator must support a minimum set of these six output voltages: 0.85, 0.95, 1.1, 1.2, 1.3, 1.4 and 1.55 V.
- The VCC_CORE regulator must also support programming the voltage ramp rate over a one decade range of the nominal default value (10mV per Sec.). Ramping is accomplished via a smooth analog ramp driven by an internal ramp generator, or through a series of micro steps of 10-25 mV per micro step, which are performed sequentially after a small delay to make up the requested change in voltage. Faster ramp rates can, in practice, be limited by the capabilities of the regulator and by the amount of bulk capacitance on the buck converter that delivers core voltage.

Controlling the core voltage is accomplished by communicating with the VRM via the I^2C serial bus. So the VRM must have communication capabilities and additional feature to be compatible with DVS enabled computing system. The bus transfers data one byte at a time to the smart VRM. Register loads are 8 bits wide, although not all bits need be utilized by accompanying circuitry.

The PXA270 processor communicates with the smart VRM using the I^2C serial bus. The flexible I^2C controller in the processor can pre-load a buffer with a series of commands, or multi-byte commands of any size, up to a total of 32 bytes of command address and data. The I^2C controller can be programmed to send a series of commands with programmable intervals between groups of commands to accommodate a variety of different power controllers and regulators [44].

The I^2C interface runs in either standard mode at 40 kHz or fast mode at 160 kHz using standard 7-bit addressing. The hardware general call and 10-bit extended addressing are not supported by the PXA270 processor.

3.4.3. Preparations for PXA270 Core-Frequency Change

When the need arises to change the PXA270 core frequency the task can be accomplished in several ways:

1. Selecting the 13-MHz clock source
2. Changing the core PLL frequency
3. Enabling turbo or half-turbo mode

Modifying the following parameters in the Core Clock Configuration register (CCCR) changes the clock frequency the PXA270 core runs at [44] following the settings shown in table 3.4.

Table 3.4: The PXA270 core clock configuration register (CCCR) settings [44].

Core Run Freq (MHz)	CLKCFG[T]	Core Turbo Freq (MHz)	CLKCFG[T]	CLKCFG[HT]	CCCR[L]	CCCR[2N]	System Bus (MHz)	CLKCFG[B]	CLK_MEM (MHz)	CCCR[A]	SDCLK<2:1> SDRAM Clocks (MHz)	MDREFR[KxDB2]††††	Synchronous Flash (MHz)	MDREFR[K0DB4]	MDREFR[K0DB2]	LCD (MHz)
13†	X	—	X	X	X	X	13	X	13	X	13	X	13	X	X	13 or 26††
91†††	0	—	—	0	7	2	45	0	91	0	45	1	22.5	1	1	91
104	0	104	1	0	8	2	104	1	104	1	104	0	52	0	1	52
156	0	156	1	1	8	6	104	1	104	1	104	0	52	0	1	52
104	0	312	1	0	8	6	104	1	104	1	104	0	52	0	1	52
208	0	208	1	0	16	2	208	1	208	1	104	1	52	1	X	104
208	0	312	1	0	16	3	208	1	208	1	104	1	52	1	X	104
208	0	416	1	0	16	4	208	1	208	1	104	1	52	1	X	104
208	0	520	1	0	16	5	208	1	208	1	104	1	52	1	X	104
208	0	624†††††	1	0	16	6	208	1	208	1	104	1	52	1	X	104

NOTES:

† Not a PLL clock frequency. Refer to Section 3.5.7.7.

†† Use CCCR[LCD_26] to control this setting. See Table 3-31.

††† L = 7 (Core = 91.0 MHz) is used for hardware boot-up frequency only and must not be used for normal operation.

†††† KxDB2 represents K1DB2 and K2DB2

††††† 624 MHz is available on the PXA270 processor only. See the *Intel® PXA270 Processor Electrical, Mechanical, and Thermal Specification* and *Intel® PXA27x Processor Family Electrical, Mechanical, and Thermal Specification* for supported frequency product points.

But before performing a core-frequency change, specific steps must be followed to accomplish successful core operating frequency change and executing this sequence imposes some requirements and system limitations that can be summarized in following points [44]:

- All interrupts to the CPU are held, causing latencies for the peripherals.
- All current instructions, including incomplete fetches, are completed.
- All outstanding memory-controller transactions are completed.
- The system-bus clock stops for up to 150 µs. No new system-bus transactions are allowed during the change sequence.
- During this time, the LCD controller cannot transmit data to the LCD panel. If the panel cannot tolerate the 150-µs latency (for example, if it does not have a built-in

frame buffer), disable the LCD controller before initiating the core-frequency change.

- The USB host controller cannot access its own FIFOs or configuration registers. This might require disabling the USB host controller before initiating the core-frequency change.

- SDRAMs are automatically placed in self-refresh mode.

- The CPU clock stops for up to 150 µs.

Table 3.5 summarizes the step sequence needed to be followed to accomplish successful clock frequency change for the PXA270 Core [44]:

Table 3.5: Summary of step sequence for PXA270 core Clock frequency change [44]

Description of Action	Unit	Latency (cycles)	Type of Change		
			Turbo	Fast Bus	Core Freq.
Write to CP14 CLKCFG register (software); interrupts are held.	CPU	1 CPU	X	X	X
All current instructions, including incomplete fetches, are completed.	CPU	? CPU	X	X	X
All outstanding stores are completed.	CPU	? SB	X	X	X
Wait for synchronization. The CPU clock halts.	CPU	<20 CPU	X	X	X
Deny all bus requests from LCD, USB-H, DMA, CPU, and memory controllers.	PM	1 SB	—	X	X
Complete all memory control transactions (allow memory controller bus requests). Place SDRAM in self-refresh mode.	MEM	? SB	—	—	X
Synchronize clocks and power manager. Switch clock sources (done in hardware).	PM	<4 13M <8 SB	—	—	X
Core-frequency change sequence splits					
Disable PLLs if appropriate (xPDIS set).	PM	2 13M	—	—	X
Enable PLLs if appropriate (xPDIS clear). Wait for PLLs to lock.	PM	2000 13M	—	—	X
Synchronize clocks and power manager.	PM	<2 13M <4 SB	—	—	X
Core-frequency change sequence merges					
Set PLL and/or SB dividers.	PM	2 SB	—	X	X
Release system bus for all transactions.	PM	1 SB	—	X	X
Wait for synchronization.	PM	<20 CPU	X	X	X
Enable clocks, enable interrupts to the CPU, and begin execution.	PM	2 SB	X	X	X

NOTES:

X	Step is followed in the corresponding clock mode.
—	Not applicable
?	Variable—depends on system/software configuration.
13M	13-MHz processor oscillator
CPU	CPU
MEM	Memory controller
PM	Power manager
SB	System bus

An important function that is required for fulfilling the DVS operation is the availability of the I^2C bus on the Power management Controller which is the smart VRM in the case of the work under hand. So any platform that would be selected to work as an intelligent controller for the VRM design should incorporate the I^2C bus and support its operation. The next section will cover a brief explanation for this bus.

3.4.4. The I^2C Bus

The I^2C Bus is a serial bus originally developed at Philips Semiconductors and originally called 'Inter Integrated Circuit' bus or abbreviated (IIC) or (I^2C) bus [45]. This bus is very useful in interconnecting a number of device circuits using only a simplified number of connections and provides a common way for communicating with similar or different I/O devices using synchronous serial communication.

The I^2C Bus communication between two or any number of devices can be accomplished using two wire connection assuming that all devices share a common power return (ground). Figure (3.4) shows the I^2C interconnect between digital devices.

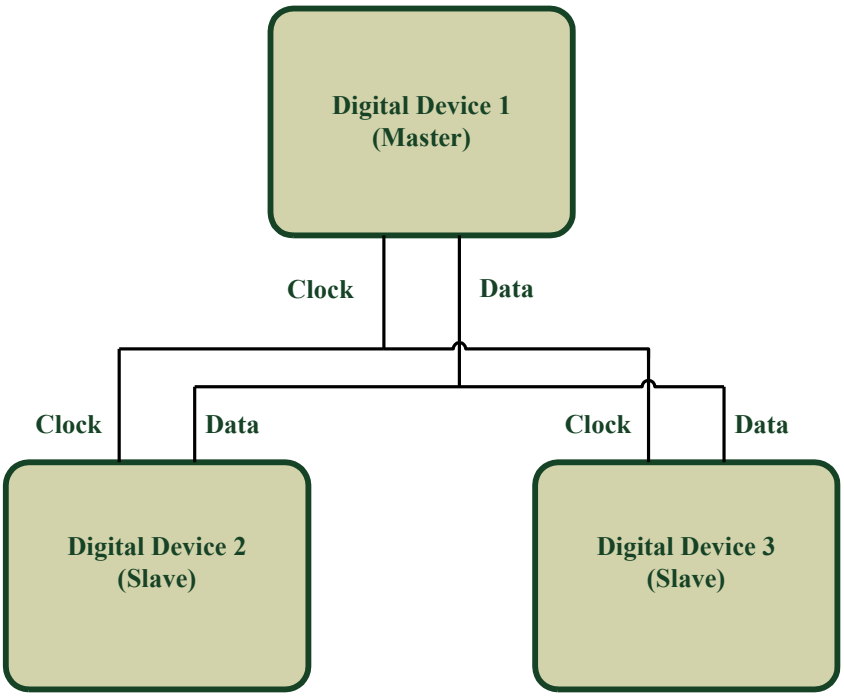


Figure (3.4) The I^2C device interconnect

The two lines that carry the I^2C bus signal are assigned different signals, the first one carries data signals and is bidirectional, the second one carries the clock signal that synchronizes data transfer between devices. There can be several Masters/Slaves combination on a certain interconnect, but there can be only one master at an instance and this will be the device that will initiate a data transfer on the data line which is also called the 'Serial data' or (SDA), and generates the clock pulses on the clock line also named the 'Serial Clock' or (SCL). The Master device can address up to 127 other slave devices. From the master a data frame is sent or received, and this data frame has a standard format set by the I^2C protocol as shown in figure (3.5)[45].

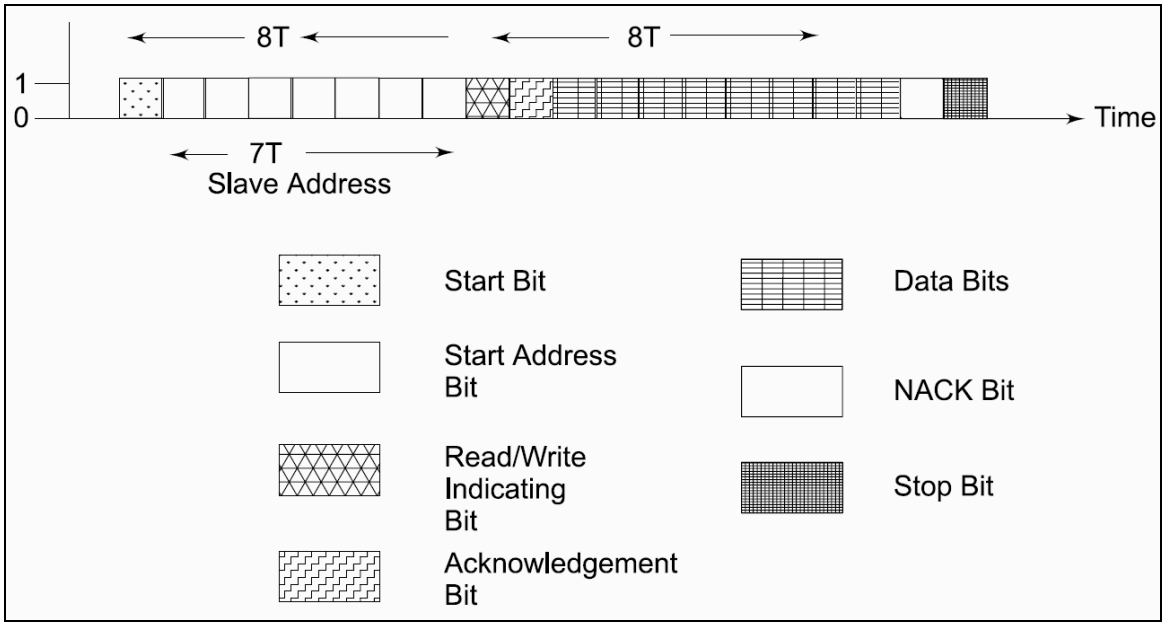


Figure (3.5) The I^2C synchronous serial bus data frame as defined by the standard protocol [45].

The I^2C bus protocol has a data frame of 20bit divided into seven fields, the following points explains the bit assignment of each field:

1. The first field is one bit wide and is defined as the start bit field.
2. The second field is seven bits wide; its function is to define the slave device address to which the data frames are sent.
3. The third field is one bit wide, the setting of this bit indicates whether a read or write cycle is commencing.

4. The fourth field is also one bit wide and is used to indicate whether the present data in the frame is an acknowledgment from a slave device.

5. The fifth field is 8 bits wide and is the I^2C device data byte.

6. The sixth field is one bit wide and is the negative acknowledge bit from the receiving device, if active, the acknowledgement after a slave device receives a data byte is not required, otherwise acknowledgement is required.

7. The seventh field is one bit wide and is reserved for the stop bit.

It should be mentioned that the start and stop bits in the I^2C protocol are similar to those found in the UART counterpart.

3.5. Smart VRM Circuit Components Selection for High Efficiency and DVS Compatibility

In this section an investigation on passive and active components used in buck converter design and their impact on converter efficiency is covered in addition to a review on the progress made in manufacturing processes and materials of design components that promoted better performance and efficiency of the end products.

The buck converter design requires passive components namely the inductors and capacitors, and active components like the PWM switching device and the synchronous rectifier device. Both are usually semiconductor devices which can be bipolar power transistor, MOS power transistors, or insulated gate bipolar transistors (IGBT). The ones which are suitable for the intended application falls in the category of MOS power devices.

3.5.1. Theory of Inductor Selection for High Efficiency PWM Buck Converters

Inductors are electromagnetic passive devices that play a major role in the success of the switch mode power converter design. It is an energy storage device that stores electrical energy in the form of a magnetic field. When the current flowing through an inductor changes with time, it creates a time varying magnetic field that induces a voltage in the

conductor that opposes the current that generated the magnetic field according to Faraday's law of electromagnetic induction. The inductance (L) is measured in the units of 'Henries' which is the ratio of the magnetic field generated by the current passing through the conductor over the value of that current.

$$L = \frac{\phi}{i} \qquad \text{.....(8)}$$

Where (L) is inductance in Henries, (Φ) is magnetic flux in Weber, and (i) is current in Amperes.

Any change in current passing through the inductor creates a changing flux that results in induced voltage across the inductor according to Faraday's law of induction. This voltage is given by:

$$v = \frac{d\phi}{dt} \qquad \text{..... (9)}$$

Substituting (Φ) with its equivalent from equation (8) results in:

$$v = \frac{d}{dt}(L \cdot i) = L\frac{di}{dt} \qquad \text{.....(10)}$$

The inductance can be interpreted as a measure for the amount of electromotive force generated per unit change of current. The polarity of this induced voltage opposes the direction of change in current according to Lenz's law [46]. Figure (3.6) shows the symbol of the ideal inductor along with a simplified practical equivalent.

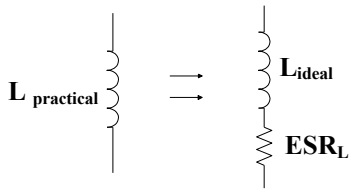


Figure (3.6) the Practical inductor and its Equivalent circuit

Where L is the ideal inductor and ESR_L is the effective series resistance of the inductor.

If not selected or designed properly, inductors can cause a multitude of problems like high losses, high voltage spikes which necessitate the addition of clamping devices or snubbers, noise coupling, and duty cycle restriction.

Inductor core material choice depends greatly on the frequency range the inductor is going to operate in. Usually, converter inductor design is aimed at the smallest size, the highest efficiency and adequate performance under the widest range of environmental conditions. But in reality, the core material that can produce the smallest size has the lowest efficiency, and the highest efficiency materials result in the largest size [47]. Thus, the inductor designer must make tradeoffs between allowable transformer size and the minimum efficiency that can be accepted. Power losses in an inductor can come from core material in the form of hysteresis losses and eddy current losses. Copper loss is the other important source of losses in inductor design and is due to winding material resistivity. Figure (3.7) shows the classical magnetizing hysteresis loop obtained subjecting a ferromagnetic material to DC current magnetization.

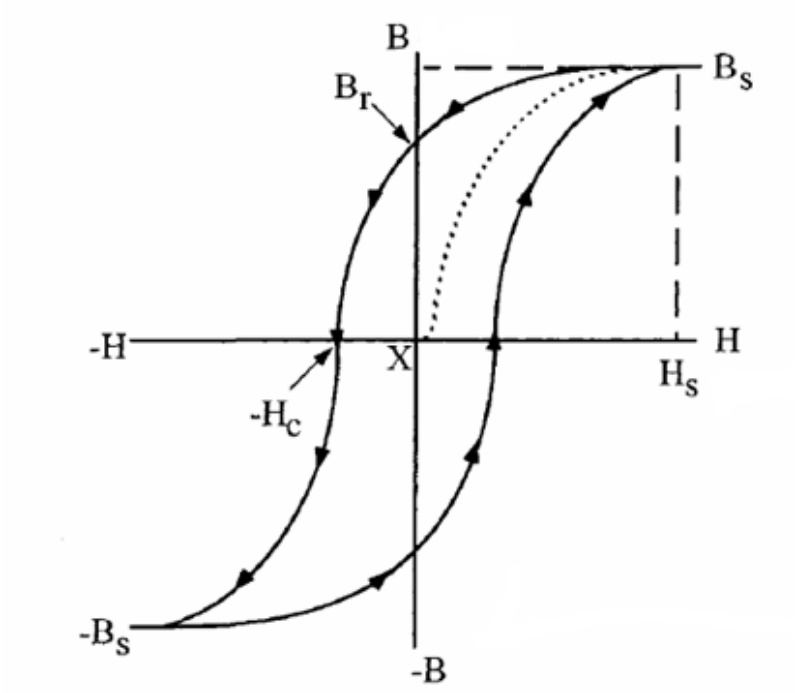


Figure (3.7) The magnetic hysteresis loop for a ferromagnetic core[48].

Where (B) is the magnetic flux density in Tesla (Weber/m^2), H is the magnetizing force in Ampere per meter (A/m) in SI units standard. The dashed curve indicates the initial magnetization action and as it is evident magnetic material reaction to magnetizing forces is nonlinear. The shape and geometry of the hysteresis loop is an indicative factor for magnetic materials performance along with other parameters like relative permeability of the magnetic material (μ_r). It must be noted that core geometry changes proportionally with the frequency of the applied magnetizing force [48] as shown in figure (3.8).

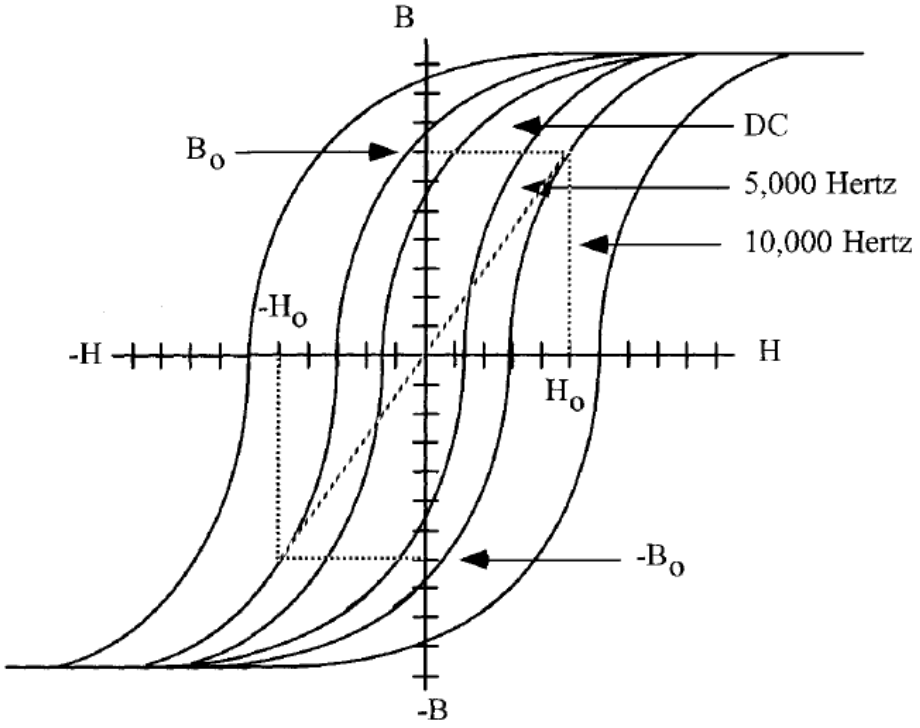


Figure (3.8) The typical B-H hysteresis loop for a ferromagnetic material operating at various frequencies [48].

In PWM converter operation the energy loss due to the changing magnetic energy in the core during a switching cycle equals the difference between magnetic energy put into the core during the on time and the magnetic energy extracted from the core during the off time, which occupies the first quadrant of the B-H loop, represents the operating region for positive flux-density excursions, because typical buck and boost converters operate with positive inductor currents. Hysteresis losses vary as a function of B^*n, where (for most ferrites) "n" lies in the range 2.5 to 3 [48]. This expression applies on the conditions

that the core is not driven into saturation, and the switching frequency lies in the intended operating range. Power loss due to eddy currents increase is proportional to the square of the applied inductor voltage, and is directly proportional with its pulse width.

Another influencing factor on inductor performance is a design factor called 'fill factor'. It is also called the 'Window Utilization Factor'. It indicates the fraction of the core window area that is filled by copper wire windings. It should be noted that round cross section copper wire does not pack perfectly which reduces fill factor resulting in the use of wires of thinner cross section for a given turns ratio which yields inductors with larger copper losses. The use of flat wire is highly recommended in application requiring high efficiency as they tend to pack perfectly inside the winding window with minimum space loss.

The selection of core material will be based upon obtaining the best characteristic on the most critical or important design parameter, and upon allowable concessions made on the other parameters. So, after analyzing several commercially available designs it can be said that most engineers will be favoring size over efficiency as the most important criterion, and as a result will select an intermediate loss factor on core material for their inductors. In general, designers will use Iron powder, Ferrite, Superflux, and Molypermalloy powder materials for inductors used in switching regulators working at frequencies below 100KHz. Switch mode regulators working at frequencies higher than 100KHz will require Ferrite, or Superflux as core material in designing the inductive component of the converter, and those working on frequencies higher than 1MHz will use Ferrite as core material [47,48]. Ferrites are ceramic materials of iron oxide, alloyed with oxides or carbonate of manganese, zinc, nickel, magnesium, or cobalt. Alloys are selected and mixed, based on the required permeability of the core. Proper care must be taken while manufacturing cores using powder technology is the fringing flux effect [48] that must be greatly taken care of to maintain high efficiency and low loss.

New magnetic materials are emerging from several manufacturing firms promising lower losses and better stability of magnetic core material through reducing thermal degradation of maximum flux density, higher Curie Temperatures and better aging factors. Würth Elektronik GmbH developed a new core material WE-PERM with 50% less deficit compared to standard material @ 500 kHz and 0.5 T with no thermal ageing.

This new core material is optimized for high ripple current because of extremely low core losses [49]. Another material introduced by Magnetic Inc. is claimed to be suitable for power supplies with switching frequencies above 800 kHz, and is optimized for transformer and inductor applications from 500 kHz to 3 MHz. Within this range, AC core losses are minimized and the loss versus temperature curve exhibits its minimum at a suitable elevated temperature (70°C to 100°C). In addition, the Curie temperature is quite high (>300°C), so that saturation flux density (Bmax) is maintained within the required value acceptable tolerance across a wide temperature range [50].

Designers of power converters and PWM switched regulators rely on commercially available inductive components because of the availability of manufacturers' literature containing tables, graphs, and examples that simplify the design task. The use of hand made inductors and the selection of its core material may result in an inductor design not optimized for size and weight. For example, Molypermalloy powder cores, operating with a dc bias of 0.3T, have only about 80% of the original inductance, with very rapid falloff at higher flux densities. When size is of greatest concern, then magnetic materials with high flux saturation would be first choice. Materials, such as silicon or some amorphous materials, have approximately four times the useful flux density compared to Molypermalloy powder cores. Iron alloys retain 90% of their original inductance at greater than 1.2T. Iron alloys, when designed correctly and used in the right application, will perform well at frequencies up to100kHz. When operating above 100 KHz, then the only material is Ferrite. The problem with Ferrite materials is that they have a negative temperature coefficient regarding flux density [47]. Thus the operating temperature and temperature rise should be considered carefully when calculating the maximum flux density required to handle load currents without sacrificing efficiency which will fall steeply when the core of the inductor get saturated at lower load currents due to fall in the value of core maximum flux density handling value.

Some of the industry standard core shapes used to design surface mounted inductors are shown in figure (3.9).

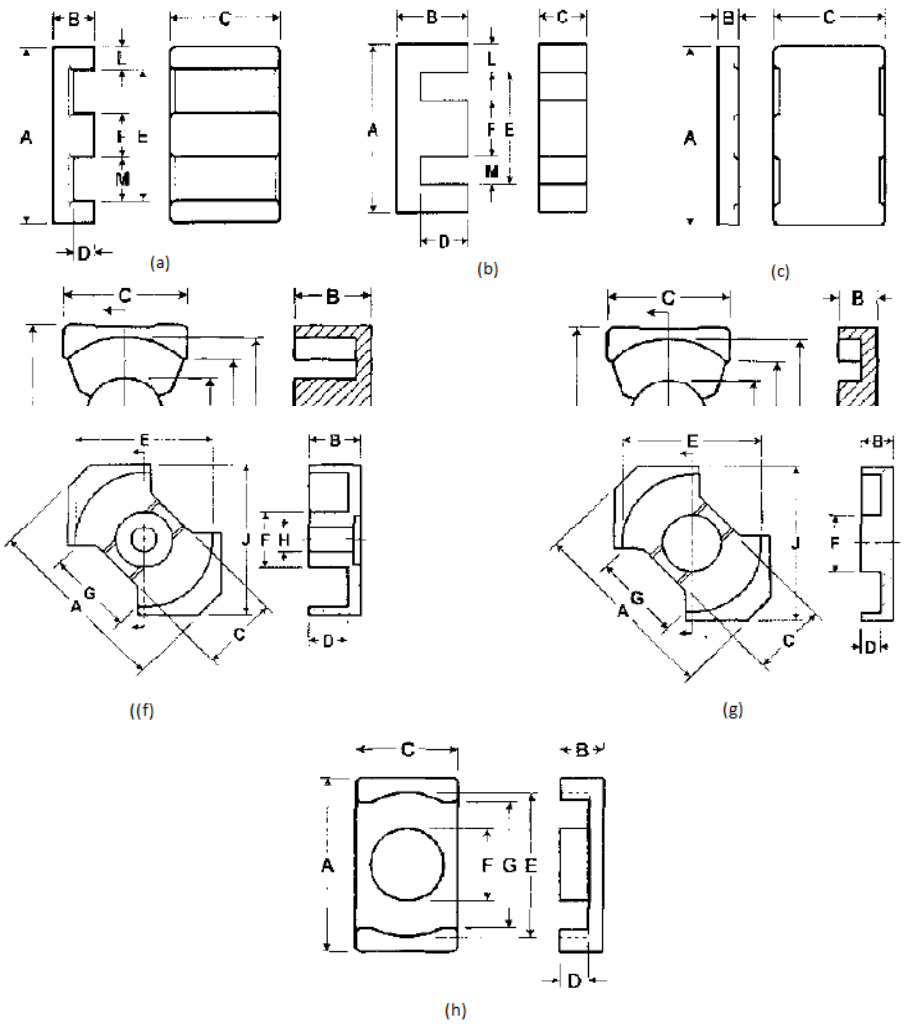


Figure (3.9) various standard shapes of inductor cores, a: Planar E-core, b: Traditional E-core, c: Planar I-core, d: Standard PQ-core, e: Planar PQ-core, f: Standard RM-core, g: Planar RM-core, h: Planar ER-core [48]

3.5.2. Theory of Capacitor Selection for High Efficiency PWM Buck Converters

The second passive device that has great impact on converter performance and overall VRM efficiency is the capacitor.

Capacitors come in various designs, materials and shapes, the function of the capacitor is also energy storage but unlike the inductor where energy is stored as a magnetic field, the capacitor stores energy as an electric field. The basic capacitor consists of two parallel

conductive plates of area (*A*), separated by a distance (*d*), separated by a dielectric with permittivity (ε). Figure (3.10) shows the construction of a basic capacitor.

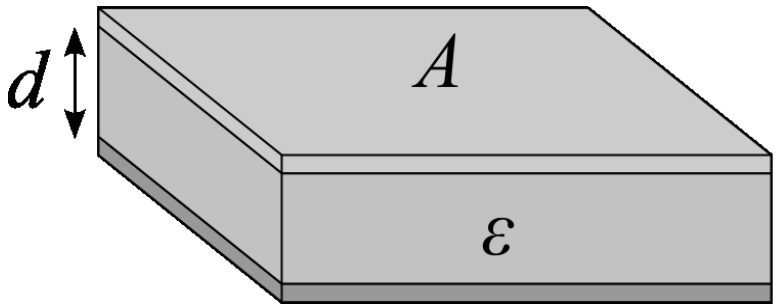


Figure (3.10) The Basic capacitor [46].

The capacitance *C* can be defined in the following terms:

$$C = \varepsilon_r \cdot \varepsilon_0 \frac{A}{d} \qquad \text{..... (11)}$$

Where (*C*) is the capacitance in Farads, (*A*) is plate area in m^2, (d) is the distance between plates in meters, (ε_r) is relative permittivity of the dielectric medium separating the two plates and it is equal to (1) for vacuum, (ε_0) is the absolute permittivity of vacuum space and is equal to 8.854 187 817*10^{-12} Farad per meter in SI standard units. Capacitance value can be influenced by several factors as can be seen from equation (11). These are: (*A*) the area where capacitance value is directly proportional to it, it is inversely proportional to the distance (*d*), and directly proportional to the relative permittivity value (ε_r).

The real capacitors have several parasitic components that set them apart from the ideal capacitor, and these component vary according to capacitor design, material and their application. Figure (3.11) shows a simplified equivalent circuit of a practical capacitor.

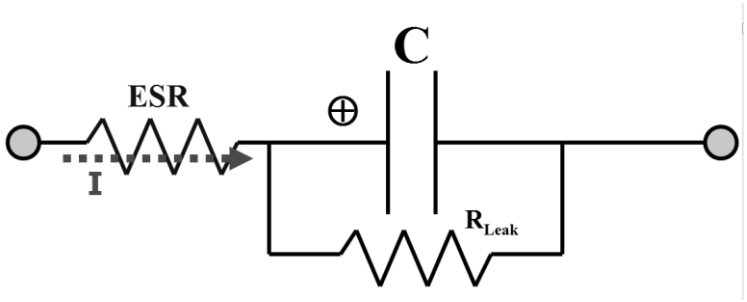


Figure (3.11) The equivalent circuit of a practical capacitor [24].

Where (*ESR*) is the effective series resistance, it is an ac resistance component that appears in series with an ideal capacitor. In the simplified equivalent circuit its value is in the range of few milliohms to several ohms depending on the type of capacitor and operating frequency, R_{Leak} is the dielectric leakage resistance with appears in parallel with the ideal capacitor. An additional component that has not been mentioned in this equivalent circuit is a series effective inductance. This component's effect becomes serious when capacitors are operated at frequencies of several hundreds of KHz and more. For lower frequencies the inductive component effect is negligible. The effective series resistance of a capacitor has an important role in setting an important feature in the operation of a switch mode power converter; it has a big influence on setting the ripple voltage value at the output of the converter as can be seen from equation (12) and figure (3.12):

$$v_r = \Delta I_L * ESR \qquad \text{....(12)}$$

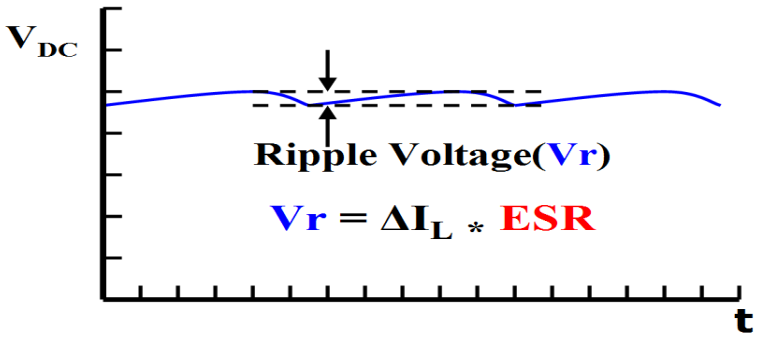


Figure (3.12) The ripple voltage waveform in the output of Switch mode Power converter.

Where (V_r) is the peak to peak output ripple voltage, (ΔI_L) is the inductor ripple current, and (ESR) is the effective series resistance of the series device.

There are several kinds of capacitors that are designed using a wide range of material to suit a specific application. In this discussion only those that can be implemented in designing VRMs for low voltage battery operated equipment will be mentioned. These will include:

- Aluminum Electrolytic capacitors [49,50]; This type comes in two main variations: one with liquid electrolyte, this type is characterized by cheap cost, moderate *ESR* figures, and moderate ripple current ratings. They work at a wide voltage range, but suffer from large size of capacitance ratio, low temperature rating, degraded performance with aging as the electrolyte dries out, thus consequently becomes unable to withstand high temperature application. The other type of aluminum capacitors comes with solid-state electrolyte. It features lower *ESR* values and higher ripple current ratings, longer life, and better stability against aging and temperature but at higher cost and lower voltage rating. A third alternative version of the aluminum capacitor is the hybrid electrolyte type which offers the same *ESR* figures and ripple current ratings of the solid electrolyte type at a much lower cost but still has reduced high temperature endurance and has low voltage rating.

- Tantalum solid electrolytic capacitor [49,52]. This type of capacitors is characterized by higher stability, temperature ratings and lower ESR figures and moderate ripple current ratings compared with the aluminum based counterpart. It comes in two variations: the first produced with manganese dioxide cathode (MnO2), this type is characterized by low *ESR* figures, long-term performance at high temperature but has low voltage ratings, limited tolerance, resulting in combustion hazard upon failure therefore care should be taken to prevent that when implemented in circuit design. The other type of tantalum capacitors is designed with MnO2 cathode replaced by a highly conductive polymer called 'Polypyrrole'. This cathode material has a conductivity figure 100 times greater than that of MnO2 resulting in very low *ESR* figures, high ripple current ratings, and increased safety, as it comes with combustion suppressing construction, in

addition to long term stability, but it comes at a higher cost and again has low voltage rating.

- Niobium solid electrolytic capacitors [49,51]: This type of capacitors uses Niobium instead of Tantalum as anode material. It is one of the alternatives that can be considered as a replacement for the tantalum in capacitor manufacturing as tantalum is becoming increasingly scarce and thus more expensive, yet niobium is more than 100 times more plentiful than tantalum and thus will result in less expensive capacitors that exhibit features very comparable with the tantalum counterpart. Niobium Solid electrolytic capacitors are usually constructed using conductive polymer cathode which gives extra safety feature by providing much higher ignition resistance and reliability compared with tantalum.

- Multi layer ceramic capacitors (*MLCC*) [46,52]: This type of capacitors while has low capacitance value of only up to 100μF, it comes featured with ultra low ESR figures and moderate ripple current ratings and the high tolerance to transients as it is non polarized and has high temperature ratings but it suffers from aging resulting in large effective capacitance loss over time in addition to suffering from piezoelectric effect.

Care should taken when selecting capacitors to suit the requirements of a given application so as to consider all design conditions from capacitance value, operating voltages, operating temperature required *ESR* value, along with the proper derating applied to maintain recommended operational tolerance and safety. Figure (3.13) shows the internal structure of some modern chip capacitors.

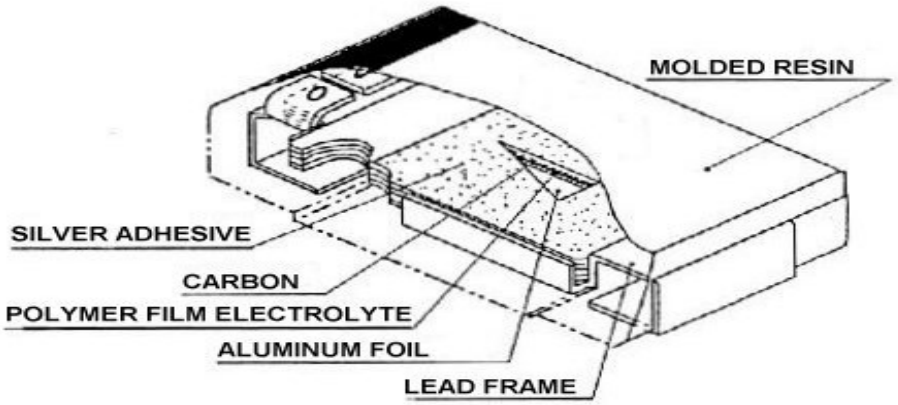


Figure (3.13a) Structure of modern aluminum solid electrolytic chip capacitor[49]

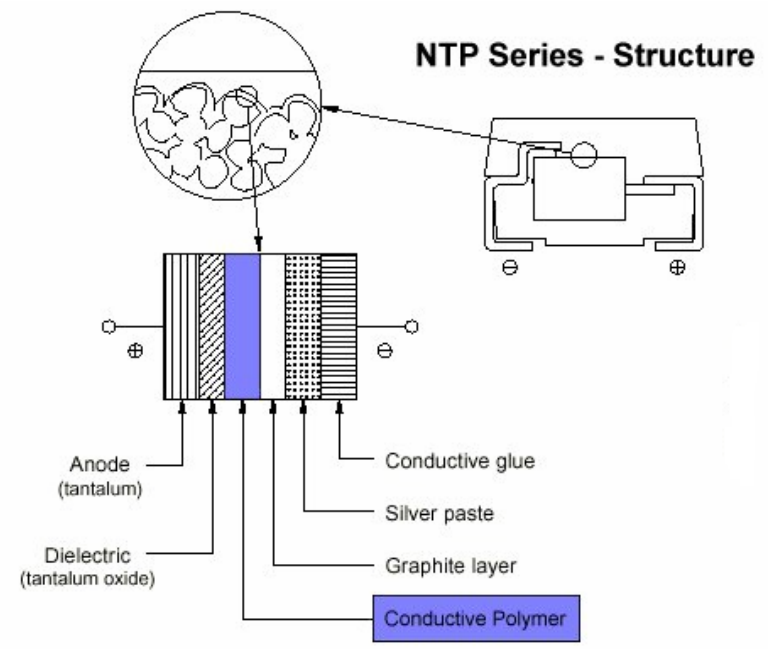


Figure (3.13b) Structure of modern Tantalum solid electrolytic chip capacitor [49]

The curves shown in figure (3.14) indicate that the *ESR* figures relative to operational frequency for the Aluminum solid electrolytic capacitor, indicated by the red curve, is superior in performance compared with the aluminum liquid electrolytic capacitor, indicated by the blue curve [49,50].

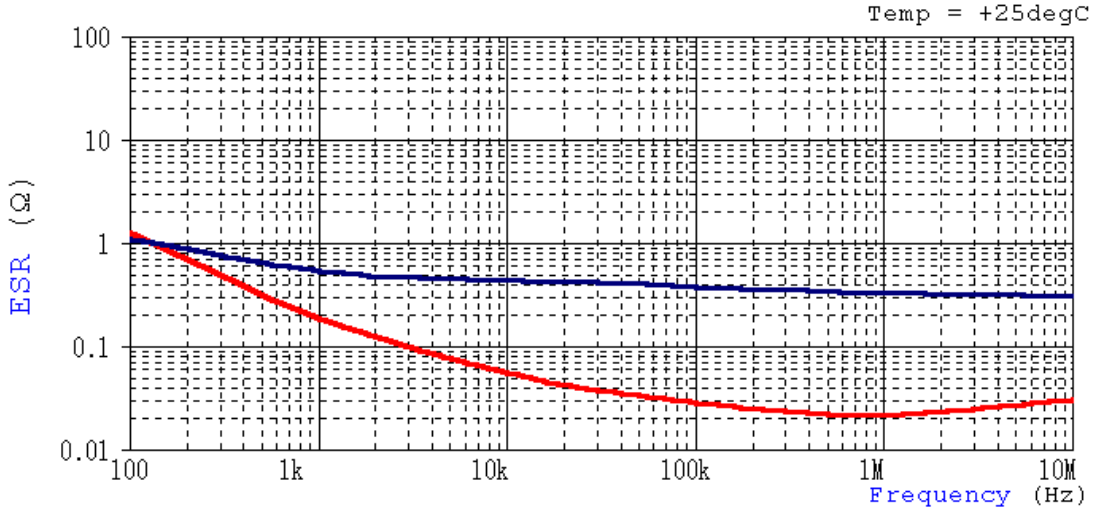


Figure (3.14) ESR figure variation with operating frequency for Aluminum solid electrolytic capacitor (red) and Aluminum liquid electrolytic capacitor (blue).

3.5.3. Theory of Switching Device Selection for High Efficiency PWM Buck Converters

The Switching devices that can be incorporated in the design of power converters are electronic power control devices these can include bipolar transistors, thyristors, power MOSFETs, and IGBT Devices. The suitable device that can suit the intended buck converter design for battery operated low voltage applications as the one this work is targeting are of MOSFET type.

Power MOSFETs are the favored devices for designing modern low voltage power conversion applications because when compared to bipolar transistors, the MOSFET operation does not suffer from minority carrier storage time effect or from secondary breakdown occurring during forward and reverse biasing conditions. In bipolar transistor these secondary breakdowns could lead to a serious uncontrollable conduction condition called *thermal runaway* that results in damaging the device permanently. This occurs because bipolar transistors have negative temperature coefficient resulting in reduced resistance in the hot spot created by the secondary breakdown which will result in further current increase, resulting in augmented temperature rise and the effect becomes regenerative and out of control, thus the term thermal runaway. While MOSFETs have positive temperature coefficient so the hot spots generated by secondary breakdown will lead to increased spot resistance resulting in higher voltage drop that tends to redistribute load current away from the hotspot [53,54].

Power MOSFETs are found in two main types; the lateral MOSFET (also called DMOS) and the trench MOSFET. The trench in this type of power MOSFET comes in shapes like the V-shaped and the U-shaped trench. This categorization is based on the semiconductor substrate structure of the device.

Using either a trench or lateral architecture, there is a distinct relationship between the conduction channel on-resistance ($R_{DS(ON)}$) and gate capacitance charge requirement. This relation is sometimes called Figure of Merit factor (*FOM*). This factor is calculated as shown in equation (13)[55]:

$$FOM = R_{DS(ON)} \cdot Q_G \qquad \text{.....(13)}$$

Where $R_{DS(ON)}$ is the source to drain on resistance of the MOSFET, Q_G is the total gating charge required to turn the MOSFET device on.

So when selecting a transistor for designing a high efficiency VRM it is important to select the device while observing both $R_{DS(ON)}$ and Q_G values and the final decision will be made on the device that satisfies both lower on channel resistance and lower gating charge drive requirements.

It must be noticed that the ratio of $R_{DS(ON)}$ per unit area compared to capacitance per unit area is different for each, and each approach offers distinct advantages. Figure (3.15) shows the structure of both lateral and trench MOSFETs.

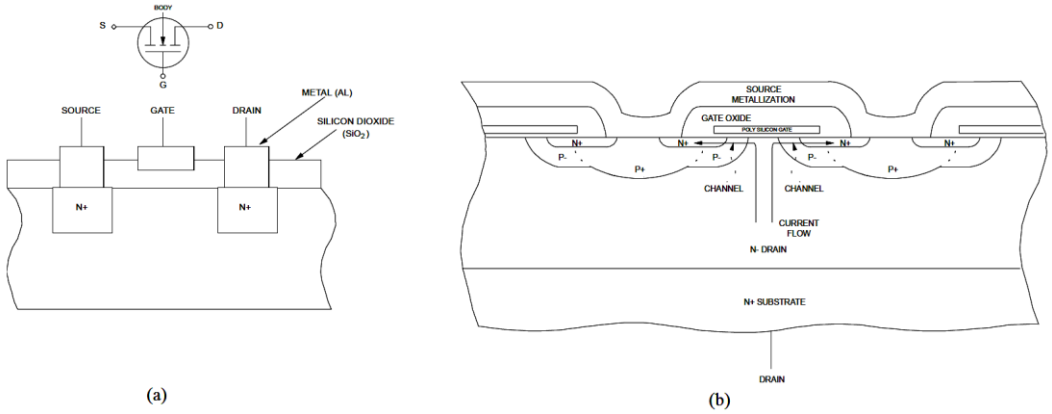


Figure (3.15) Structure of: (a) the lateral MOSFET, (b) the trench MOSFET.

The lateral MOSFET requires lower power requirements for the gate control signal due to smaller gate capacitance, it also exhibits faster switching speeds. These advantages come on the cost of higher $R_{DS(ON)}$ and the only method in this structure to reduce $R_{DS(ON)}$ is to use of wider channels, which tend to require larger silicon area resulting in expensive devices.

Trench MOSFETs exhibit relatively lower $R_{DS(ON)}$ than lateral MOSFET but at the expense of increased drive requirements due to larger gate to channel capacitance. It can be said that switching losses for a given on-resistance in a MOSFET using a lateral architecture can be less than half of those exhibited by a comparable trench MOSFET, allowing them to offset the higher conduction loss that their higher on-resistance generate.

Texas Instruments announced the NexFET power MOS device [56], this advancement is considered the third generation in power MOSFET devices. This new power device architecture promises $R_{DS(ON)}$ figures similar to those offered by the competitive TrenchMOS technology and at the same time offers reduction in input and Miller capacitances, significantly resulting in a product that reduces switching losses in switch mode power supplies, especially those operating below 30V. This device makes it possible to operate the converter at higher switching frequencies resulting in smaller end products. Figure (3.16) shows the architecture of the NexFET device.

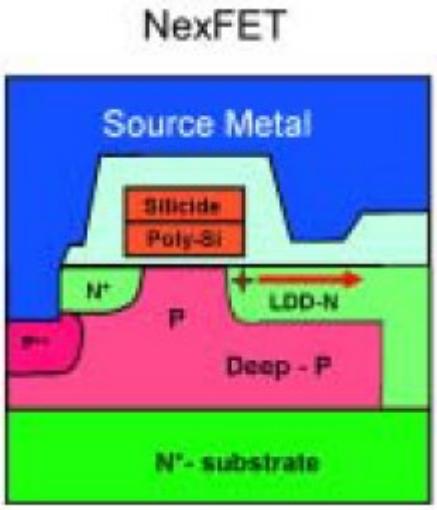


Figure (3.16) the NexFet Device Architecture [56].

Figure (3.17) shows the improvements made in the FOM factor for both TrenchFET and NexFET technology throughout a decade.

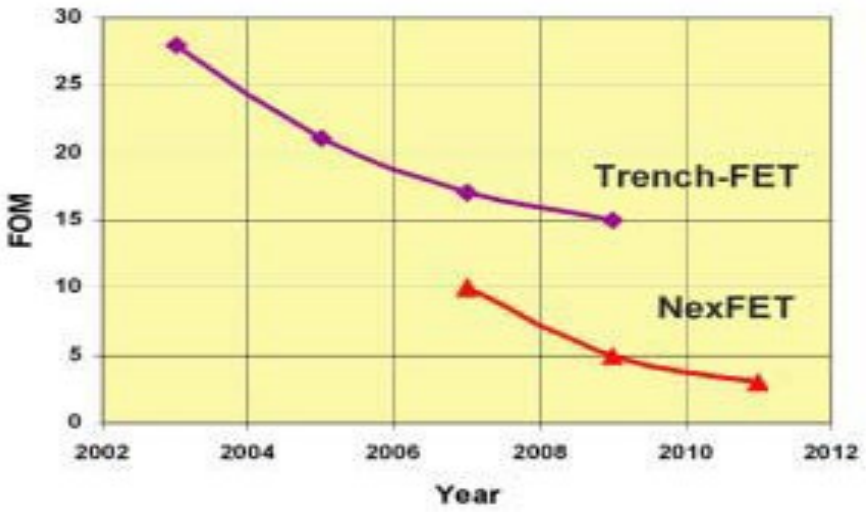


Figure (3.17) Comparison of FOM reduction for TrenchFET and NexFET technologies

The important factors that must be made upon deciding to select a given device is to investigate thoroughly its characteristics and define the FOM factor and then selection decision can be made successfully. Figure (3.18) shows the data sheet of a MOSFET power device and its associated values of $R_{DS(ON)}$ and total gating charge value (Q_G) required to turn on the device is clearly stated in field **7** of the gate charge characteristics table.

Infineon technologies

			IPD04N03LA IPS04N03LA		IPF04N03LA IPU04N03LA	
Parameter	**Symbol**	**Conditions**	**Values**			**Unit**
			min.	**typ.**	**max.**	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz	-	3909	5199	pF
Output capacitance	C_{oss}		-	1488	1979	
Reverse transfer capacitance	C_{rss}		-	174	261	
Turn-on delay time	$t_{d(on)}$	V_{DD}=15 V, V_{GS}=10 V, I_D=25 A, R_G=2.7 Ω	-	14	21	ns
Rise time	t_r		-	11	16	
Turn-off delay time	$t_{d(off)}$		-	44	66	
Fall time	t_f		-	6.6	10	
Gate Charge Characteristics[6)]						
Gate to source charge	Q_{gs}	V_{DD}=15 V, I_D=25 A, V_{GS}=0 to 5 V	-	12	16	nC
Gate charge at threshold	$Q_{g(th)}$		-	6.3	8.3	
Gate to drain charge	Q_{gd}		-	8.1	12	
Switching charge	Q_{sw}		-	14	19	
Gate charge total	Q_g		-	31	41	
Gate plateau voltage	$V_{plateau}$		-	3.0	-	V
Gate charge total, sync. FET	$Q_{g(sync)}$	V_{DS}=0.1 V, V_{GS}=0 to 5 V	-	28	37	nC
Output charge	Q_{oss}	V_{DD}=15 V, V_{GS}=0 V	-	32	43	
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	25	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=80 µA	1.2	1.6	2	
Zero gate voltage drain current	I_{DSS}	V_{DS}=25 V, V_{GS}=0 V, T_j=25 °C	-	0.1	1	µA
		V_{DS}=25 V, V_{GS}=0 V, T_j=125 °C	-	10	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	10	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=4.5 V, I_D=50 A	-	4.8	5.9	mΩ
		V_{GS}=4.5 V, I_D=50 A, SMD version	-	4.6	5.7	
		V_{GS}=10 V, I_D=50 A	-	3.4	4.0	
		V_{GS}=10 V, I_D=50 A, SMD version	-	3.2	3.8	
Gate resistance	R_G		-	1.3	-	Ω
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=50 A	48	96	-	S

Figure (3.18) A typical data sheet table to estimate FOM for a power MOSFET device[55].

From comparing several devices offered by several semiconductor manufacturing firms the devices that will yield the most efficient design within reasonable cost factor will be selected for implementation in the design that will deliver the desired performance.

3.6. Energy Source powering mobile Applications

Most of the mobile systems rely on storage batteries to power mobile computing devices. A storage battery is a chemical reaction cell, the cell reaction is divided into two electrode reactions, one that releases electrons which is the negative side of the battery and the other one that absorbs electrons which is the positive side of the battery. This flow of electrons forms the current that can be drawn from the battery to supply the energy required to operate a given device. The energy absorbed by the device connected to the storage cell terminals is created by the chemical cell reaction which is directly converted into an electric current. This chemical reaction is called an electrochemical reaction and the cell is called an electrochemical cell.

Basically an electrochemical cell consists of positive and negative electrodes that are immersed in an electrolytic solution. The reacting substance is usually stored inside the electrodes, and on certain cell designs the electrolytic solution may contain the reacting substance if it has any participation in the electrochemical reaction. When the storage cell is being discharged, the negative electrode contains the oxidized substance that releases electrons during the electrochemical reaction, while the positive electrode contains the oxidizing substance that will receive the electrons from the oxidized electrode through the electrical load connecting the two electrodes. This direct conversion of energy from chemical to electrical except for the losses that are in the form of heat generation has the advantage of high efficiency. Electrical energy can be generated directly inside batteries and fuel cells, while other in direct conversion system rely on chemical reaction that involves oxidizing as well but the product would mostly be in the form of heat that is a gain converted into electrical energy by further processing [57].

There are several kinds of storage cells each of them are characterized by the following parameters:

1- Voltage: Under no-load condition this voltage is called ‘Open Cell Voltage (*OCV*)”. In some batteries it can be indicative of battery charge status as the case

with the lead-acid battery. The cell voltage under load conditions is called "Closed Circuit Voltage (*CCV*)". Another term for cell voltage is the nominal cell voltage, it is a value that approximates the voltage of the system for its characterization.

2- Capacity: Cell capacity is defined as the electrical charge units of Ampere.Hour (Ah) that can be drained from the cell. If the cell is being discharged with a constant current, its capacity can be given as in equation (14) [57].

$$C_{Ah} = \int_0^t I(t) \cdot dt \quad \text{"Ah"} \qquad \text{……..(14)}$$

Other than design, the discharge parameters that influence the cell capacity are: the discharge current, the end of discharge voltage (EOD), and temperature. These parameters determine the depth of discharge (DOD) of a cell and it greatly influences cell service life. So the discharge current is specified by cell manufacturer at room temperature and is usually referred to in terms of capacity as C_{20}, C_{10}, C_5. Accordingly I_{20},I_{10}, I_5 means the current that results in 20, 10 ,5 hours duration to discharge the cell.

3- Energy Content: it is the Watt.Hour (Wh) that can be drawn from the cell and is given in the equation (15)[57]:

$$E = \int_0^t U(t) \cdot I(t) \cdot dt \quad \text{Wh} \qquad \text{……..(15)}$$

Where *E* is the energy in Wh, *U* is the average cell voltage in volts, *I* is the discharge current in amperes, and t is the discharge period in hours.

4- Specific Energy and Energy density: it is the ratio of cell energy content to either its weight or volume. The weight based energy density is given in Wh/Kg units and as an example the lead-acid cell has 25Wh/Kg specific energy density and a modern lithium-ion battery has 125Wh/Kg energy density. The volume based energy density is given in Wh/cm^3 units and is more favored by mobile equipment designers as this figure has more priority in the design than the weight.

5- Internal resistance: it is the ohmic resistance within the electrodes and the electrolyte as well as the over voltage at the boundaries between electrodes and

the electrolyte. It can be measured by taking the terminal voltage of the cell at two different loads the internal resistance of the cell can be measured using formula (15)[57];

$$R_i = \frac{U_1 - U_2}{I_2 - I_1} = \frac{\Delta U}{\Delta I} \qquad \text{.....(16)}$$

Where R_i is the internal resistance of the storage cell, U_1, U_2 are the measured loaded cell voltage at two different loads and I_1, I_2 are the current measure at the different loads respectively. It is favored for this figure to be as small as possible so that the whole energy content of the battery can be utilized effectively. It is usual for internal resistance of the cell to increase towards discharge because of reduced conductivity of the formed compound.

6- Self Discharge: It is the gradual loss of charge in the cell when it is idle at open circuit conditions. One of the reasons behind it is the gradual reduction of the oxidation state in the positive electrode. Secondary electro-chemical reactions can also contribute to self discharge conditions along with several other factors. It is given as a loss of energy content per year for primary cell and per month for secondary cells. It can range from 0.5% to 20% per year in commercially available cells, where the former is for modern high quality lithium based primary cells. As for secondary cells the self discharge figure can be between 2% to 20% per month depending on cell structure, content, and age. The mode lithium-ion cell can have a self discharge figure of 5% to 10% per month.

The lithium-ion and lithium-polymer cells are of prime importance for this work as they are the industry standard for mobile applications thus it is important to observe the behavior of these cells during their service period starting from fully charged state to the point where the cell is considered discharged.

The manufacturer's nominal cell voltage of a lithium-ion and lithium-polymer cell is 3.7 volts. It can reach 4.2 volts figure when fully charged and falls to about 3.4 volts when nearly discharged. Figure (3.19) shows the lithium–ion cell voltage change during charging from 0% to 100% [58].

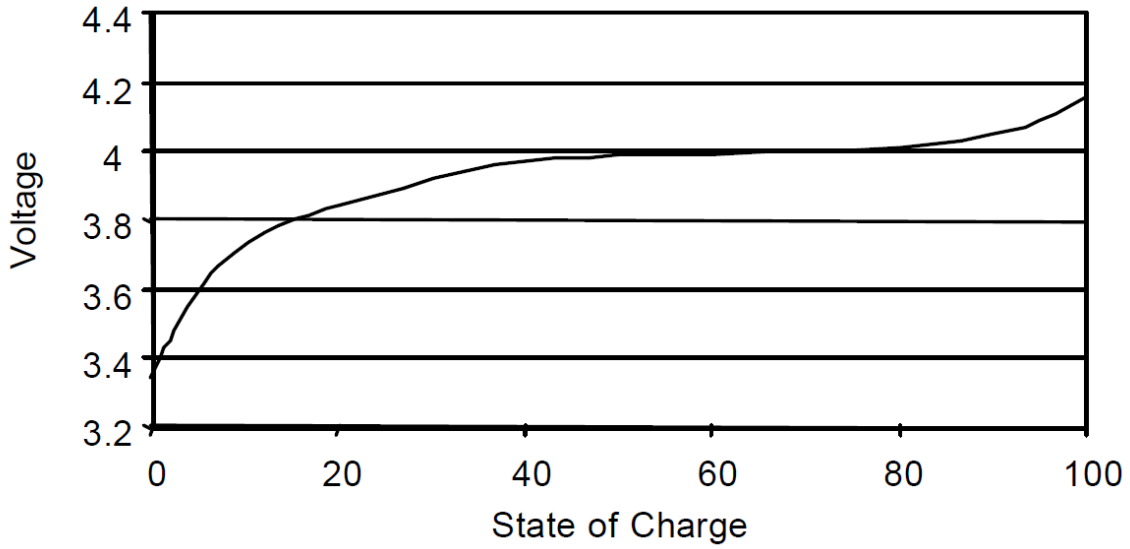


Figure (3.19) Lithium-Ion Cell nominal voltage variation during charging [58]

These figures will be of prime importance during the phase of designing the control system for the energy efficient smart VRM. The controller must keep track of the battery cell voltage and adapt its operational parameters accordingly in order to realize the best possible conversion efficiency throughout the energy content of the power source cell.

3.7. Chapter Summary

In this chapter, the concept of DVS has been discussed in addition to detailed investigation in the target processor (the Intel PXA 270) power requirements, operating modes and DVS system requirements has been covered. Along with this, a brief investigation in the buck converter passive and active component selection for high efficiency operation is done as well as a description of energy source that powers the mobile computing devices namely the lithium-ion and the lithium-polymer battery cell.

Chapter Four

Power Converters for Energy Efficient Voltage Regulating Module Design

4.1. Introduction

The main goal of this chapter is to describe approaches in power converters design that enable realizing high efficiency operation of mobile computing system that will lead to longer operation periods and more environmental friendly products.

Electronic circuits, whether digital or analogue, require electrical power to be delivered to them to operate. Each circuit is designed to work on a specific power requirement that in general is not compatible with power source specifications. In this case a power converter is required to modify source specification to suit load specifications. In this work the selection of the voltage regulating method will be made on the basis of maintaining high conversion efficiency throughout a wide range of operating currents and voltages.

The source of power in case of mobile computing devices is normally a storage cell. Modern devices obtain their power from a Lithium-ion or Lithium-polymer battery. The nominal voltage of these cells as set by cell manufacturers is 3.7volts. The target of the VRM design is the core of Intel PXA270 microprocessor. The core voltage required for this processor ranges from 1.55 volt to 0.85 volt. The choice of power supply design must include voltage regulating circuits that will step down source voltage (the battery) to the level required to operate the core of the target processor. The next section will cover an investigation about voltage regulating methods and circuits.

4.2. Voltage Regulating Methods and Circuits

The requirement of the work under hand is to convert DC voltage coming from source to a lower level suitable for the target load. So the required function is DC-DC conversion. The load voltage is required to be stable, hence the kind of circuits that are suitable must include regulation function. There are several approaches and techniques to achieve this goal. Figure (4.1) shows the kinds of available power supply voltage regulation technologies [21].

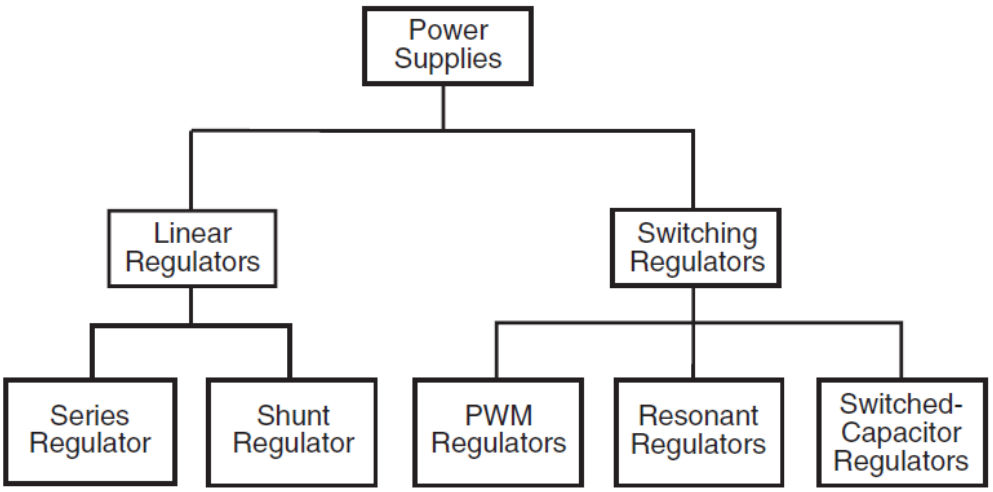


Figure (4.1) Power supply regulation techniques [21]

The most common types of voltage regulators are the linear regulators and the switch-mode regulators. Linear regulators can be found in two basic topologies, the series voltage regulating, and the shunt voltage regulating devices. The switch mode regulators come in three variations, the PWM DC-DC converter, the Resonant DC-DC converter, and the switched capacitor converter which are also called charge-pump converters or regulators [60].

In linear voltage regulators, transistors are operated in the active region and they dissipate energy as the difference in voltage between load and source is dropped on the pass transistor. With relatively high voltage drops at high currents, large amount of power would be dissipated in the pass transistor leading to reduced power efficiency. For high current applications the large heat sinking requirements make linear regulators heavy and bulky, but beside these disadvantages, linear regulators are characterized by low noise

levels which makes them suitable for audio and other application requiring low noise power sources.

In switching-mode converters, transistors are operated as switches, so most of the operational time the devices will be in the saturation or cutoff region making them dissipate much less power than transistors operated as dependent current sources. When the transistor is switched on, the voltage drop across it becomes very low so, even when high current is passed through, the power dissipated remains low as it operates in the saturation region, and when it is switched off, the transistors conduct a nearly zero current while the voltage drop across them is high because they operate in the cut off region. For this reason the conduction losses are low and the efficiency of switching-mode converters is high, and in some applications it could reach 80% to 90% figures and some cases even more. However, switching losses reduce the efficiency at high operating frequencies as these losses increase proportionally to switching frequency.

Linear and switched capacitor regulator circuits are used in low-power and low-voltage applications, but in low power application field they are sometimes favored over linear regulators as they exhibit higher efficiency.

PWM converters and resonant regulators are used at high power and suitable for a wide range of voltage levels applications. They are small in size, light in weight, and have high conversion efficiency.

In general, the DC-DC converters main function is to convert input voltage to the desired output voltage level within the tolerance specified by the load requirements. It is required to regulate output voltage against variations in input voltage and load currents. It should respond fast enough to keep load voltage at desired level when subjected to fast variations load or source conditions within given operational limits. The ripple in the output of the converter should be low and conforms to load requirements. In addition to that, the converter should be designed so that the emitted Electromagnetic Interference (EMI) from its operation should be below the levels specified by EMI standards [21.59].

Linear regulators and switch mode regulators come in a variety of circuits, functions and operational features. Figure (4.2) includes several basic circuitries for linear regulators while figure (4.3) shows the basic circuitries for some switch-mode regulators [21,59].

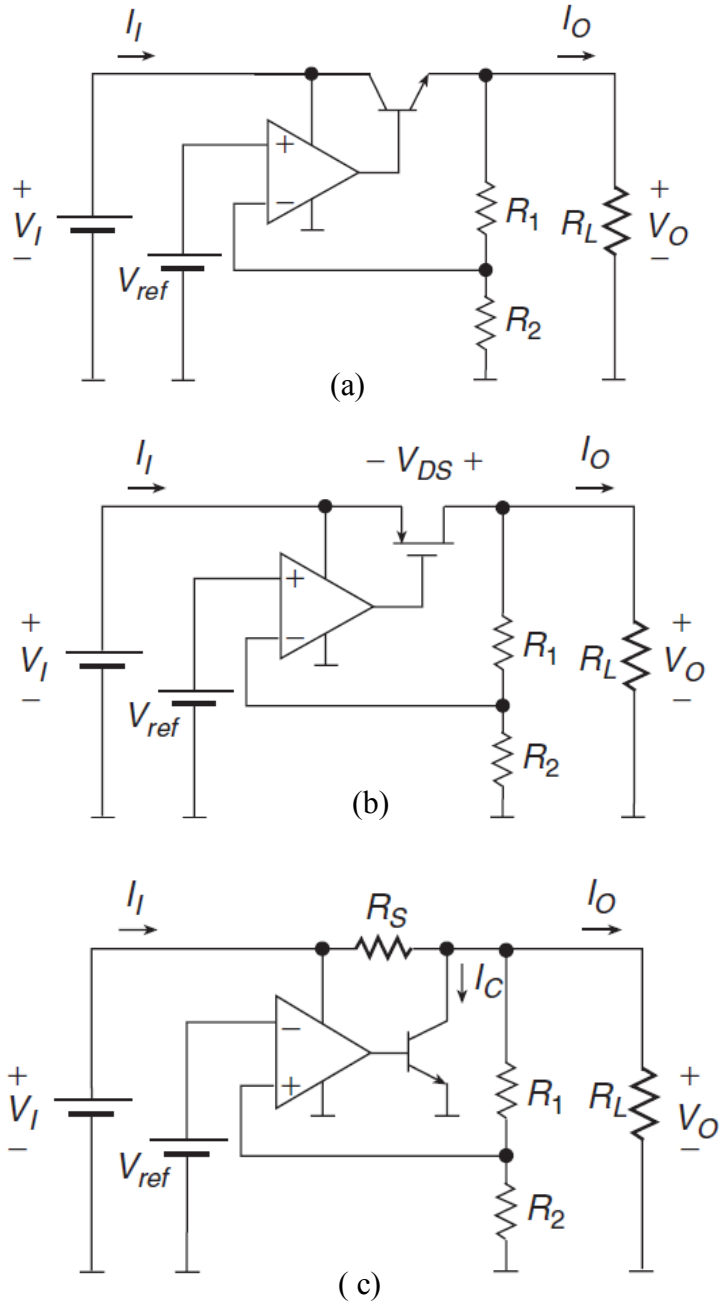


Figure (4.2) Basic circuits of linear regulators, a: linear series regulator, b: linear low drop out (LDO) regulator, c: linear shunt regulator [21].

The linear series regulator that uses a PNP bipolar transistor or n-channel MOSFET device as a series pass element is called low drop out (LDO) regulator and it has a unique feature over other types that use bipolar transistor as a passing element in that it can provide regulation function even if the difference between input and output voltage drops

to 0.1 volts whereas standard series regulator seizes to function when the voltage difference between input and output is less than 2 volts.

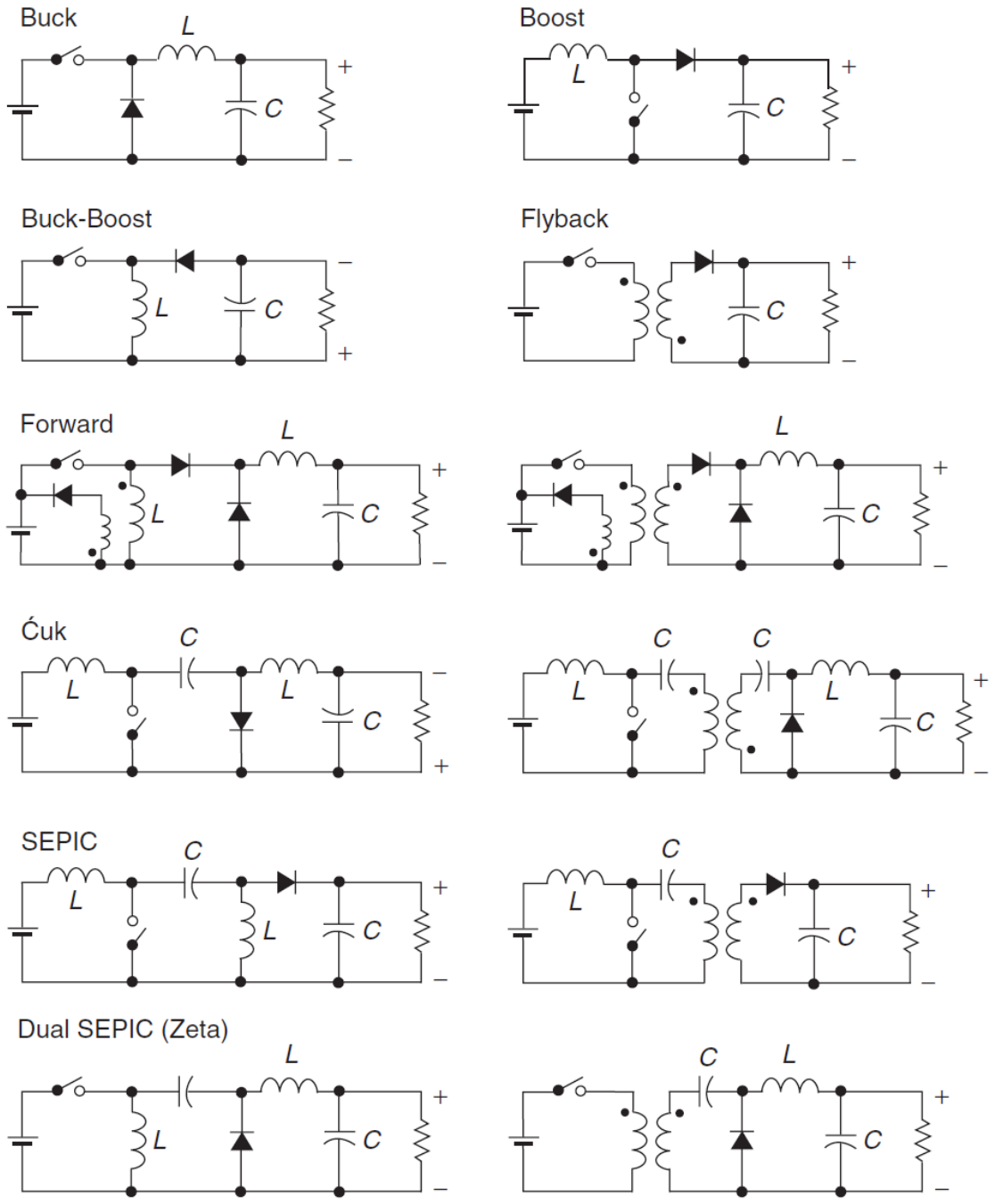


Figure (4.3) Basic circuits for non isolated and isolated PWM converters [21]

The PWM converter serves several requirements and can deliver any relation between input voltage and output voltage, the buck converter delivers output voltages that are smaller that input voltage while the boost converter provides output voltages greater than input voltage, the buck-boost converter delivers a voltage to load that is in opposite

polarity to that of its input. The rest can provide features that are a mix between buck and boost which are useful in certain applications where the input supply fluctuates greatly. In addition to that, the isolated versions can provide electrical isolation between input source and the load to which the output voltage of the regulator is delivered.

4.3. Features of a DC-DC Converter Circuit

Any DC-DC regulator whether it is a linear regulator or a PWM converter circuit, will have special features that defines its operational characteristics. These can be categorised into static characteristics and dynamic characteristics.

4.3.1. Static Characteristics of a DC-DC Voltage Regulating Circuit

There are several parameters that define the static characteristics of a DC-DC converter, the most important are the line regulation (*LNR*), and the load regulation (*LOR*).

The line regulation defines the change in output voltage (V_O) in millivolts to a change in input voltage (V_I) in volts when the load is held constant and ambient temperature is steady during test. Its unit is given by millivolts per volts (mV/V) as given in equation (17).

$$LNR = \left(\frac{\Delta V_O}{\Delta V_I}\right)\Bigg|_{I_O=Constant,T_A=Constant} \left(\frac{mV}{V}\right) \qquad \ldots\ldots(17)$$

Where ΔV_O is the change in output voltage, and ΔV_I is the change in output voltage. Figure (4.4) shows the graphical representation of the line regulation [59].

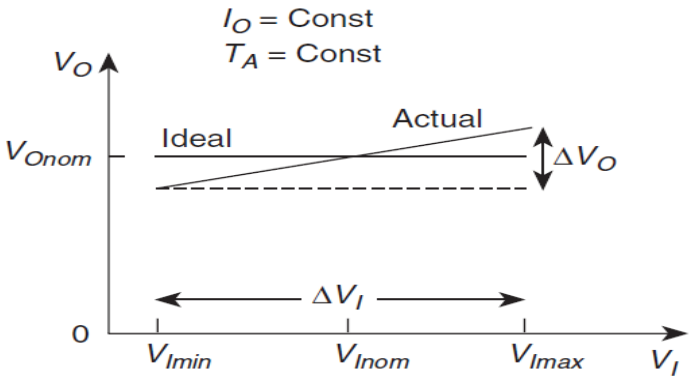


Figure (4.4) Illustration of the line regulation [59]

The load regulation is an indication of the ability of a regulator to keep output voltage steady while load current is being increased slowly from 0 to $I_{O(Max)}$ when input voltage is kept constant and ambient temperature is steady as shown in equation (18).

$$LOR = \left(\frac{\Delta V_O}{\Delta I_O} \right) \Bigg|_{V_I = Constant, T_A = Constant} \left(\frac{mV}{A} \right) \qquad \text{.....(18)}$$

Figure (4.5) shows graphically how the change in load affects the regulation of a converter [59].

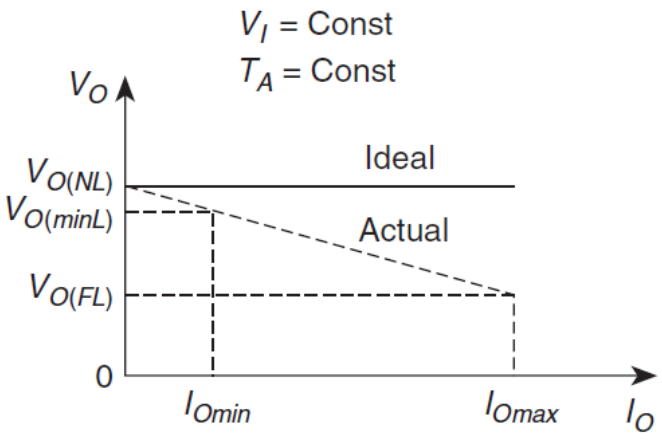


Figure (4.5) Load regulation effect on output voltage of a converter circuit [59].

4.3.2. Dynamic Characteristics of a DC-DC Voltage Regulating Circuit

The transient response of a voltage regulating circuit to load changes and supply changes defines the dynamic characteristics of the voltage regulating module. These are defined as the line transient response and the load transient response.

The line transient response is described as the changes in output voltage of the regulating circuit in response to a step change in input voltage while the load is kept constant.

The load transient response is given as the change in output voltage of the voltage regulator to a step change in load current while holding input voltage to regulator

constant. Figure (4.6) illustrates the line and load transient response for a given voltage regulating circuit.

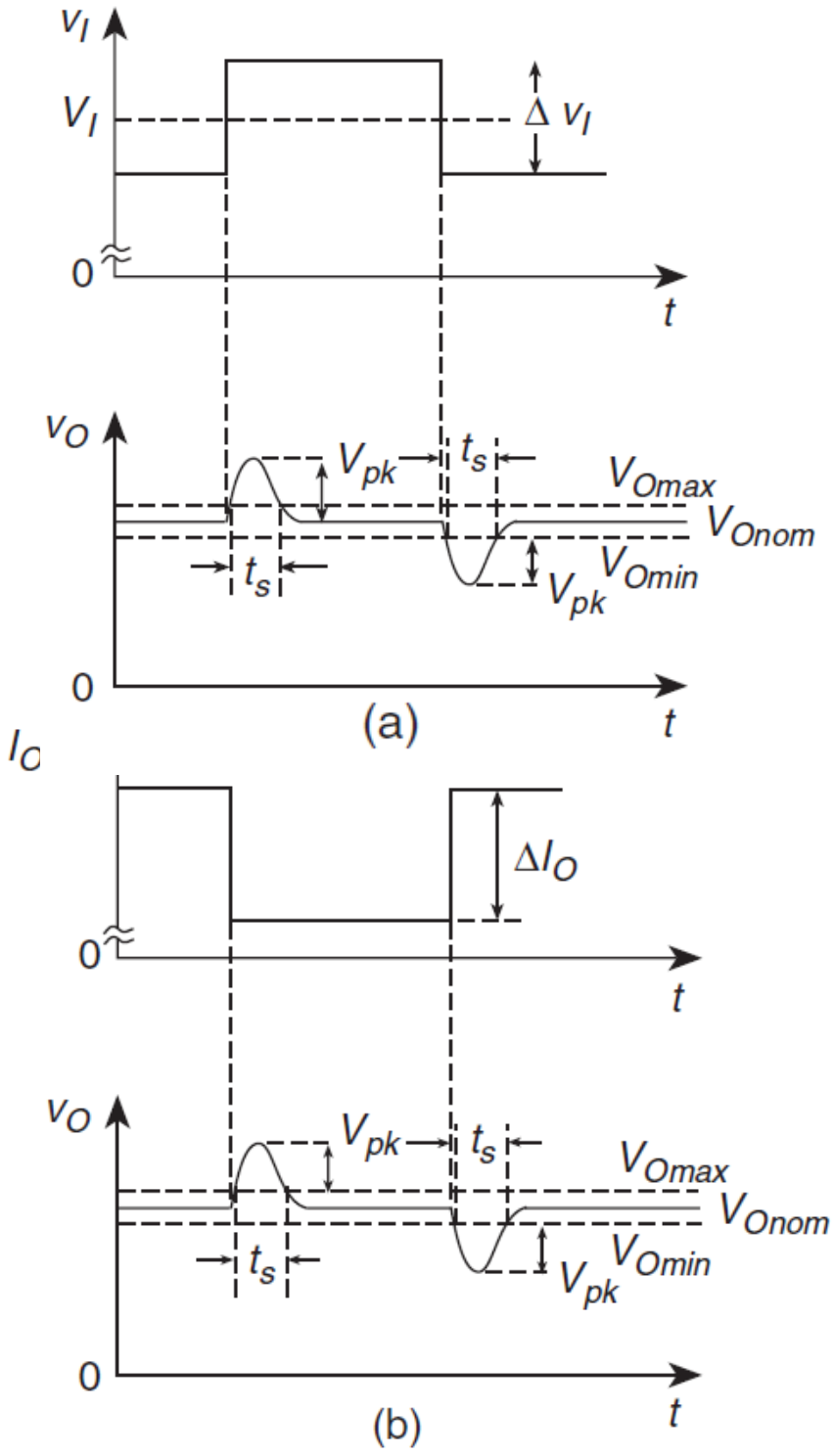


Figure (4.6) The dynamic characteristics measure for a voltage regulating circuit, a: measuring the line transient response, b: measuring the load transient response [21].

The peak overshoot voltage (V_{pk}) in the transient response of both cases should be lower that given the load supply specifications. The settling time (t_s) is the other important factor of the transient response and should conform to load requirements and as a rule these two parameters are preferred to be as small as possible.

The circuit topology of the regulating module that is going to be used in the design of the smart voltage regulator is the buck topology as it is the one suitable for implementation in the design of the regulator that will supply the core of the Intel PXA 270 Processor. The input voltage will be supplied by a lithium-ion cell with nominal voltage of 3.7 volts and the supply voltage to the core is required to be for 0.85 volts to 1.55 volts. The buck converter circuit topology provides the step down function needed.

4.4. The Buck PWM DC-DC Converter

The basic buck converter shown in figure (4.7a) consists of four components the switching device (S_1) that receives the PWM control signal, a diode (D_1) or a synchronous rectifier (S_2), an inductor (L), and a filter capacitor (C). The load is represented by a resistive value named (R_L).

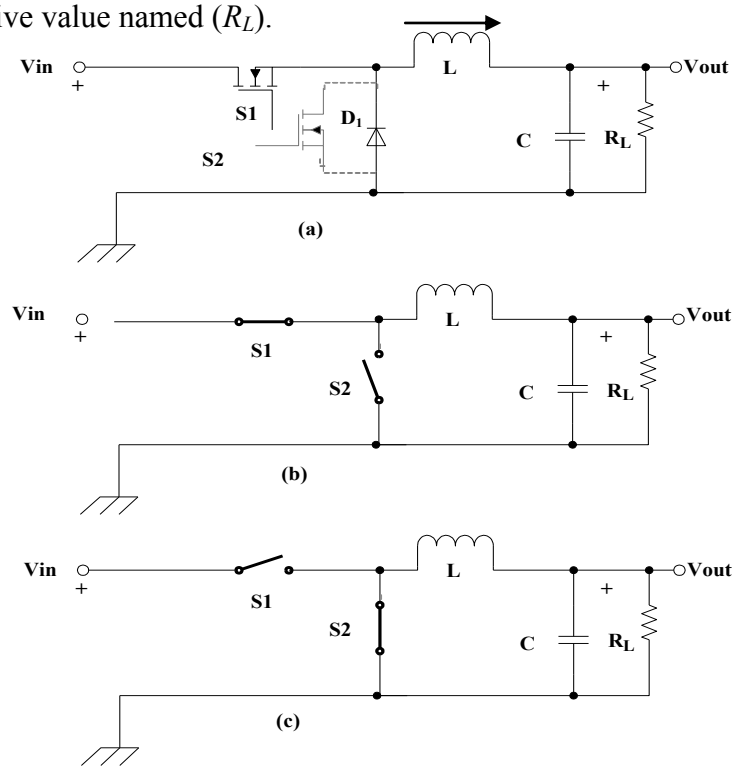


Figure (4.7) The basic buck converter showing in (a) circuit elements, (b) *S1* device is on and *S2* device is off, (c) *S1* device is off and *S2* device is on.

The switching devices that are most commonly used in modern buck converter design for low voltage application are MOSFETs. S_1 is the PWM controlled switch and S_2 is either a diode or a synchronous rectifier. As shown in figure (4.7b) and (4.7c) when the converter starts operating the PWM switching device and the diode or the synchronous rectifier are turned on and off alternately at a switching frequency (f_S) for an interval (D) known as the duty cycle. This duty cycle is defined in equation (19) [59]:

$$D = \frac{t_{ON}}{T} = \frac{t_{ON}}{t_{ON} + t_{OFF}} = f_S \cdot t_{ON} \qquad \text{……..(19)}$$

Where t_{ON} is the time interval when S_1 is closed and S_2 is open while t_{OFF} is the time interval when S_1 is open and S_2 is closed. If ideal conditions are assumed, and there are no losses in the components of the converter, then the relation between output voltage and input voltage can be written as:

$$V_O = D \cdot V_I \qquad \text{…..(20)}$$

Where V_O is the output voltage of the converter, V_I is the input voltage to the converter.

The duty cycle can be varied and along with it the other waveforms change accordingly. This action provides the means to control the output voltage of the converter to stabilize it against changes in input voltage and load current requirements. It can be mentioned that while in theory D can be varied from 0 to 1, but in practice this is not possible and the change in D is limited from 0.05 to 0.95 so the output voltage in the buck converter is therefore always less than the input voltage.

According to current waveform flowing through the converter's inductor L, the buck converter can operate in a Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM). In CCM the inductor current flows during the whole switching cycle, while in DCM inductor current flows only during part of the switching cycle and it falls to zero and remains at this value for a certain period then starts increasing again with the start of the next cycle. The operation of the converter near CCM and DCM boundary is called the critical mode [59]. There are many distinctive operational features between CCM and DCM operation of the converter that will influence the design criterion and component selection to suit a given application.

In CCM there are two distinct intervals, the first is when the PWM switch S_1 is on and the diode shown in ideal case by S_2, is off as shown in figure (4.7b), the second interval shown in figure (4.7c) where S_1 is off and S_2 is on.

The principle of operation for the buck converter in CCM can be explained by the idealized current and voltage waveforms shown in figure (4.8). At time $t = 0$, the PWM switch is turned on by the voltage control circuits, this results in a voltage across the diode at a value ($v_D = -V_I$). This voltage causes the diode to become reverse biased. The voltage across the inductor L is given by ($v_L = V_I - V_O$) which results in a linear increase in inductor current with a slope of $\{(V_I - V_O)/L\}$. The inductor current i_L flows through the PWM switch. Thus the PWM switch current (i_S) is equal to inductor current (i_L). During this time interval, the energy is transferred from the dc input voltage source V_I to the inductor L, capacitor C, and load R_L. At time $t = DT$, after this period the PWM switching device is turned off by the control circuit.

The inductor has a nonzero current when the PWM switching device is turned off. Since the inductor current waveform is a continuous function of time, the inductor current continues to flow in the same direction after the PWM switching device is turns off. For this reason, the inductor L acts as a current source that will force the diode (D) to turn on. The voltage across the PWM switching device is equal to input voltage V_I and the voltage across the inductor is $-V_O$. Therefore, the inductor current starts decreasing linearly with a slope of $-V_O/L$. During this time interval, the input voltage V_I is disconnected from the circuit and does not deliver any energy to the load and the LC circuit. The inductor L and capacitor C form an energy reservoir that maintains the load voltage and current when the PWM switching device is off. At time $t = T$, the PWM switching device is turned on again and the inductor current starts increasing and energy flow to the circuit increases along with it.

The PWM switching device S_1 and the diode D_1 work as a chopper to convert the dc input voltage V_I into a square wave at the input of the L–C –R_L circuit. The L–C –R_L circuit functions as a second-order low-pass filter that converts the square wave into a low-ripple dc output voltage. Since the average voltage across the inductor L is zero for steady state, the average output voltage V_O is equal to the average voltage of the square wave generated by the chopping circuit.

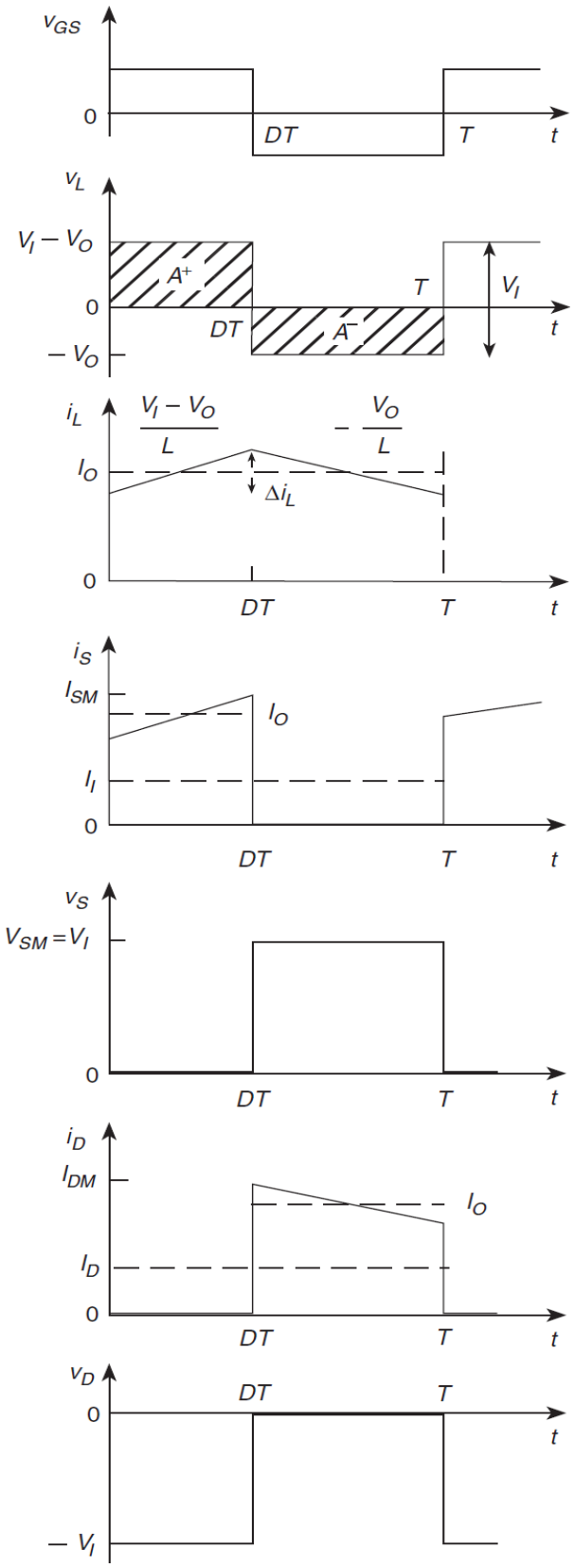


Figure (4.8) The ideal voltage and current waveforms in PWM buck converter operating in CCM [21].

The width of the square wave is equal to the on-time of the PWM switching device S_1 which can be controlled by varying the duty cycle D of the PWM switch drive signal. Thus, the square wave is a PWM voltage waveform. The average value of the PWM voltage waveform is V_O will depend on the duty cycle D and is almost independent of the load for CCM operation as show in equation (20). In practice, the dc input voltage V_I varies over a specified range while the output voltage V_O should be held constant as much as possible. If the dc voltage V_I increases, the duty cycle D must be reduced so that the product DV_I, which is the average value of the PWM voltage, remains constant. On the other hand, if the input voltage, V_I decreases, the duty cycle D should be increased in order to maintain the average value of the PWM signal constant. So, the amount of energy delivered from the input voltage source V_I to the load can be governed by manipulating the switch on-duty cycle D. If the output voltage V_O and the load resistance R_L are constant, the output power is also constant. When the input voltage V_I increases, the switch on-time is decreased so as to transfer the same amount of energy to the load.

The inductor current contains an ac component called inductor ripple current which is independent of the dc load current in CCM and a dc component which is equal to the dc load current I_O. This dc output current I_O flows through the inductor L, thus it biases the magnetic core of the inductor L resulting in only one-half of the B–H curve of the inductor ferrite core being exploited. For this reason, the inductor L should be designed to handle operating currents without causing the core to saturate. To avoid core saturation, a core with an air gap and a sufficiently large volume must be selected.

When operating the buck converter in DCM, inductor current reaches zero value resulting in three distinct operational intervals that can be shown in idealized equivalent circuit shown in figure (4.9). The first circuit is obtained during the first interval when the PWM switch S_1 is on and the diode shown in ideal case by S_2 is off as shown in figure (4.9a), the second interval shown in figure (4.9b) where S_1 is off and S_2 is on, and the third interval is shown in figure (4.9c) where both S_1 and S_2 are open [21,59].

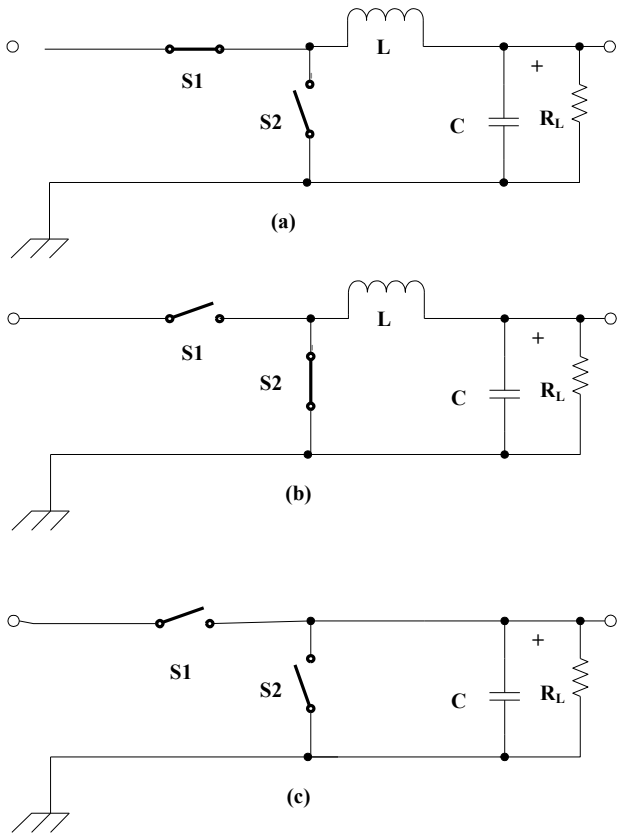


Figure (4.9) The exploitation of the magnetic material of the inductor during CCM and DCM operation of a PWM converter.

With the aid of figure (4.10), which shows the idealized voltage and current waveform in a PWM buck converter operating in DCM, three distinct operation regions can be characterized. At time *t*=0 the PWM switching device is turned on, the inductor current is zero. Afterwards it starts rising linearly from zero, *S2* is off and the voltage across the inductor is equal to (V_I-V_O) for the period $0 < t \le DT$. After this period the PWM switching device S_1 is turned off at $t = DT$, the diode D_1 becomes forward biased and can be described as being turned on. This case is shown in figure (4.9b). So, for the time interval $DT < t \le (D + D_1) \cdot T$, the current passing through the inductor L starts decreasing linearly until it reaches zero value. At this point where $t = (D + D_1) \cdot T$, the diode seizes to conduct. For the period where $(D + D_1) \cdot T < t \le T$, inductor current remains at zero value. When the cycle completes after time T the PWM switching device becomes turned on and the cycle repeats.

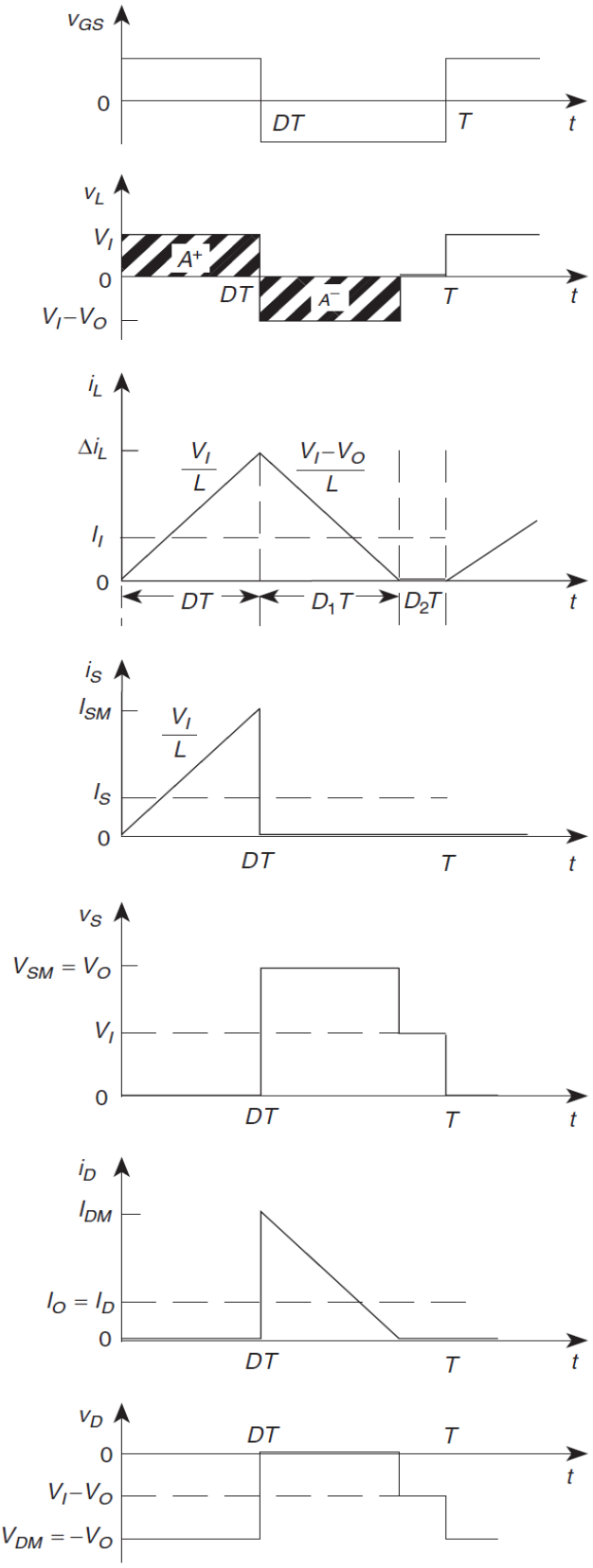


Figure (4.10) The idealized voltage and current waveform in a PWM buck converter operating in DCM [21].

It must be noted that in DCM the relation between output voltage V_O , duty cycle *D*, and input voltage V_I is not linear and the minor B-H hysteresis loop of the inductor is larger than the one seen in CCM operation as shown in figure (4.11) [47].

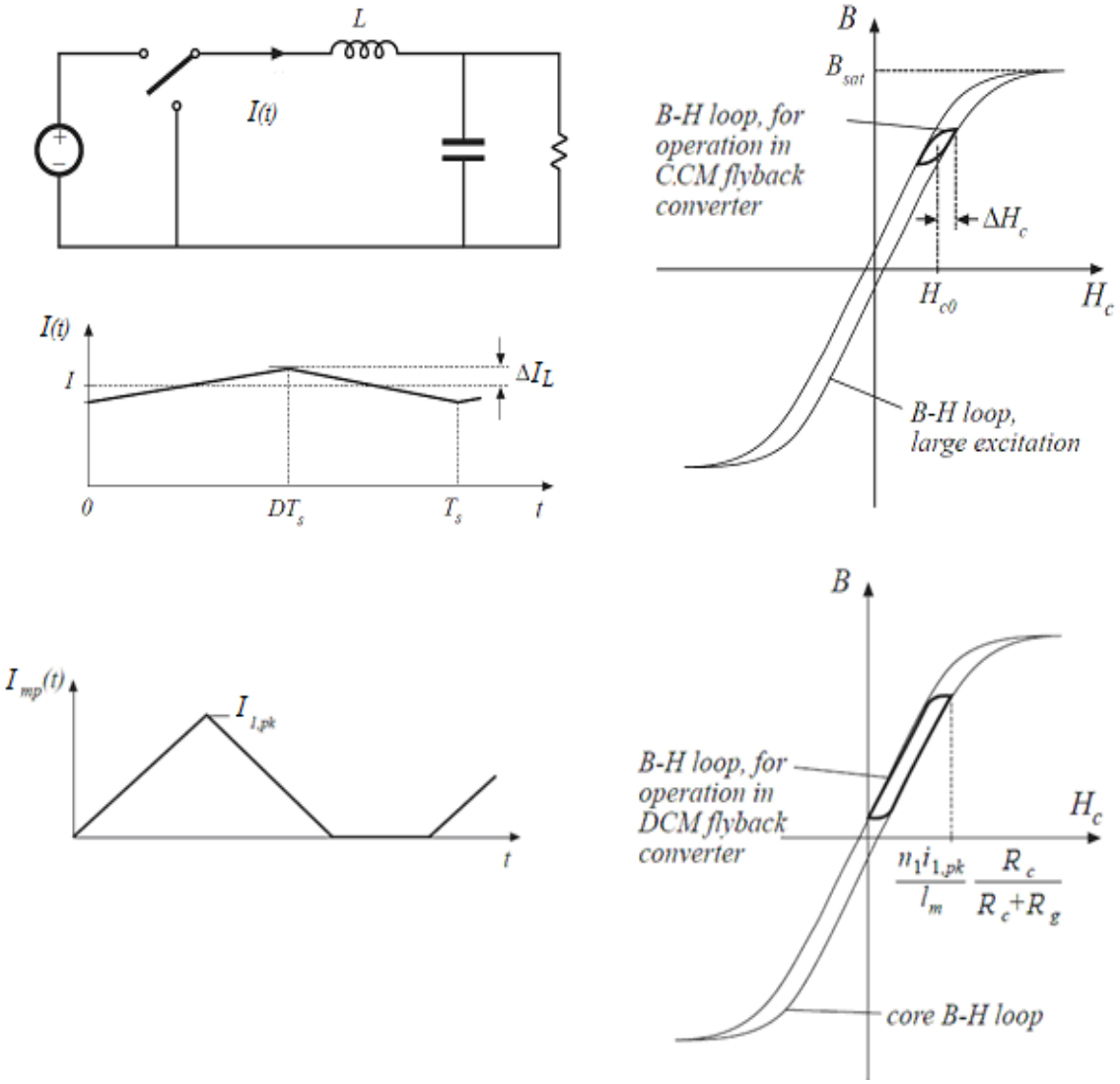


Figure (4.11) The minor B–H hysteresis loop generated in CCM and DCM operation of the buck converter [47]

So it can be noticed that ripple current values and magnetic hysteresis losses are larger in DCM operation of a given buck converter than those observed while operating the buck converter in CCM.

4.5. Selecting the Proper Values for L and C for a Buck Converter Operating in CCM

The inductor L and the capacitor C in a buck converter can be thought of as being the elements of a filter that receives the square wave generated by the chopping action on the input supply voltage and filters the square wave harmonics to produce a constant DC voltage at its output.

4.5.1. Selecting the Proper Value for the Inductor

The type of magnetic core and wire that suits a given application has been covered in chapter 3, now it is required to select the value of the inductor suitable for a given load condition, input supply, required output voltage and converter operating frequency.

On observing the third waveform in figure (4.8), it can be seen that it represents the inductor current I_L versus time when the converter is operated in CCM. It is noticeable that this current is not constant but varies around the output current value I_O between a maximum and minimum value whose difference ΔI_L is the peak to peak value of inductor current ripple.

Selecting a proper value for the power inductor is an important factor in determining converter operational performance. The first step in process of selecting the inductor is to define the acceptable value for inductor ripple current ΔI_L at the application level. The inductance value can be calculated from the following equation [21,59, 61]:

$$L = \frac{(V_I - V_O) \cdot V_O}{V_I \cdot f_S \cdot \Delta I_L} \qquad \text{..... (21)}$$

Where V_I and V_O in Volts, L in Henries, f_S converter switching frequency in Hz, and ΔI_L is the peak to peak inductor current in A.

Observing equation (21) it is evident that a larger value of L goes with a smaller value of inductor ripple current ΔI_L. This results in lower output voltage ripple, better efficiency, and better electromagnetic compliance (EMC) behavior. This comes at the expense of slower load transient response. For this reason, selecting the right value of converter

inductance is made by trade off between the different factors that define the converter performance. As an engineering approach ΔI_L is chosen to be between 20% to 40% of I_O value [59,61].

Another important parameter that needs to be considered is the saturation current I_{SAT} of the selected inductor. This value should not be exceeded in the application as it results in severe reduction in efficiency due to significant inductor value loss, overheating of the inductor core due to steep increase in inductor current and high ripple in output voltage. The maximum current flowing into the conductor can be calculated as in equation (22) [59,61]:

$$I_{L\max} = I_{O\max} + \frac{\Delta I_{L\max}}{2} \qquad \ldots\ldots(22)$$

The selected inductor must have a design value of inductor saturation current that is larger than that calculated in equation (22). In addition to that, the selected inductor should have sufficiently low DC nominal resistance (*DCR*) in order to minimize resistive power losses. Flat wire inductors offer the best possible low *DCR* value for a given core size.

4.5.2. Selecting the Proper Value for Converter Capacitor

The output capacitor is an important part in the PWM converter filter or energy storage elements. Its role is to keep output voltage constant and limit voltage excursions in the output of the converter.

The first parameter of the output capacitor to be investigated the ESR as it plays a vital role in limiting output voltage ripple value to required specifications. The ESR value of the output capacitor is calculated from the following equation [59,61] :

$$ESR = \frac{\Delta V_{O,ripple}}{\Delta I_L} \qquad \ldots..(23)$$

Additional calculation can be made to obtain the value of ESR for output capacitor is to replace the term of the ripple voltage in equation (23) with the value of maximum overshoot allowable in the output of the converter. This case is applicable only if changes from full load to no load are anticipated. Then equation (23) becomes:

$$ESR = \frac{\Delta V_{O,overshoot}}{I_{L,\max}} \qquad \text{.....(24)}$$

Where $\Delta V_{O,overshoot}$ is the maximum voltage overshoot allowable on converter output as specified by load requirements, and I_{Lmax} is the maximum inductor current.

The minimum required value of the output capacitance can be calculated from the following equation [59,61]:

$$C = \frac{L \cdot \left(I_{L,\max}\right)^2}{\left(V_O + \Delta V_{O,overshoot}\right)^2 - V_O^2} \qquad \text{.....(25)}$$

The choice of capacitor made, must meet the ESR and minimum value of output capacitance C in addition to selecting the proper voltage rating which must be selected so that the voltage rating of the capacitor is always higher than the maximum voltage expected to occur at the output. Some references suggest a 50% increase in the voltage rating of the capacitor over the output voltage of the converter [21,59,61].

It is desirable to add an input capacitor C_{in} to the buck converter circuit as this capacitor will help reducing ripples in input voltage caused by the discontinuous input current resulting from converter operation. When selecting the input capacitor the first thing to calculate is the RMS current and its voltage rating.

The RMS current can be calculated as follows [61]:

$$I_{Cin,RMS} = I_O \cdot \sqrt{D - D^2} \qquad \text{.....(26)}$$

The maximum value for this current component occurs when the duty cycle D is 50% the RMS current of the input capacitor reaches the highest value throughout the operation range of the converter. In this case the chosen capacitor must have ESR value small enough not to let this current component result in its overheating. As for its voltage rating, this capacitor must be rated at least 50% over maximum expected input voltage. In addition to this input capacitor, it is preferred to add a small value ceramic capacitor in parallel to decouple high frequency components occurring on the input power line.

4.6. Power Losses of the Buck Converter

Buck converter circuits especially those designed for low output voltages, have many parasitic parameters that lead to power loss. These include all series resistance found in passive and active components, in addition to parasitic capacitances C_G, stray inductance L_S, and drain-body diodes of the switching power transistors [21,59].

The following subsections will detail the main sources of dissipation that cause the conversion efficiency of a buck converter circuit to drop below unity value.

4.6.1. Conduction Losses in Buck Converter

Current flowing through non-ideal circuit components like power transistors, the filter elements, and circuit interconnections can results in dissipation in each component where i_{rms} is the root mean squared current through the component, and R is the resistance of the component. In the transistor it will be $R_{DS(on)}$, while in the inductor it will ESR_L, in the capacitor it will be ESR_C. The total power loss in the converter P_q is given as:

$$P_q = i_{rms}^2 \cdot R \qquad \text{.....(27)}$$

In PWM converters, i_{rms} current has a DC and an AC component, thus:

$$i_{rms}^2 = i_{rms(DC)}^2 + i_{rms(AC)}^2 \qquad \text{.....(28)}$$

Where the *DC* rms current component is given by:

$$i_{rms(DC)}^2 = D \cdot I_O^2 \qquad \text{.....(29)}$$

While the *AC* rms current component is given by:

$$i_{rms(AC)}^2 = \frac{1}{3} \cdot D \cdot \left(\frac{\Delta I_L}{2} \right)^2 \qquad \text{.....(30)}$$

D indicates the duty cycle of the current flow through a given component.

It can be observed that the DC conduction losses are proportional to the square of the *DC* load current I_O. While the *AC* conduction losses have a fixed value that degrades efficiency figures especially at light load.

4.6.2. Losses Due to Flywheel Diode implementation.

The implementation of fly wheeling diode in the design of the Buck converter imposes degradation in overall possible efficiency, and this loss becomes very evident in low voltage applications. To visualize the impact of implementing the fly wheel diode in buck converter design an assumption that other losses are negligible compared to those caused by implementing the fly wheel diode is made. If the buck converter circuit shown in figure (4.3) was implemented in a battery operated application where the load voltage is required to be 1.55 volts, and the power source is a lithium–ion battery with nominal voltage of 3.7 volts, as the fly wheeling diode operates for the period equal to (1-*D*) of the switching period, then the maximum efficiency for this circuit can be given by:

$$\eta_{\max}\% = \frac{V_O}{V_O + (1-D)\cdot V_{Fdiode}} \cdot 100 \qquad \ldots(39)$$

In this example if the diode being used is a silicon diode having a forward voltage of approximately 0.7 volts then the maximum achievable efficiency would be about 79%. Even if this diode is replaced with a Shottky diode with forward voltage of 0.3 volts the maximum attainable efficiency would be about 89%.

But if this diode is replaced with a power MOSFET switching device working as a synchronous rectifier with extremely low voltage drop across the terminals of a conducting device then using the same previous assumptions of losses being negligible, the maximum efficiency attainable of this low voltage buck converter would approach 100%.

While the implementation of the synchronous rectifier has its merits, it also comes with a host of extra requirements that makes its implementation not straightforward.

4.6.3. Gate-Drive Losses in the Buck Converter

Driving the PWM switching power transistor on and off each cycle results in gating power dissipation P_g, the average of which is given by:

$$P_g = E_g \cdot f_S \qquad \text{....(31)}$$

where E_g is directly proportional to the gate energy due to charge Q_G transferred with each turning on and off of the device, and is due to the total gating charge of the device. It can include dissipation in the drive circuitry of the PWM switch and the synchronous rectifier (if implemented).

The Gate-drive losses are independent of load current and will therefore also degrade efficiency at light loads.

4.6.4. Power Losses Due to Timing Errors

These power losses are associated with the Buck converter topology that employs the synchronous rectifier instead of the flywheel diode; here three loss mechanisms can be defined for timing errors in driving the PWM power MOSFET and the synchronous rectifier power MOSFET. The causes of these losses can be attributed to the following reasons [21]:

- **Zero-Dead-Time:** When the PWM switching device and the Synchronous rectifier Switching device are turned on an off alternately, a short-circuit path may occur temporarily between the input power rails during power MOSFET device switching transitions. This is called *cross conduction current* and is a dangerous condition that degrades efficiency significantly and could lead to device failure. To avoid potentially large short-circuit losses, it is essential to introduce dead-times between the switching change over taking place between PWM device and the synchronous rectifier device to ensure that the two devices can never be given the chance of conducting simultaneously.

- **Long Dead-Times:** if the dead time introduced between the alternate switching of the PWM power device and the synchronous rectifier power device is too long,

the body diode of the synchronous rectifier power MOSFET starts conducting if the durations of the dead-times are too long, the body diode of the NMOS power transistor may be forced to pick up the inductor current for a fraction of each switching cycle. In low-voltage applications, the forward bias voltage V_f of the NMOS device body diode is a bout 0.7 volt. This value can be very close to output voltage of the converter and this makes its conduction loss significant. This power loss due to body diode conduction P_{Bdiode} is given by:

$$P_{Bdiode} = 2 \cdot I_O \cdot V_f \cdot t_{err} \cdot f_S \qquad \ldots\ldots(32)$$

where t_{err} is the timing error between PWM power MOSFET and Synchronous rectifier power MOSFET conduction intervals.

To aggravate the situation furthermore, when the PWM switching device is turned on, it must remove the excess minority carrier charge from the body diode, thus dissipating further energy required for reverse recovery (E_{rr}) that is given by:

$$E_{rr} = Q_{rr} \cdot V_I \qquad \ldots\ldots(33)$$

where Q_{rr} is the stored charge in the body diode.

- **Short Dead-Times:** Power switching devices in a PWM converter are switched on hard. When the PWM MOSFET is switched on, it charges parasitic capacitance C_G to V_I with each switching cycle, dissipating an average power P_{CG}:

$$P_{CG(LH)} = \frac{1}{2} \cdot C_G \cdot V_I^2 \cdot f_{SW} \qquad \ldots\ldots(34)$$

where C_G includes reverse-biased drain-body junction diffusion capacitance C_{db} and some or all of the gate-drain overlap (Miller) capacitance C_{gd} of the power transistors, wiring capacitance from their interconnection, and stray capacitance associated with the main inductor L.

When PWM power MOSFET is turned off, the inductor begins to discharge C_G from V_{in} to ground. If the synchronous rectifier MOSFET is turned on exactly when v_{CG} reaches ground, this transition is lossless. If the NMOS device is turned

on too late, C_G will be discharged below ground, until the body diode is forced to conduct. If the NMOS device is turned on too early, it will discharge C_G to ground through its channel thus introducing power losses that can be calculated from:

$$P_{CG(HL)} = \frac{1}{2} \cdot C_G \cdot v_{CG}^2 \cdot f_{SW} \leq \frac{1}{2} \cdot C_G \cdot V_I^2 \cdot f_{SW} \quad \text{.....(35)}$$

4.6.5. Switching Losses Due to Stray Inductance

Energy storage by the stray inductance L_S in the loop formed by the input decoupling capacitor C_{in} and the power transistors causes dissipation.

If the PWM switch and the synchronous rectifier MOSFETs are considered ideal, and the converter inductor L is considered a current source of $i(t) = i_L(t)$ then when PWM switching device turns on, current through L_S starts rising from i_{LS}=0 to i_{LS}= *Imin, where Imin* is given by [59]:

$$I_{\min} = I_O - \frac{\Delta I_L}{2} \quad \text{....(36)}$$

When PWM switch opens and synchronous rectifier closes, current through L_S starts decreasing from $i_{LS} = I_{max}$ to $i_{LS} = 0$, where I_{max} is given by:

$$I_{\max} = I_O + \frac{\Delta I_L}{2} \quad \text{....(37)}$$

The average power dissipated in stray inductances can be given by:

$$P_{LS} = \frac{1}{2} \cdot L_S \cdot \left(I_{\min}^2 + I_{\max}^2 \right) \quad \text{.....(38)}$$

This loss component is dependent on load current, and the value of L_S which depends on PCB layout component layout, boding and packaging. It can be reduced by minimizing the area where this critical high current loop occurs and using PCB techniques to minimize stray inductances.

4.6.6. Losses Due to Quiescent Operating Power

The PWM control circuitries along with other secondary circuits dissipate static power called quiescent power. This is the power consumed by a circuit when it is connected to power source. In low-power applications, this power consumed by control circuitry may present a big contribution to the total power losses, even at full-load resulting in poor power efficiency.

4.7. Implementing Adaptive and Predictive Dead-Time Control in Synchronous Buck Converter for Better Efficiency

The implementation of the synchronous rectifier has its merits but it also comes with a host of extra requirements. First of all it will require additional gate drive circuitry, then the problem of cross conduction current takes place and to prevent it, there are additional circuit requirements that add to the increased overall complexity of the design. As has been covered by last section the problem of cross conduction current can be solved by introducing a delay between the turning off of the PWM converter and turning on of the synchronous rectifier and vice versa. If the delay is fixed then depending on load conditions this delay may becomes too long or too short, thus resulting in either a small cross conduction loss or body diode conduction loss as shown in section (4.6.4). The solution for this problem is to make this delay adaptive or predictive thus ensuring that the switching devices are turned on and off without risking cross conduction current or body diode conduction losses [21,59].

The adaptive delay gating technique delivers a variable gating delay that changes with circuit operating conditions thus ensuring that the required delay is always introduced to prevent cross conduction current and not to be too long to cause body diode conduction. The adaptive delay circuit senses the node voltage of the inductor and switching elements and opens gate signal when this voltage passes a specified level. Figure (4.12) illustrates the adaptive gate drive technique [62].

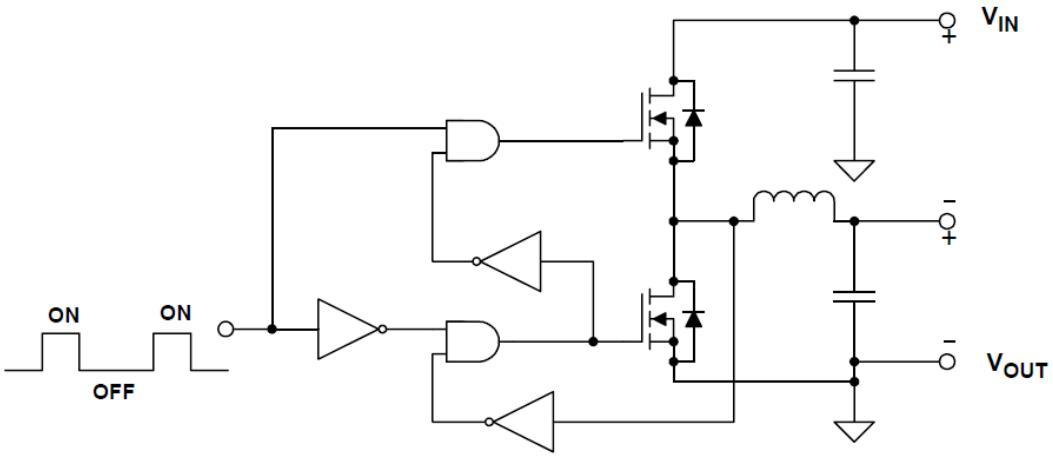


Figure (4.12) The adaptive gate drive circuit technique [62]

The advantage of the adaptive drive technique comes from the instantaneous gate delay adjustment that compensates for temperature dependent device delays and different MOSFET devices implementation. The weak points of this technique arises from its inability to compensate for MOSFET gate charging delays and to detect the synchronous rectifier MOSFET full recovery from the on state which are compensated for by introducing additional fixed delay between PWM turning on and synchronous rectifier turning off. This approach leads to cases where the body diode of the synchronous rectifier starts conducting resulting in losses affecting power control circuit efficiency. The solution for this shortcoming is presented by Texas Instruments in a method called the predictive gate drive technique [62,63] introduced in their UCC27222 gate drive device. Figure (4.13) shows the switch node voltage waveform along with different delay introduction technique.

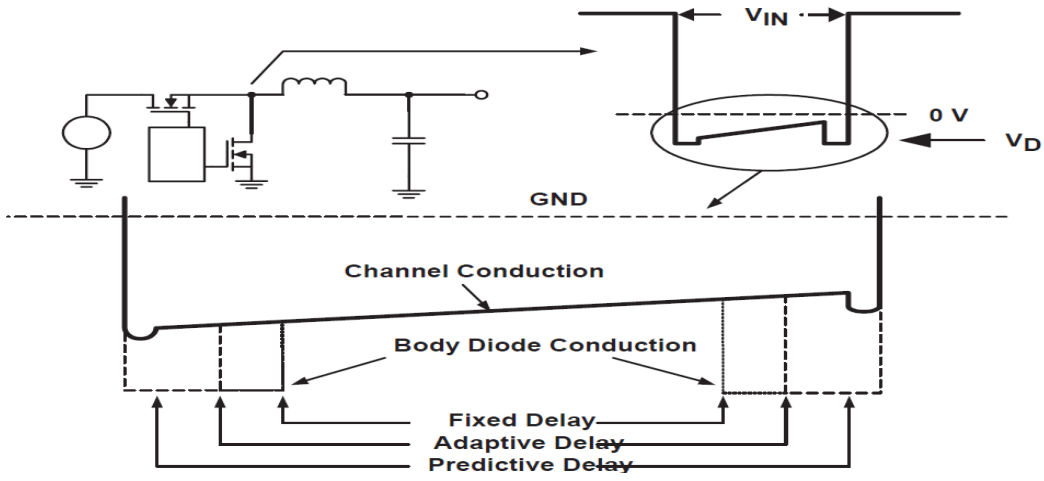


Figure (4.13) The switch node voltage waveform in a Buck converter [63]

Figure (4.13) shows the switch-node voltage waveform for a synchronously rectified buck converter. The relative effects of a fixed-delay drive scheme, the adaptive delay drive scheme, and the predictive delay drive scheme are shown. It can be concluded that the longer the time spent in body-diode conduction during the rectifier conduction period, the lower the efficiency. In addition to that the predictive delay circuit can prevent the body diode from becoming forward biased while at the same time avoids cross conduction. This results in a significant power saving when the PWM MOSFET is turning on, and minimizes reverse recovery loss in the body diode of the synchronous rectifier MOSFET.

The UCC27222 provides drive signals that can control two N-channel MOSFETs thus introducing better design flexibility by not requiring a complementary pair switching devices. The signal that is used to drive an N-channel MOSFET as a rectifier is carefully coordinated with the drive signal for the PWM switch so that there is minimum delay from the time that the MOSFET rectifier turns off and the main switch turns on, and minimum delay from when the main switch turns off and the MOSFET rectifier turns on. This Predictive Gate Drive delay scheme makes use of information from the current switching cycle to adjust the delays that are to be used in the next cycle as shown in figure (4.14).

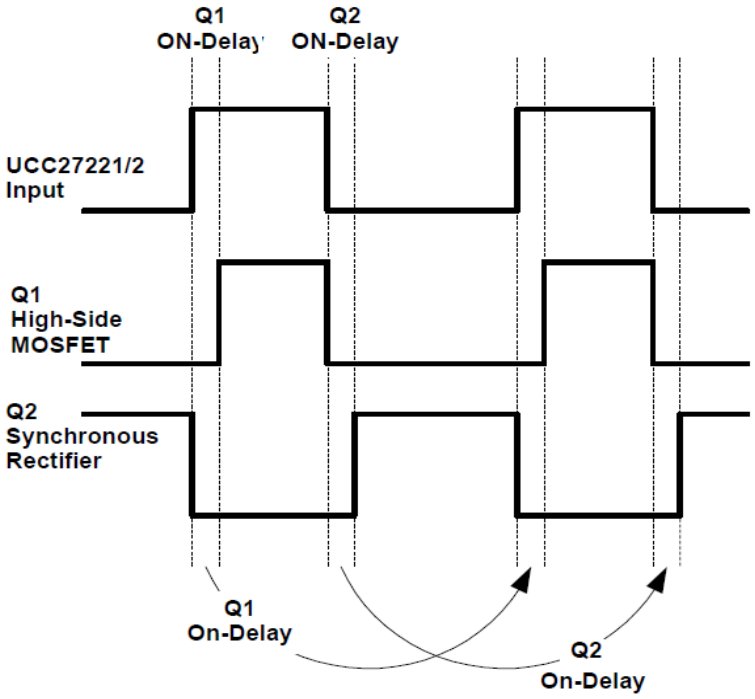
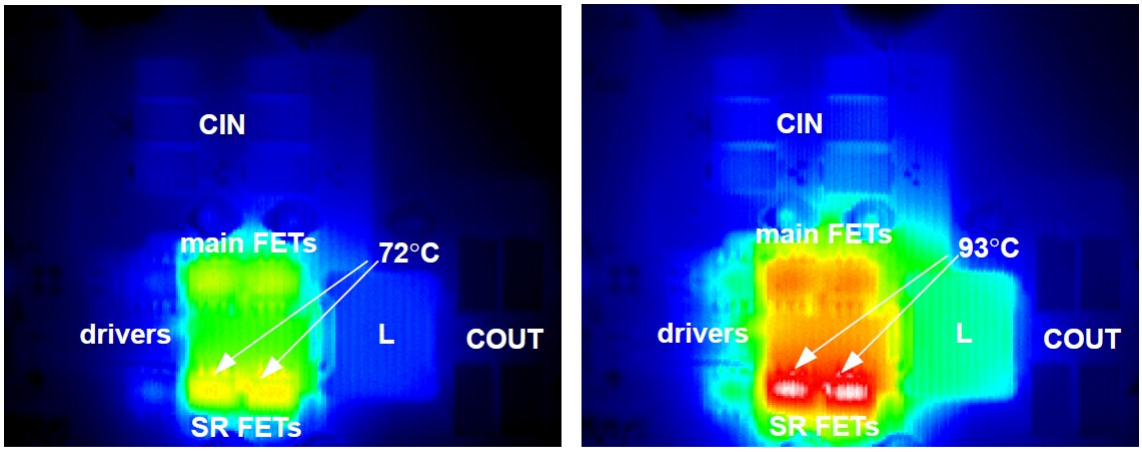


Figure (4.14) The predictive delay technique used in UCC27222

Implementing the predictive gate delay technique benefits reducing power dissipation on the PWM MOSFET as well, although the savings made are not as significant as the savings in the synchronous rectifier MOSFET.

The reduced power dissipation gained by introducing the predictive gate drive delay reflects on cooler driving of power devices as can be seen from figure (4.15) that represents a thermal imaging of a power MOSFET device implemented in a buck converter design operated under the same load and source condition while using predictive gate drive delay technique (a) and while using adaptive gate drive delay technique (b). The white color indicates temperatures in the range of 93°C, the yellow color indicates temperatures in the range of 72°C. These pictures indicate that using the predictive gate drive delay technique enables cooler drive components operation resulting in better efficiency, smaller heat sink requirements, and longer mean time between failure MTBF resulting in higher device reliability.



(a) (b)

Figure (4.15) Thermal imaging of power MOSFET device operating with (a) predictive gate drive delay technique and (b) adaptive gate drive delay technique.

4.8. Alternative Techniques for Voltage Regulation in Low Power Conditions

When controlled system power requirements start falling to few milliamperes as the case when the processor goes to standby mode or sleep mode, providing the required operating current using the PWM converter can prove very taxing regarding energy

consumption of the control elements of the buck converter with regards to the current requirements of the load. In that case, two alternatives that do not require magnetic components are linear regulators and switched-capacitor converters. Both types of circuits can be advantageous in ultra-low-power applications.

4.8.1. Switched capacitor Converters

Switched-capacitor converters (also known as charge pumps) [60,64] are widely used in applications requiring low operating currents. These converters deliver stable supply voltage at these low load currents and operate with higher efficiency figures than possible with PWM converters. Unlike a PWM converter, a switched-capacitor converter requires no magnetic components. In addition to that, it is often possible to integrate the necessary capacitors on a regulator die, but their application is usually limited to those in which very low output power is required.

Circuit simplicity and reduced components count in addition to low quiescent current and efficiency figures that could reach 90% while working in Buck mode makes this type of converters an attractive choice for an applications condition that does not require high current ratings. Figure (4.16) shows a simple arrangement for a switched capacitor converter that shows how the flying capacitor can be replaced with a resistor in the equivalent circuit.

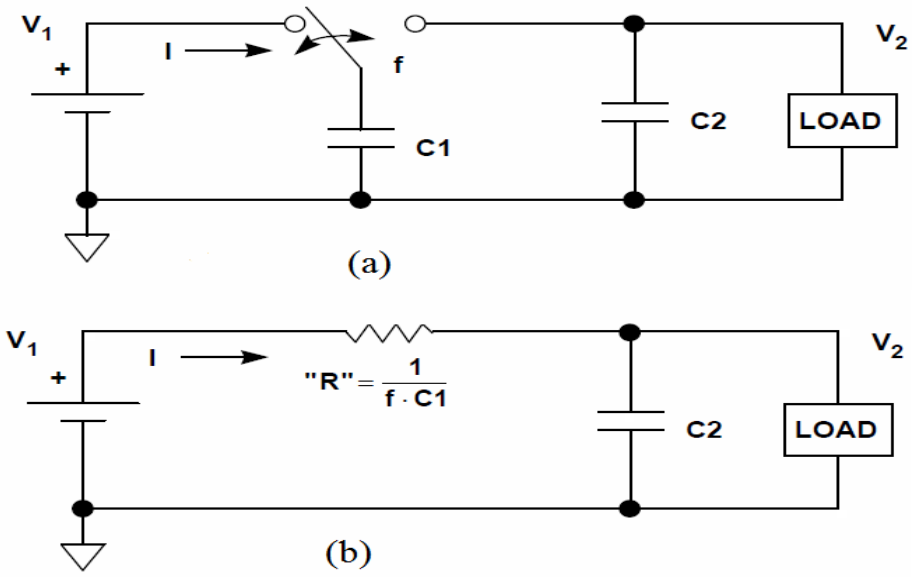


Figure (4.16) A simple Switched capacitor converter (a), and with its resistive equivalent circuit (b) [64].

The circuit in figure (4.16) represents simple model for a switched capacitor regulator. In this model the capacitor C_1 switches between the output voltage V_2 and the input voltage V_1 at a frequency f. At the output there is the reservoir capacitor C_2 and the load that can be represented by R_L.

The charge transmitted per cycle (ΔQ) can be given as:

$$\Delta Q = C_1 \cdot (V_1 - V_2) \qquad \ldots\ldots(39)$$

This charge corresponds to an average current I given by:

$$I = \frac{\Delta Q}{T} = f \cdot \Delta Q = f.C_1(V_1 - V_2) = \frac{V_1 - V_2}{1/(f \cdot C_1)} \qquad \ldots\ldots(40)$$

The function of the charge transfer done by C_1 at frequency f can be replaced by the function of an equivalent resistor R_{ER} connected between the source and the load:

$$R_{ER} = \frac{1}{f \cdot C_1} \qquad \ldots\ldots(41)$$

The power dissipation associated with this equivalent resistance is essentially forced to be dissipated in the switch on resistance and the capacitor ESR, irrespective of their values. In addition to these two dissipation sources comes the switching device on resistance and its contribution should be taken into account. However it can be observed that using higher frequencies and larger capacitors tend to reduce the value of the equivalent dissipative resistance resulting in minimized losses. However, increasing switching frequency tends to increase switching losses. Therefore the optimum switched capacitor operating frequency is highly process and device dependent. For this reason, the specific recommendations given in the data sheet must be followed for each device being implemented.

In this work the Ti TPS60500 switched capacitor buck regulator has been implemented as a secondary power supply used to supply the target processor core while it is in standby or sleep mode. It is characterized by low quiescent current and high efficiency figures capable of reaching 90%. It has the capability to change its operating mode to

LDO when operated at higher currents. This feature helps obtaining smoother transfer from the secondary regulator to a primary regulator as the secondary regulator keeps supplying load current until the primary regulator commences operation.

4.8.2. Low Dropout (LDO) Regulators.

This type of regulators are essentially series closed loop regulators in which the regular passing element an NPN bipolar transistor is replaced with a MOSFET device ensuring possible operation of the regulator even at very low voltage difference between input and output voltage. Typical LDO regulators can keep on operating even when the difference between input and output voltage reaches 0.1volt. While the series regulator that implements a bipolar transistor as a series element stops operating when the difference between input and output voltages drops below 2Volts. The LDO regulators are characterized by low noise, and are very useful in applications requiring stable low noise voltage sources. The Intersil™ ISL9021A is a typical LDO regulator with a host of protection features and high power supply rejection ratio (PSRR). Figure (4.17) shows the typical circuit of an LDO regulator [21].

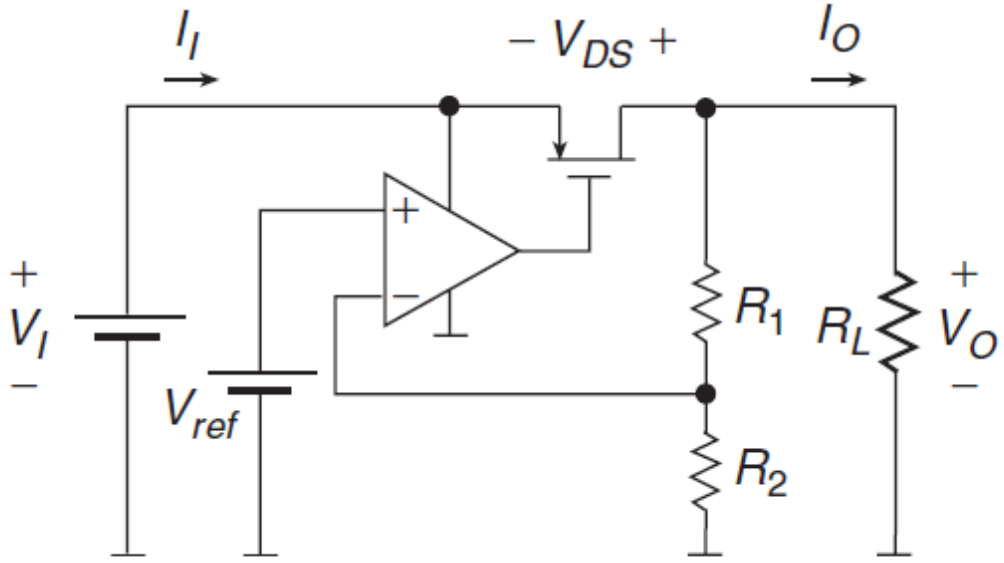


Figure (4.17) Circuit elements of a typical LDO regulator [21]

4.9. Chapter Summary

In this chapter, a general definition for voltage regulation is given with emphasis on the synchronous buck converter, how to select its components, how to improve its efficiency, and how to measure the power losses in it. It has also covered the types of regulators that are alternatively favoured over PWM converters in low load current cases.

Chapter Five

Mathematical Modelling and Simulation of the PWM Buck Converter

5.1. Introduction

In this chapter a mathematical model for the PWM buck converter is derived after selecting circuit components that are used to build the prototype model that is being tested and evaluated empirically. A RISC based micro controller is selected to function as a controller for the Buck converter in addition to furnishing other vital function in the complete VRM system.

A small signal analysis is carried out using the mathematical derivations of the buck converter model using matlab.

A simulation model is built using matlab/simulink in order to investigate the closed loop response and then trying different types of controllers and select the type suitable for implementation on the selected platform.

5.2. Mathematical Analysis of the Synchronous Buck Converter

The design of the smart VRM started with the choice of the control platform that will govern the operation of the module. A microcontroller with micro-power requirements equipped with the required peripheral devices mainly the ADC and PWM signal generation capability, storage capacity, and computational power is selected. The selection was made while keeping in mind that the power loss contribution of the control

device must be as small as possible in order to boost module efficiency. For this reason an 8-bit micro controller from Microchips™ the PIC16F1509 was selected [65].

The buck converter components were calculated while considering the capabilities of the selected microcontroller to deliver the require PWM drive signal frequency. This microcontroller PWM module can deliver up to about 200 KHz signal, but at low resolution for duty cycle control, lower frequency settings at about 80 KHz for the PWM module allows for 8 bit duty cycle resolution. Buck converter components were calculated for the following operating frequencies 40 KHz, 80 KHz, and 120 KHz using the design methods explained in chapter 4. Table 5.1 contains the selected components parameters and values for the buck converter circuit.

Table 5.1: Synchronous buck converter component values and parameters

Circuit Elements Specs.	At Operating frequency		
	40 KHz	80 KHz	120 KHz
FET_1 Rds_{ON} (mΩ)	2.1	2.1	2.1
FET_2 Rds_{ON} (mΩ)	2.1	2.1	2.1
L (μH)	100	47	33
ESR_L (Ω)	0.19	0.13	0.066
C (μF)	150	68	47
ESR_C (m Ω)	25	55	70
R_{LOAD} (Ω)	2.356	2.356	2.356

These parameters will be implemented in the small signal analysis processes.

The simplified circuit of the buck converter is used in performing the mathematical derivations for the buck converter circuit. Figure 5.1 shows the approximate components of the synchronous buck converter circuit where the switching elements were replaced by an ideal switch in series with a resistor having the value of the on resistance of the channel, the inductor was replaced with an ideal inductor in series with a resistance which is the effective series resistance of the inductor, the capacitor was replaced by an ideal capacitor in series with a resistor having the value of the effective series resistance of the capacitor selected in the design.

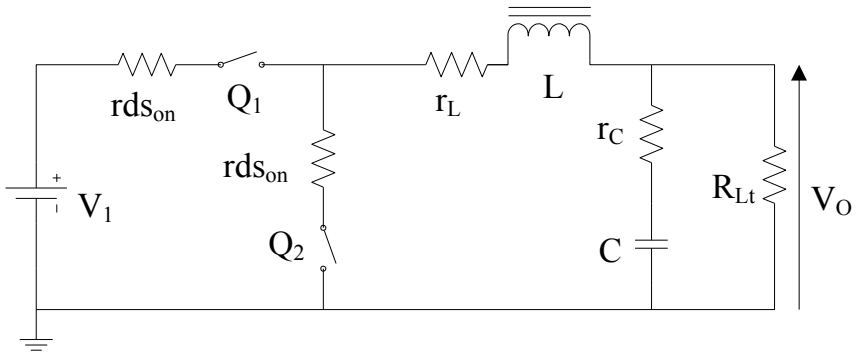


Figure (5.1) The buck converter approximate circuit used in mathematical analysis.

Where Q1 is the MOS Switch and Q2 is the MOS synchronous rectifier, V_1 is the source voltage, V_O is the output voltage, L is the converter Main Inductance, C is the main capacitor and R_{Lt} is the load resistance. Additional elements are included in the circuit like the on channel resistance of the switch and synchronous rectifier MOS transistors (rds_{on}), ESR of the Inductor (r_L) and Capacitor (r_C). These elements are essential to make the model mimic near life operating conditions.

5.2.1. Deriving the Mathematical Relationships

The analysis method of this converter has been carried out assuming CCM operation mode for the buck converter and has followed the literature of references [21,59, 66,67].

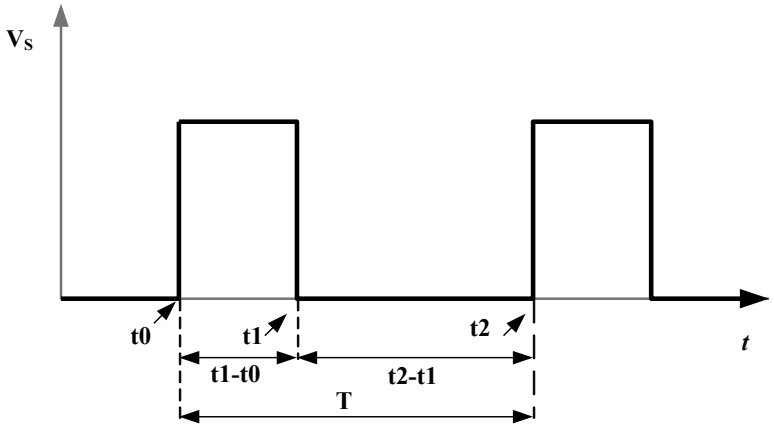


Figure (5.2) Switching waveform for the Synchronous buck converter model

Assuming that both Q_1 and Q_2 operate as switches, if Q_1 is ON then Q_2 is OFF and vice versa. Both of the MOSFETs have a turn on resistance of rds_{on}. Furthermore, Vs is a square wave with period of T which is equal to (t_1+t_2) as shown in figure (5.2).

Circuit analysis will consider each period as follows:

- **At t0<t<t_1** ($Q_1$is ON and Q_2 is OFF)

  Applying Kirchhoff's voltage law on the inductor results in:

$$V_1 - i_L \cdot rds_{on} - L\frac{di_L}{dt} - i_L \cdot r_L - V_O = 0 \quad \text{..... (41)}$$

  Or

$$\frac{di_L}{dt} = \frac{1}{L}\left[(V_1 - V_O) - i_L(rds_{on} + r_L)\right] \quad \text{..... (42)}$$

- At **t_1<t<t_2** ($Q_1$is OFF and Q_2 is ON)

  Applying Kirchhoff's voltage law on the inductor gives:

$$-i_L \cdot rds_{on} - L\frac{di_L}{dt} - i_L \cdot r_L - V_O = 0 \quad \text{..... (43)}$$

  Or

$$\frac{di_L}{dt} = \frac{1}{L}\left[-V_O - i_L \cdot (rds_{on} + r_L)\right] \quad \text{.....(44)}$$

By introducing Sf as a switching function to equations 42 and 44, that turns V1 ON and OFF or

$$Sf = \begin{cases} 1 & t_0 < t < t_1 \\ 0 & t_1 < t < t_2 \end{cases} \quad \text{..... (45)}$$

Results in:

$$\frac{di_L}{dt} = \frac{1}{L}\left[(Sf.V_1 - V_O) - i_L \cdot (rds_{on} + r_L)\right] \quad \text{..... (46)}$$

The output voltage of the circuit V_0 is given by:

$$V_O = i_L \cdot Z_L \quad \text{…….. (47)}$$

Where Z_L is the output impedance and it is given by

$$Z_L = \frac{(R_{Lt} \cdot Z_C)}{(R_{Lt} + Z_C)} \quad \text{…….. (48)}$$

and

$$Z_C = {}^{1}\!\!\diagup\!\!{}_{(S.C)} + r_C \quad \text{…….. (49)}$$

or it can be written as:

$$Z_L = \frac{R_{Lt}.(S.C.r_C + 1)}{S.C.(R_{Lt} + r_C) + 1} \quad \text{……(50)}$$

Substituting 50 into 47 results in:

$$[S.C.(R_{Lt} + r_C) + 1].V_O = R_{Lt} \cdot (S \cdot C \cdot r_C + 1).i_L \quad \text{……(51)}$$

Taking the inverse Laplace transform of equation (51) results in:

$$\frac{dV_O}{dt} = \frac{(C \cdot r_C R_{Lt} \frac{di_L}{dt} + R_{Lt}.i_L - V_O)}{C.(R_{Lt} + r_C)} \quad \text{……(52)}$$

This is the voltage equation of the buck converter,

Now to analyze the stability of the circuit equation 46 and 52 will be rewritten as follows respectively:

$$i'_L = \frac{1}{L}\left[\left(dV_1 - V_O\right) - i_L\left(rds_{ON} + r_L\right)\right] \quad \text{……(53)}$$

$$v'_O = \frac{C \cdot r_C \cdot R_{LT} \cdot i'_L + R_{LT} \cdot i_L - V_O}{C \cdot (R_{LT} + r_C)} \quad \text{.....(54)}$$

Now to derive the steady state roots (S.S.R):

Let

$$i'_L = X'_1 \quad , \quad X_1 = i_L$$

$$V'_O = X'_2 \ , \ X_2 = V_O \quad \text{.....(55)}$$

U as input dV_1 where $d[0 \to 1]$ (d is the control action representing the duty cycle of the PWM signal)

$$X'_1 = \frac{1}{L}\left[(dV_1 - X_2) - X_1(rds_{ON} + r_L)\right] \quad \text{.....(56)}$$

$$X'_2 = \frac{C \cdot r_C \cdot R_{LT} \cdot X'_1 + R_{LT} \cdot X_1 - X_2}{C(R_{LT} + r_C)} \quad \text{.....(57)}$$

Substituting 56 in 57 results in:

$$X'_2 = \frac{C \cdot r_C \cdot R_{LT} \cdot \frac{1}{L}\left[(dV_1 - X_2) - X_1(rds_{ON} + r_L)\right] + R_{LT} \cdot X_1 - X_2}{C(R_{LT} + r_C)} \quad \text{..... (58)}$$

$$X_2' = \frac{\frac{C \cdot r_C \cdot R_{LT}}{L} \cdot dV_1 - \frac{C \cdot r_C \cdot R_{LT}}{L} \cdot X_2 - \frac{(rds_{ON} + r_L) C \cdot r_C \cdot R_{LT}}{L} \cdot X_1 + R_{LT} \cdot X_1 - X_2}{C(R_{LT} + r_C)} \quad ..$$

(59)

$$X_2' = \frac{C \cdot r_C \cdot R_{LT}}{L \cdot C(R_{LT} + r_C)} dV_1 - X_2 \left[\frac{\left(\frac{C \cdot r_C \cdot R_{LT}}{L} \right) + 1}{C(R_{LT} + r_C)} \right] - X_1 \left[\frac{\left(\frac{rds_{ON} + r_L}{L} \right) C \cdot r_C \cdot R_{LT} - R_{LT}}{C(R_{LT} + r_C)} \right] \quad ..(60)$$

Now putting the equation for small signal analysis in state space form:

$$\begin{bmatrix} X_1' \\ X_2' \end{bmatrix} = \begin{bmatrix} \frac{-(rds_{ON} + r_L)}{L} & -\frac{1}{L} \\ -\left[\frac{\left(\frac{rds_{ON} + r_L}{L} \right) C \cdot r_C \cdot R_{LT} - R_{LT}}{C(R_{LT} + r_C)} \right] & -\left[\frac{\frac{C \cdot r_C \cdot R_{LT}}{L} + 1}{C(R_{LT} + r_C)} \right] \end{bmatrix} \cdot \begin{bmatrix} X_1 \\ X_2 \end{bmatrix} + \begin{bmatrix} \frac{V_{IN}}{L} \\ \frac{C \cdot r_C \cdot R_{LT} \cdot V_{IN}}{L \cdot C(R_{LT} + r_C)} \end{bmatrix} d \quad ...(61)$$

Where $d = [0 \rightarrow 1]$

Output:

$$X_2 = \begin{bmatrix} 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} X_1 \\ X_2 \end{bmatrix} \quad .....(62)$$

The standard form of the C/Cs is [68]:

$$S^2 + 2\xi\omega_n S + \omega_n^2 = 0 \quad .....(63)$$

This form will be translated to the following:

$$\left(\frac{C\cdot r_C\cdot L+C\cdot L\cdot R_{LT}}{C\cdot r_C\cdot L+C\cdot L\cdot R_{LT}}\right)S^2+\left(\frac{L+C\cdot r_C\cdot r_L+C\cdot r_C\cdot R_{LT}+C\cdot r_L\cdot R_{LT}+C\cdot r_C\cdot rds_{ON}+C\cdot R_{LT}\cdot rds_{ON}}{C\cdot r_C\cdot L+C\cdot L\cdot R_{LT}}\right)S+\left(\frac{r_L+R_{LT}+rds_{ON}}{C\cdot r_C L+C\cdot L\cdot R_{LT}}\right)=0 \quad ..(64)$$

Therefore:

$$2\xi\omega_n=\frac{L+C\cdot r_C\cdot r_L+C\cdot r_C\cdot R_{LT}+C\cdot r_L\cdot R_{LT}+C\cdot r_C\cdot rds_{ON}+C\cdot R_{LT}\cdot rds_{ON}}{C\cdot r_C\cdot L+C\cdot L\cdot R_{LT}} \quad \ldots(65)$$

and

$$\omega_n^2=\frac{r_L+R_{LT}+rds_{ON}}{C\cdot r_C\cdot L+C\cdot L\cdot R_{LT}} \quad \ldots\ldots.(66)$$

The time constant of the system (τ) is:

$$\tau=\frac{1}{\xi\omega_n} \quad \ldots\ldots.(67)$$

And the damping factor (ζ) is:

$$\xi=\frac{L+C\cdot r_C\cdot r_L+C\cdot r_C\cdot R_{LT}+C\cdot r_L\cdot R_{LT}+C\cdot r_C\cdot rds_{ON}+C\cdot R_{LT}\cdot rds_{ON}}{2\omega_n\left(C\cdot r_C\cdot L+C\cdot L\cdot R_{LT}\right)} \quad ..(68)$$

The natural frequency of the system (ω_n) is:

$$\omega_n=\sqrt{\frac{r_L+R_{LT}+rds_{ON}}{C\cdot r_C\cdot L+C\cdot L\cdot R_{LT}}} \quad \ldots\ldots\ldots(69)$$

To investigate the effect of changing of various system components parameters on system behaviour, Matlab based programs were written to test the open loop system's behaviour to the variation of these parameters. Additional calculations were carried out for a converter designed to operate on the same specified load but at different frequencies, 40 KHz and 120 KHz, in addition to the first design that was for the 80 KHz PWM operation.

5.2.2. Performing Small Signal Analysis

First the effect of load changes on system time constant is investigated. The resulting response to this parameter variation can be observed in figure (5.3). The load resistance was changed through the range from 2.345Ω to 23.45Ω to mimic load variations from heavy load to light load.

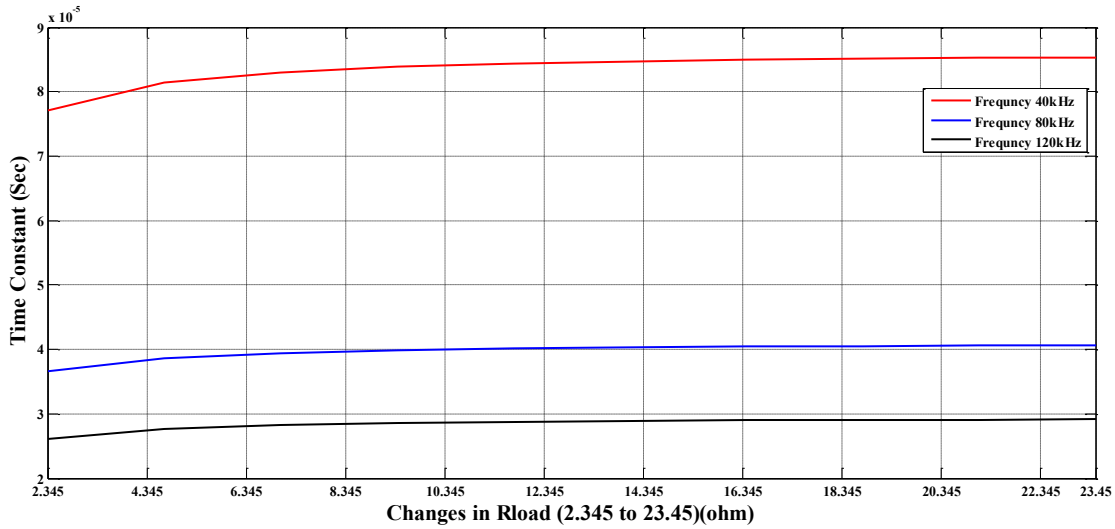


Figure (5.3) The effect of load resistance change on system time constant

On observing figure (5.3) it can be noticed that as load current decreases, the system time constant increases. This effect is more prominent for lower frequency operation of the converter. For 40 KHz operation the change in time constant was from 77 µSec To 85 µSec in response to load resistance change from low value to high value. The 80 KHz version showed lesser susceptibility to the changes in this parameter and for the same variation and the change in time constant was from 37 µSec To 41 µSec in response to the same range of change in load resistance. The 120 KHz version showed even lesser change in system time constant in response to load changes, the resulting time constant change

was in the range of 26 µSec to 29 µSec in response to the same range of change in load resistance. Figure (5.4) shows the effect of load changes on system damping factor value.

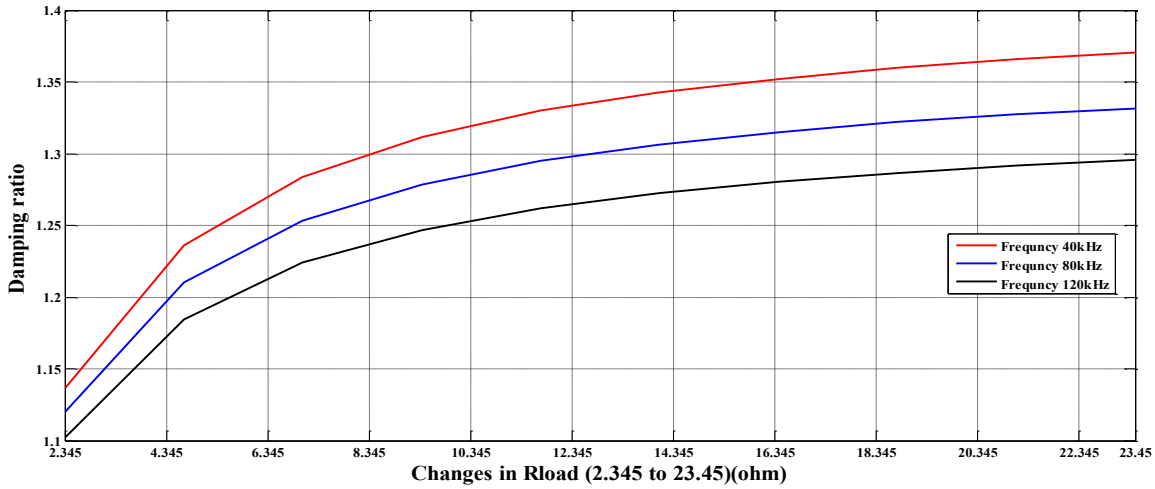


Figure (5.4) The effect of load resistance change on system damping factor

From figure (5.4) it can be concluded that the effect of load change on system damping factor, lower loads (higher load resistance) results in higher values for damping factor and this change is large for converter operation at lower frequencies. In figure (5.5) the same parameter change effect on system natural frequency is observed.

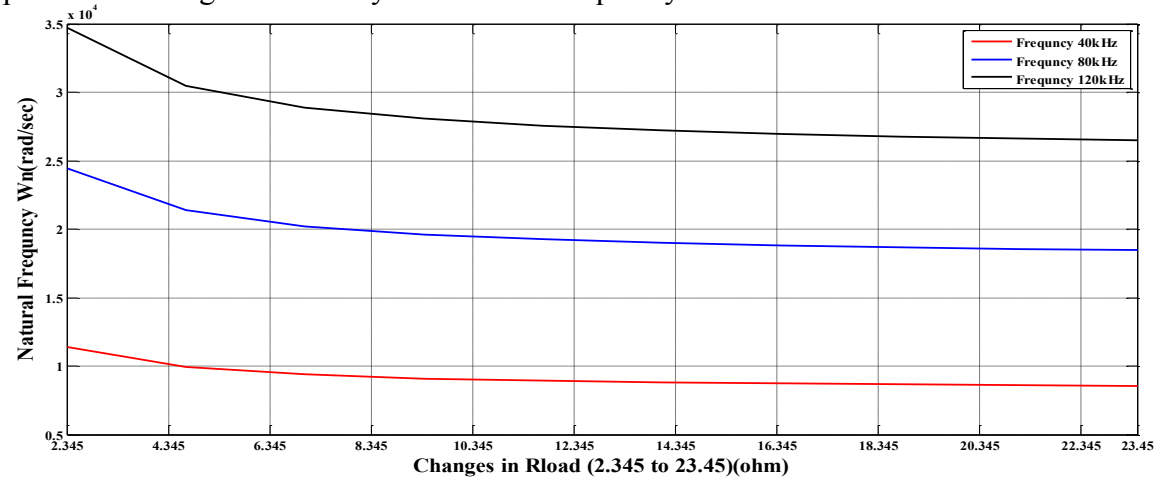


Figure (5.5) The effect of load resistance change on system natural frequency

From this figure it can be concluded that the effect of load change on system's natural frequency is proportional which means that the natural frequency of the system increases and the load current increases and the effect is more evident on converter designs that operate on higher PWM frequencies.

The next three figures will illustrate the effect of capacitance ESR value change on systems parameter. This effect shows how the implementation of different types of capacitors can affect buck converter system parameters. Figure (5.6) shows the effect of capacitance ESR change on system's time constant.

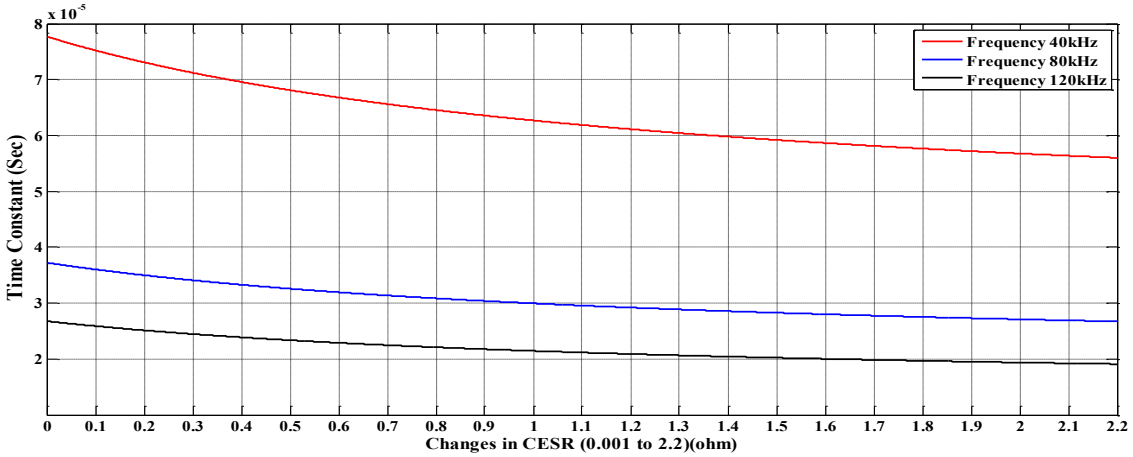


Figure (5.6) The effect of capacitance ESR change on system's time constant.

This figure illustrates the effect of using different types of capacitors on converter system parameters. For instance, low ESR values correspond to implementing MLCC type of ceramic capacitors while the large values of ESR represent using lower quality capacitors like the aluminium liquid electrolytic capacitor. Again it can be concluded that capacitors with larger ESR value tend to shorten converter's system time constant and their effect is less prominent on converters designed to operate at higher PWM frequencies. The next figure illustrates the effect of capacitance ESR change on systems damping factor.

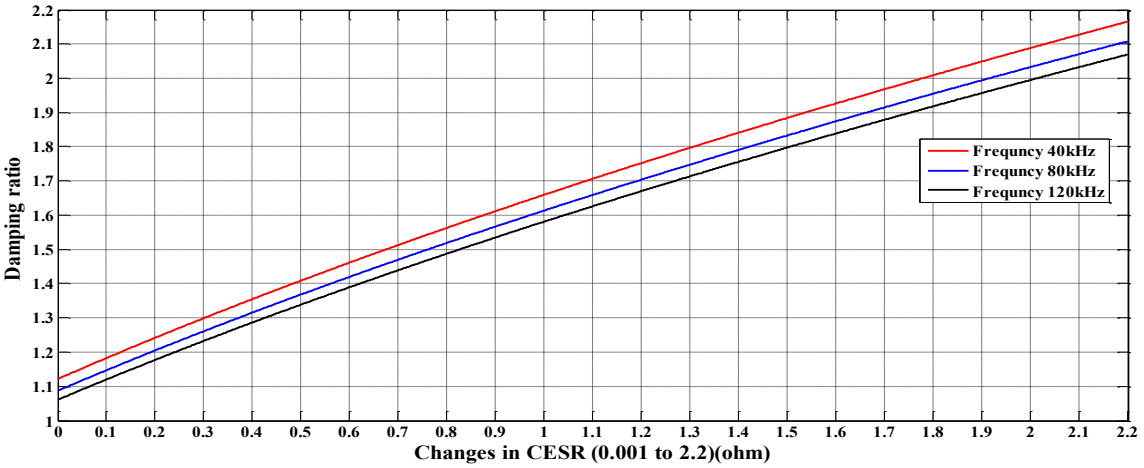


Figure (5.7) The effect of capacitance ESR change on system's damping factor.

From figure (5.7) it can be noticed that as the value of capacitance ESR increases, the value of the damping factor increases as well. The effect of different PWM operating

frequency is small and all three cases response curves are close to each other with lower PWM operating frequencies having the relatively larger change.

Figure (5.8) shows the effect of the variation in capacitance ESR can have on the natural frequency of the converter system.

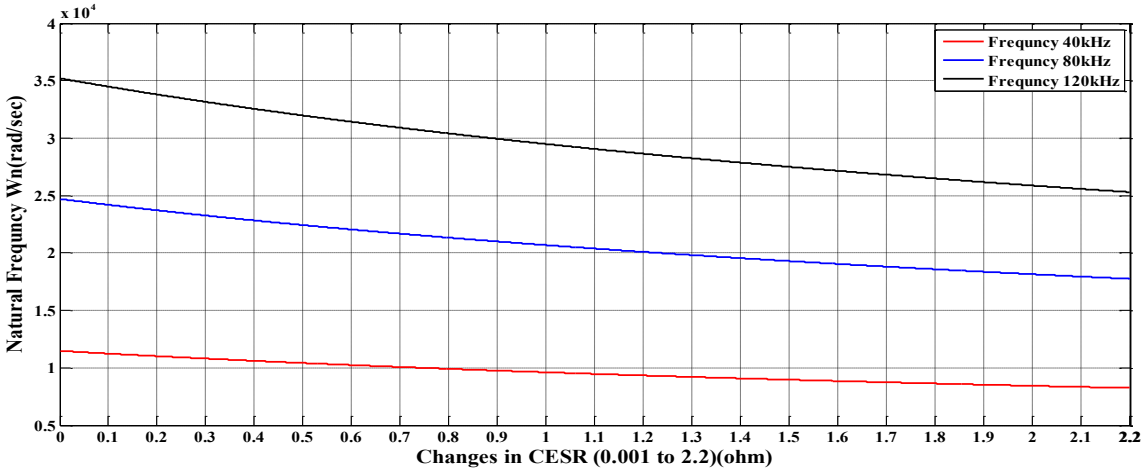


Figure (5.8) The effect the change in capacitance ESR on natural frequency

The impact of larger values of capacitance ESR on converter's system natural frequency is seen in lowered natural frequency, and the effect is more prominent on buck converter systems designed to work at higher PWM frequency as can be seen from the larger curve slope value representing the higher PWM frequency operation.

The next parameter to be investigated is the change in effective series resistance ESR of inductor which can be related to different inductor designed with different wire gauges and types. Figure (5.9) shows how the converter system time constant is being affected by different values of inductor ESR.

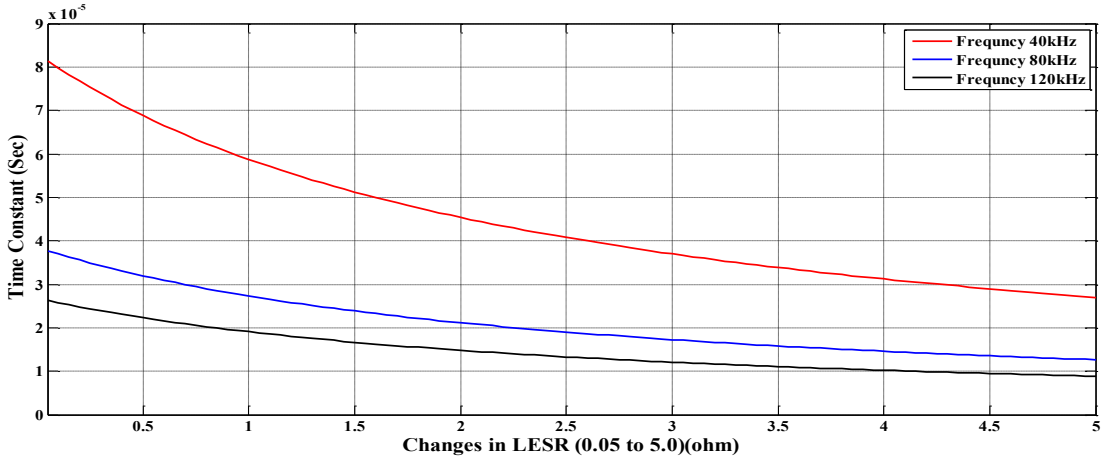


Figure (5.9) The effect of inductor ESR change on converter system time constant.

The increase in inductor ESR has a significant effect on reducing the converter system's time constant. And the effect on converter systems designed to operate on lower PWM frequencies is larger, while the effect on converter operating at higher frequencies is smaller. Figure (5.10) displays the effect the variation in inductor's ESR has on converter system's damping factor.

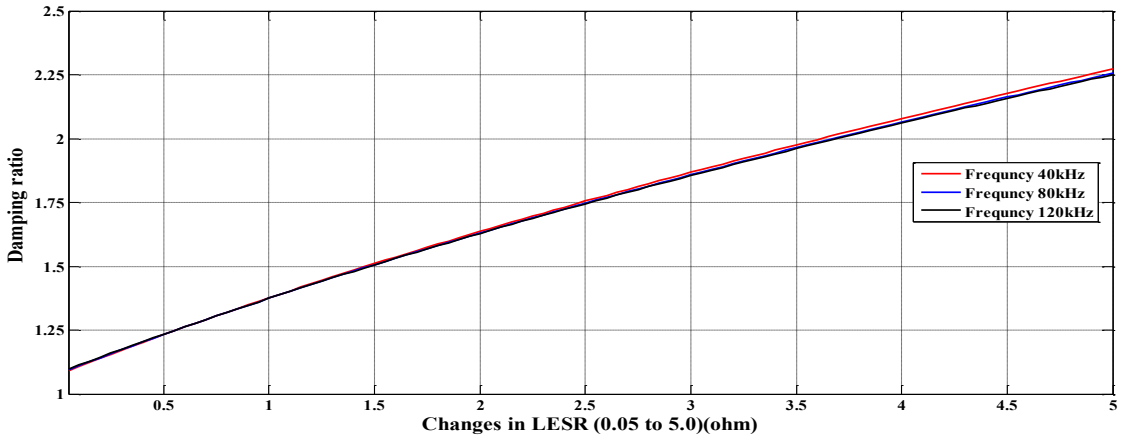


Figure (5.10) the effect of inductor ESR change on converter system damping factor.

On examining figure (5.10) it can be realised that as inductor ESR value increases so does the damping factor and this effect is almost not influenced by changes in the PWM operating frequency of the buck converter circuit. The next set of curves on figure (5.11) shows the effect of increasing values of inductance ESR have on systems natural frequency.

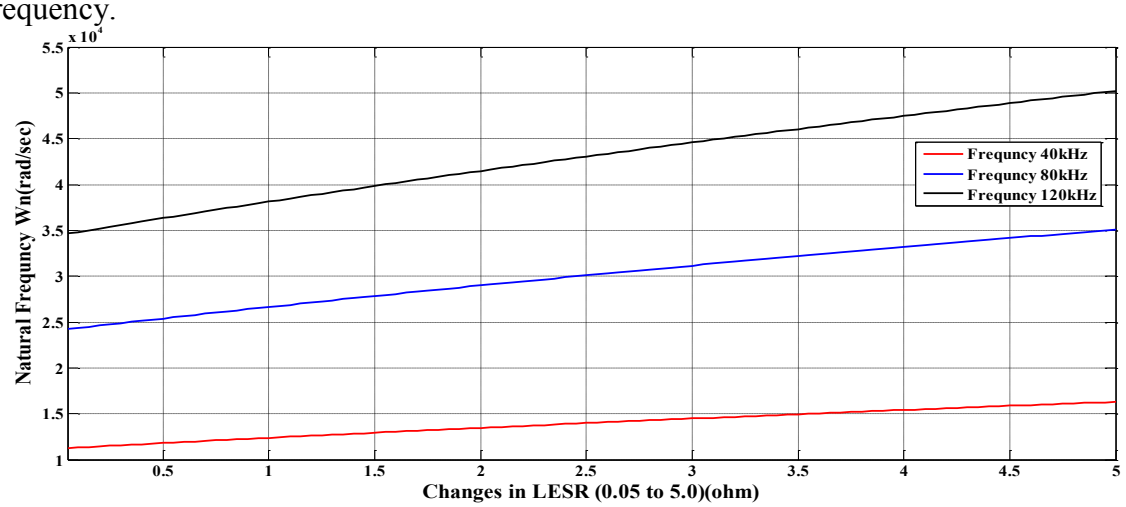


Figure (5.11) The effect of increasing value of inductance ESR on converter system natural frequency.

On looking into figure (5.11), it is evident that the natural frequency of the Voltage converter circuit increases as the inductor ESR does. The effect is more prominent on converter circuits operating at higher PWM frequencies.

To study the open loop stability of the PWM converter circuit which has two prominent poles, a Bode plot for the gain and phase margin is made. Figure (5.12) shows the bode plot of the gain and phase margin of the open loop response of the buck converter circuit.

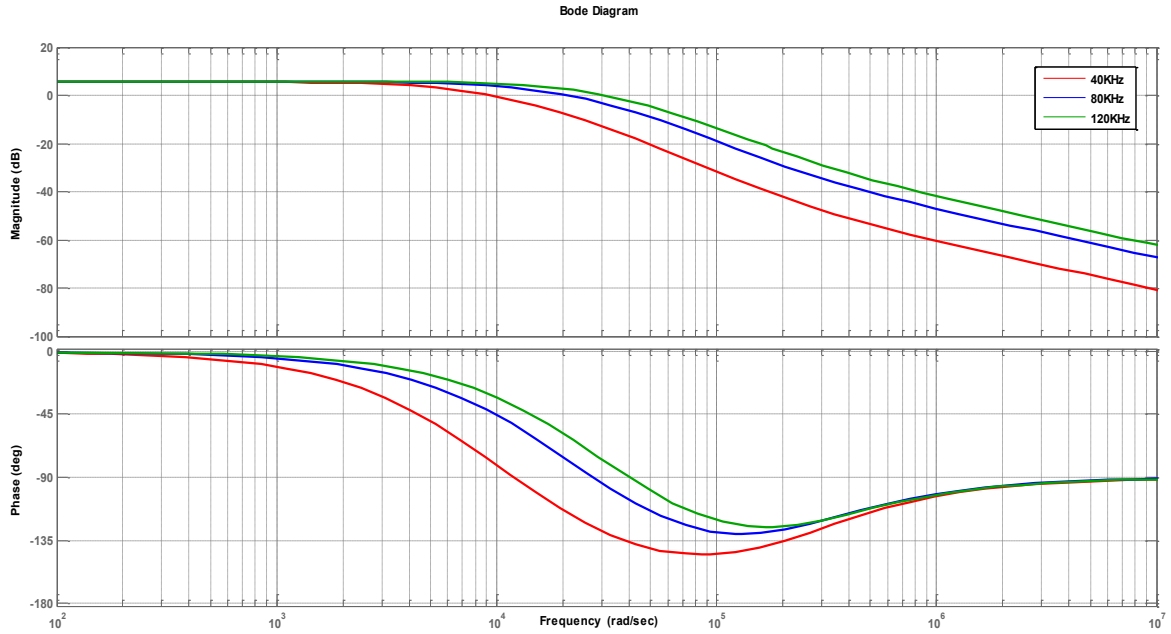


Figure (5.12) Bode plot of the gain and phase margin for the open loop response of the buck converter circuit.

The resulting Bode plot for the gain and phase margins of the converter circuit showed as the input frequency to the system is increased, the resulting output from the system decreases below 0 dB line, also the phase shift increases as the input signal frequency increases. This behaviour indicates that the system under hand is stable.

Next the locations of the poles of the converter circuit are required to be known in addition to investigating the path these poles would follow in order to verify that this circuit in unconditionally stable. This can be achieved by plotting the root-locus of the system as shown in figure (5.13).

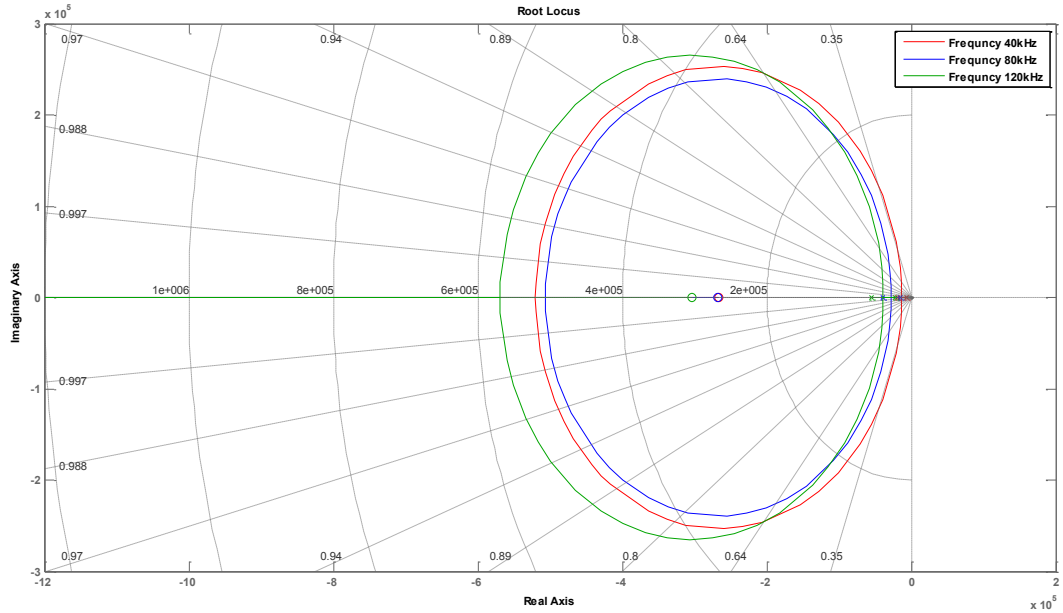


Figure (5.13) The root-locus plot for the converter circuits designed to work at different PWM frequencies.

The obtained root locus shows that the systems being investigated are stable because the circuit poles are on the left side quadrants and each pole is moving towards the zero, otherwise it moves towards infinity.

Finally a step response test for the circuits is carried out, and the resulting time responses are shown in figure (5.14).

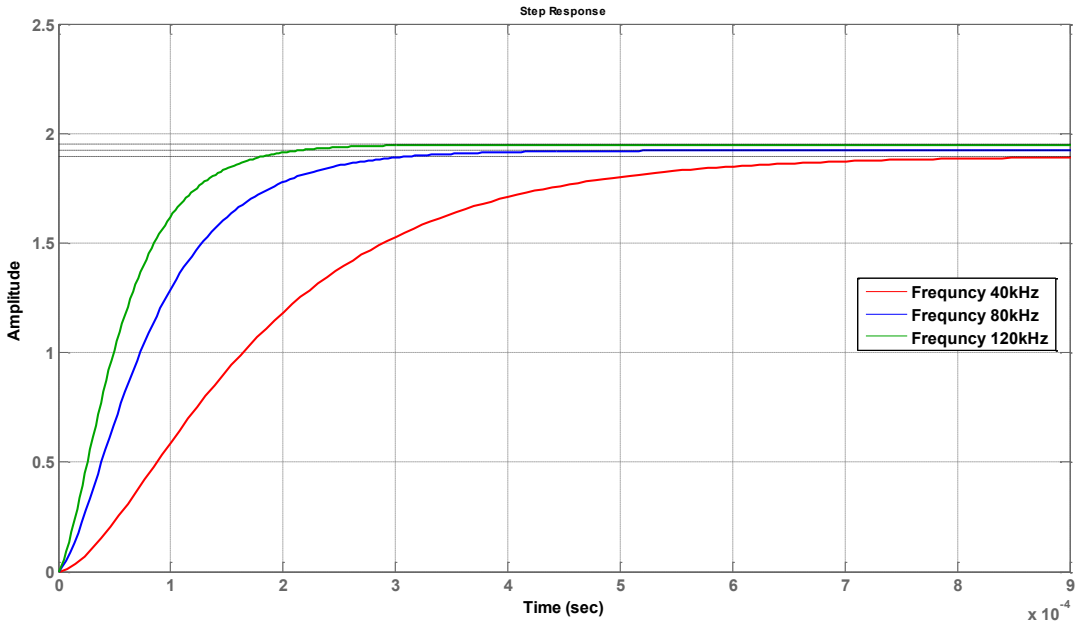


Figure (5.14) The step response for converter circuits designed to work on different PWM frequencies.

Observing figure (5.14) shows that the resulting time response for the tested systems indicates that system response speed increases for circuits designed to work on higher PWM frequencies along that steady state error for circuits designed to work on higher PWM frequencies is smaller than that observed in systems operating at low PWM frequencies.

5.3. Building the Simulation Model

The simulation model is used to conduct large signal analysis and to investigate the operation of the buck converter under closed loop operation and investigate the dynamic behaviour of the synchronous buck converter. Several types of controllers would be tested and evaluated to choose a controller type that suits the intended implementation on a general purpose 8bit microcontroller. Matlab/Simulink software was used for constructing the simulation model and then to evaluate some of the widely implemented control schemes. In this work, the PID controller and the fuzzy logic controller will be examined.

Equations 46 and 52 will be used to construct the function of the converter circuit. Additional elements are added to the simulation module to provide means to carry out tests that will aid in visualizing the performance of the overall circuit and controller combination made by testing its output response to input supply changes and transient load current changes. The extra elements will aid the process of studying the effect of battery voltage drop and any other test condition that is required to measure circuit / controller performance.

Two simulation circuits were constructed; one using a PID controller, and the other using a fuzzy logic controller. Figure (5.15) shows the simulation model built for converter operation with a PID controller, and figure (5.16) shows the simulation model built for converter operation with a PD like FLC, while figure (5.17) illustrates the simulation model built for converter operation with PID like FLC.

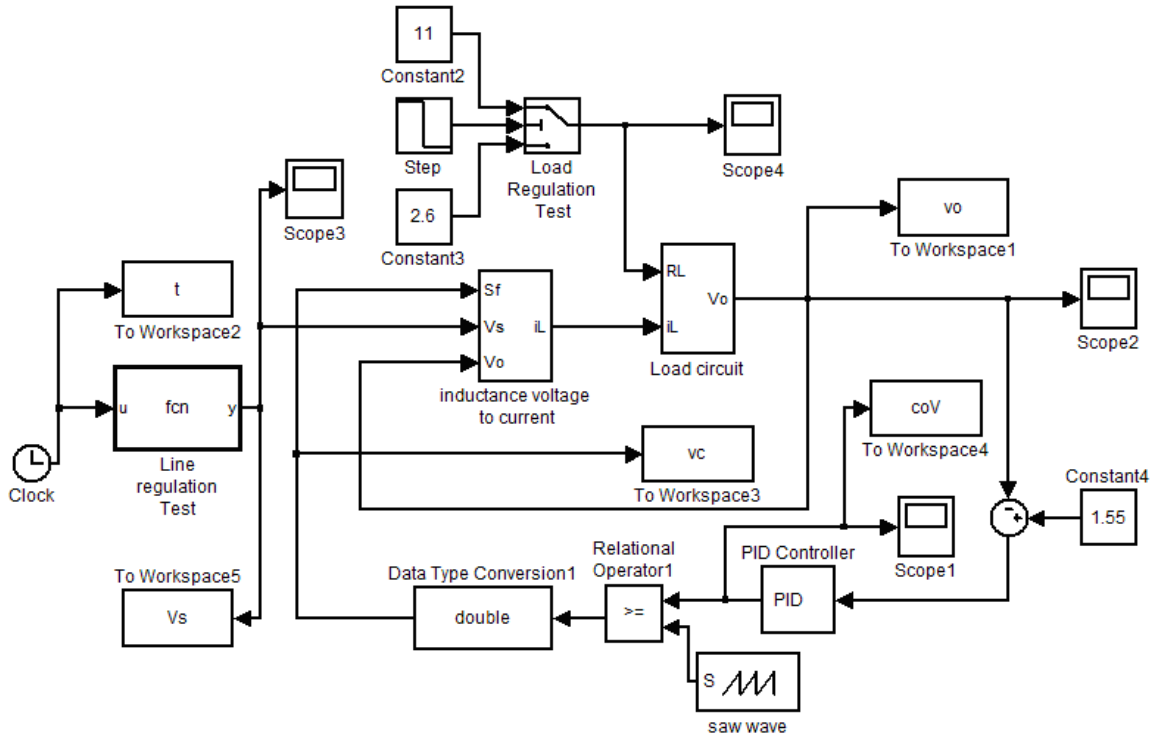


Figure (5.15) The Matlab/Simulink simulation module for the buck converter with PID controller.

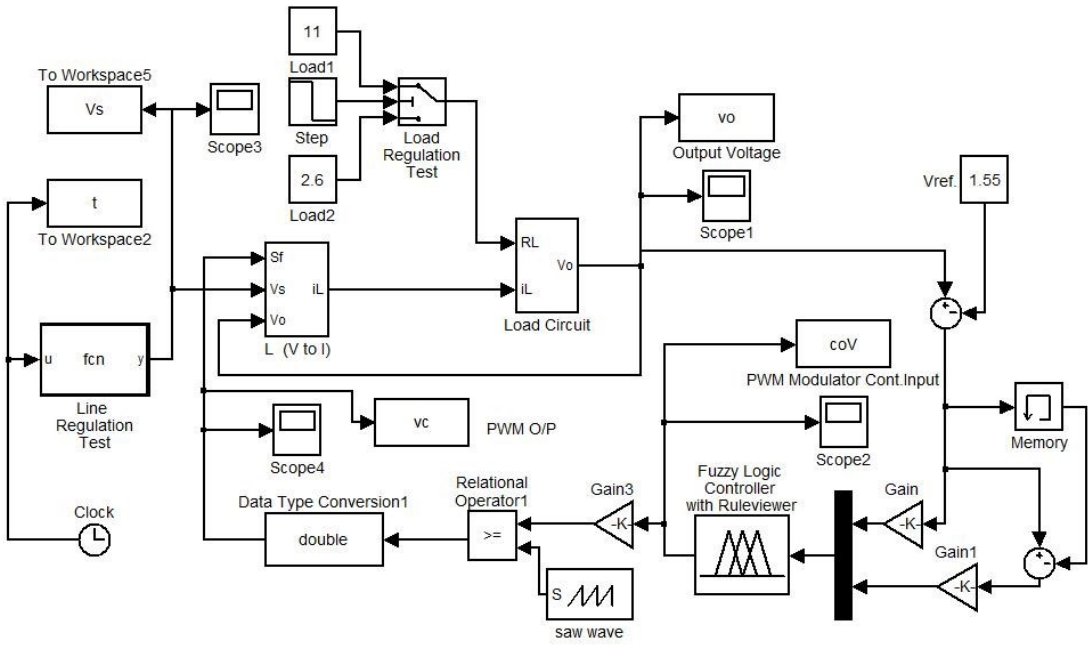


Figure (5.16) The Matlab/Simulink simulation module for the buck converter with PD like fuzzy logic controller.

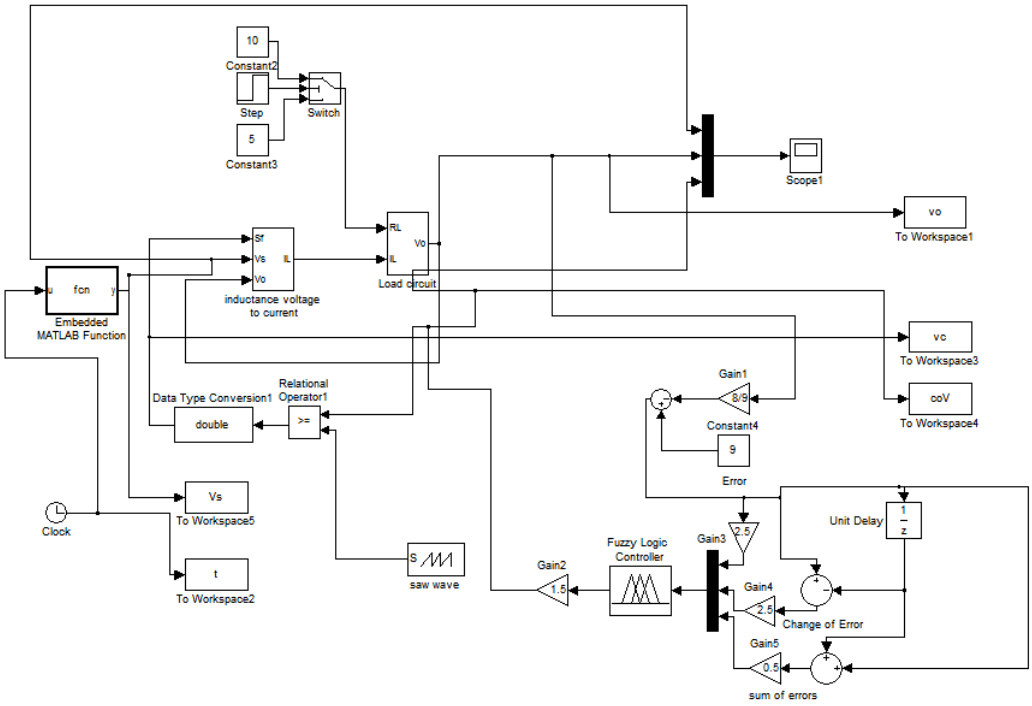


Figure (5.17) The Matlab/Simulink simulation module for the buck converter with PID like fuzzy logic controller

The PID and the PID like fuzzy controller implementation were considered for comparison reason; the performance of the PD like FLC is compared against that obtained from the PID in the process of enhancing the response characteristics obtained from the FLC implementation. The next section describes the fuzzy logic approach and its usefulness in DC-DC converter implementation

5.4. Fuzzy Logic

Fuzzy logic was introduced by professor Lotfi Zadeh in 1965, while contemplating how computers could be programmed for handwriting recognition. This theory has its roots in the previous history of science particularly in logic science.

There are many complex problems in the control field that are difficult to deal with by the conventional approaches, because of system nonlinearities, time varying behavior and imprecise measurement information. Nevertheless, it is quite often observed that human operators can handle these complex problems by their practical experience.

Fuzzy logic control provides a formal methodology for representing, manipulating and implementing a human's heuristic knowledge about how to control a system. Basically it is an artificial decision-maker that operates in a closed loop system in real time. It gathers plant output data, compares it to reference input and then decides what the plant input should be to ensure that the performance objective will be met [69].

The fuzzy logic procedure consists of three parts: input fuzzifcation, input-to-output mapping, and output defuzzification. the block diagram for the fuzzification procedure is shown in figure (5.18). A precise input, such as voltage, current, etc is measured. The input is then fuzzifed by mapping it to a set of input membership functions, through a set of inference procedures. Once the membership to the input functions is determined, the input is mapped to the output membership functions according to a rule base. The rule base is unique to the system and based on expert knowledge. The degree of belonging to the output membership functions is determined and is used to produce a precise output through defuzzifcation or another inference procedure.

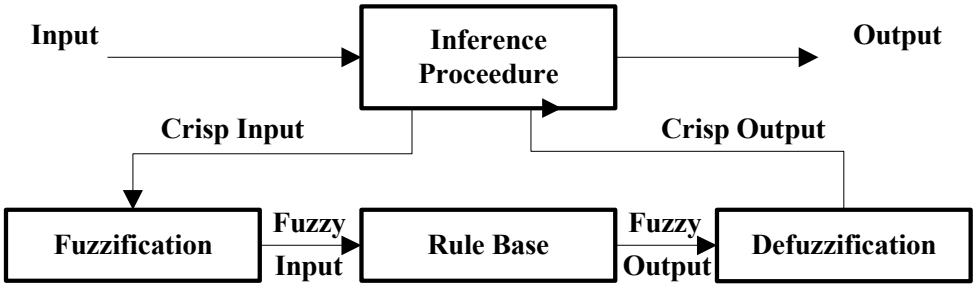


Figure (5.18) The fuzzy logic procedure.

The unique feature of the fuzzy logic is its use of linguistic variables instead of numerical variables to determine relationships. For example, the variables used within this thesis to express the error voltage are given the names "Negative Big (NB)", "Negative Medium (NM)", "Negative Small (NS)", "Zero (ZE)", "Positive Small (PS)", "Positive Medium (PM)", and "Positive Big (PB)". In order to determine which category the input belongs to, membership functions are defined in order to show the degree of belonging to each particular variable.

Membership functions are graphical mapping tools used to determine how much something belongs to a certain group. A membership function can have any arbitrary

shape, but the most often used membership function comes in one of the following shapes: piecewise linear (triangular or trapezoidal), quadratic, Gaussian, or conforming to a special function. The most common shape for the membership function is the triangular and is generally appropriate to cover most of the application successfully.

The fuzzification process: the input data (crisp data) is fuzzified according to the membership function. The membership function maps the crisp input *x* into the corresponding amount of membership. The fuzzified input is the degree to which each part of the antecedent has been satisfied for each rule. The implemented fuzzification method will cover only the shapes which are symmetrical around a central value. It can be expressed as follow:

$$\mu_A(x) = H \cdot \left(\frac{x-b}{a} \right) \qquad \ldots(70)$$

This relation will transfer the crisp input into fuzzy input.

The inference procedure is one of the important operations in a fuzzy system it determines the degree of correlation between the rules and the input to the fuzzy system. In order to understand this procedure the fuzzy operation and the rule base need to be clarified. In common applications membership functions usually overlap necessitating the need to define a set of rules for the interaction of the membership function within a fuzzy set. The basic sets of operation are: union, intersection, and complement. An example can be given to aid explanation, if A and B are fuzzy sets in the universe of discourse U over the entire range of possible input values x with membership functions μ_A and μ_B.

- Union operation: The membership function $\mu(A \cup B)$ of the union $A \cup B$ is defined for all $x \in U$ by: $\mu(A \cup B)(x) = \max(\mu_A(x), \mu_B(x))$.

- Intersect operation: The membership function $\mu(A \cap B)$ of the intersection of $A \cap B$ is defined for all $x \in U$ by: $\mu(A \cap B)(x) = \min(\mu_A(x), \mu_B(x))$.

- Complement operation: the membership function of the complement $\mu_{\bar{A}}$ of the fuzzy set A is defined for all $x \in U$ by: $\mu_{\bar{A}} = 1 - \mu_A(x)$.

Figure (5.19) represents these operations using triangular membership function as an example.

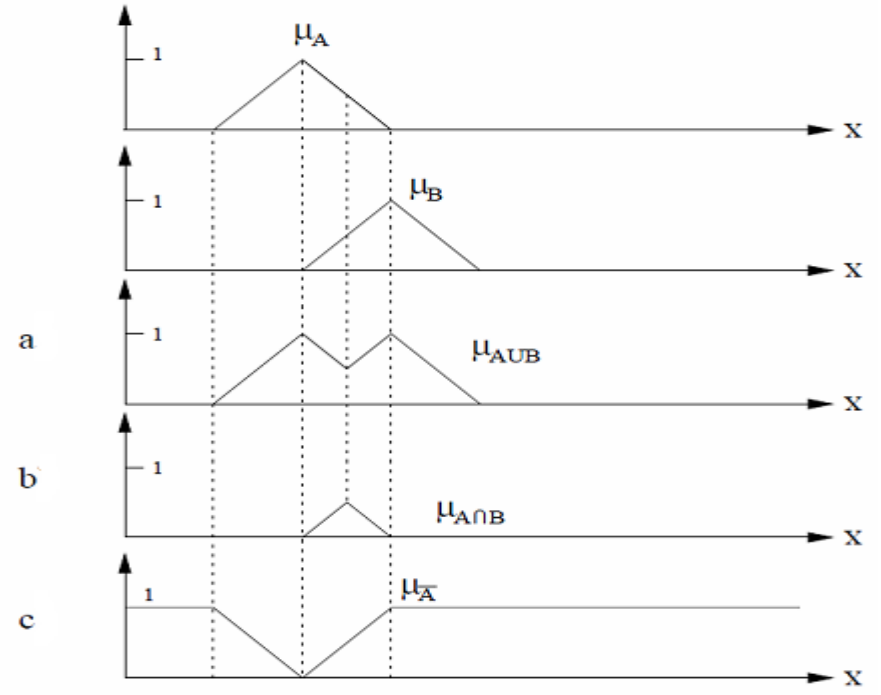


Figure (5.19) the graphical representation of the fuzzy operations; a(union), b(intersection), c(complement)[69].

Fuzzy rule sets are used to mapping the fuzzy input to the output. The definition of these sets requires expert knowledge of the system under hand. It usually follows a specific structure like (if…then). The principle can be clarified by an example, the following rule base is given as:

If x is A and y is B, then z is C

Where x, y, and z are fuzzy variables and A, B and C are fuzzy subsets corresponding to the universe of discourse of X,Y,and Z respectively. If there are n rule bases they will be defined as:

Rule1: if x is A1 and y is B1 then z is C1

Rule 2: if x is A2 and y is B2 then z is C2

⋮

Rule n: if x is An and y is Bn then z is Cn

The rule base R is defined as the union of the individual rules. Fuzzy rule-based control systems are similar to expert systems in that the rules embody human expert knowledge about the control operation that is being mechanized. The way of implementing the control rules depends on whether or not the process can be controlled by a human operator. If the operator's knowledge and experience can be explained in words, then linguistic rules can be written immediately. If the operator's skill can keep the process under control, but this skill cannot be easily expressed in words, then control rules may be formulated based on the observation of operator's actions in terms of the input-output operating data [36,37,38,39].

In the case of the work in this thesis the fuzzy logic controller is used to control the operation of a PWM controlled buck converter. The construction of the fuzzy control rules is heuristic and is built following the criteria described below:

- If the output of the converter is far from the set point, the change in duty cycle must be large in order to bring the output to the set point value quickly.
- If the output of the converter is approaching the set point value, a small change in duty cycle is required.
- If the output of the converter is near the set point and is approaching it rapidly, the duty cycle is kept constant in order to prevent overshoot.
- If the set point value is reached and the output is still changing, the duty cycle must be changed a little bit in order to prevent the output from moving away from set point value.
- If the set point is reached and the output is steady, the duty cycle must remain unchanged.
- If the output is over the set point, the sign of the change in duty cycle must be negative. Conversely if the output is under the set point value the change in duty cycle is positive.

These are the elements of the knowledge base that is used to construct the fuzzy rule set of the designed FLC.

The PD like FLC is chosen for this work in order to reduce calculation overhead which is a requirement for implementing the controller on the selected platform [36,37,].

The equation for a conventional PD-controller is given by:

$$u(k) = K_P \cdot e(t) + K_D \cdot \Delta e(t) \qquad \text{……..(71)}$$

Where u is the control signal K_P is the proportional gain factor and K_D is the derivative gain factor, e is the error and Δe is the change in error.

From this equation it can be noticed that the control signal (u) is calculated for any pair of error (e) and the change in error (Δe). Then the PD like fuzzy controller will consist of a rule set having the following structure:

If the value of error is < linguistic value>and the value of change of error is < linguistic value > then the value of control output is < linguistic value >. The linguistic value is given expression like small, medium, large, or the like.

The fuzzy rule set constructed for this work has used seven linguistic fuzzy sets. On selecting a smaller rule set of five, it did not give acceptable system response. While using larger number of linguistic rules improves the function of the controller but at the expense of larger memory requirements and longer processing time that may require a fast micro controller to implement. Table (5.1) shows the fuzzy rule set used in controller design.

Where NB,NM,NS,ZE, PS, PM, PB are the seven fuzzy sets chosen and defined for the error E and the change in error ΔE:

NB: negative big

NM: negative medium

NS: negative small

ZE: zero equal

PS: positive small

PM:Positive medium

PB: positive big

Table 5.2: The fuzzy rule set implemented in the designed FLC

ΔE \ *E*	*NB*	*NM*	*NS*	*Z*	*PS*	*PM*	*PB*
NB	*NB*	*NB*	*NB*	*NM*	*NM*	*NS*	*Z*
NM	*NB*	*NB*	*NM*	*NM*	*NS*	*Z*	*PS*
NS	*NB*	*NM*	*NM*	*NS*	*Z*	*PS*	PM
Z	*NM*	*NM*	*NS*	*Z*	*PS*	PM	PM
PS	*NM*	*NS*	*Z*	*PS*	PM	PM	PB
PM	*NS*	*Z*	*PS*	PM	PM	PB	PB
PB	*Z*	*PS*	*PM*	PM	*PB*	PB	PB

The defuzzification process: The task of defuzzification is to map the fuzzy output from the universe of discourse to a crisp output. There are several defuzzification strategies, each provides a means to choose a single output based on the implied fuzzy sets. The input for defuzzification is the fuzzy set and the output is a crisp number. The most common methods for defuzzification are :

1- The mean of maximum method.

2- The maximizing decision method.

3- The centre of gravity method.

The third method is the most popular one used for defuzzification and is followed in the work done in this thesis for its simplicity.

A crisp output U is computed using the centre of gravity method [38,39].

$$U = \frac{\sum_{i=0}^{N} \mu(u_i).u_i}{\sum_{i=0}^{N} \mu(u_i)} \quad \ldots.(72)$$

Where N is the number of the used intervals, μ_i is the degree of membership of every output variable corresponding to each error and change of error groups. U is the crisp output of the controller. The Matlab fuzzy tool box is used in performing the calculations for the crisp output.

Figure (5.20) shows the fuzzy rule set of the FLC used in the simulation model

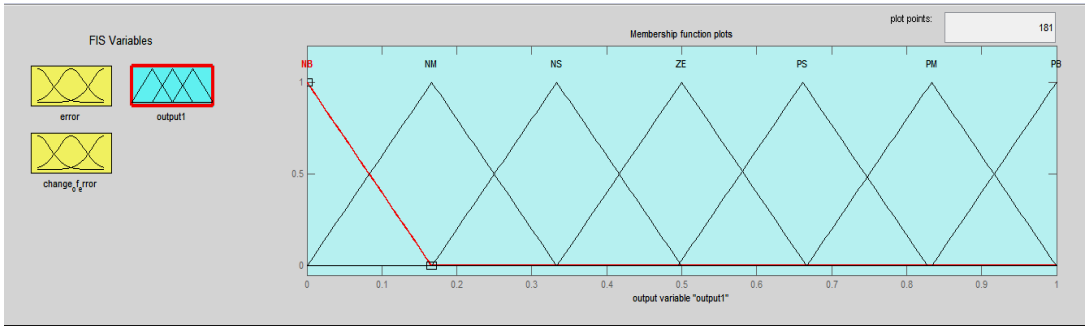


Figure (5.20) The membership function of the fuzzy rule set used in the FLC design

Figure (5.21) shows the Control surface obtained from implementing the fuzzy rule set table shown in table 5.2.

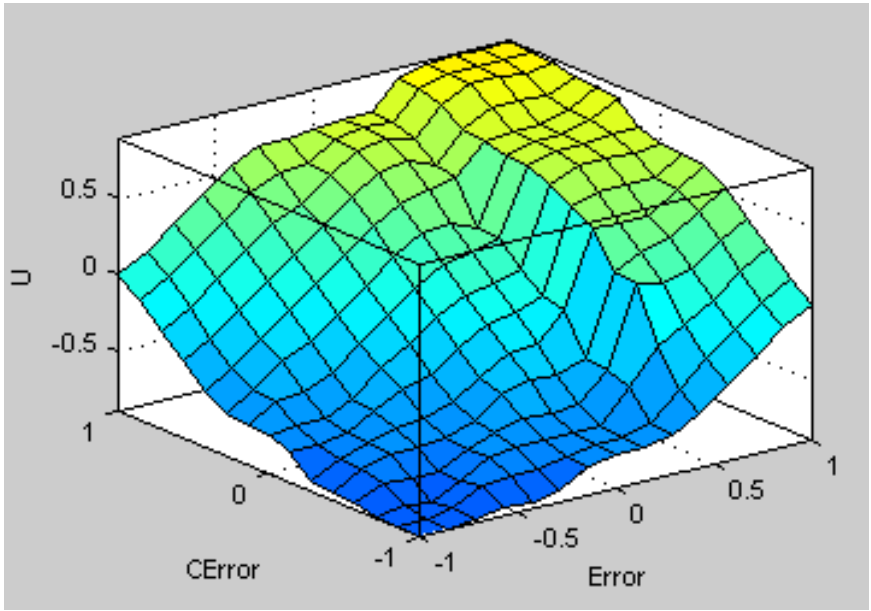


Figure (5.21) The control surface obtained from implementing the Fuzzy Rule Set Table 5.2.

5.5. Simulation Results

In this section some of the final results obtained for the simulation modules built are shown in the following figures.

The PID simulation module was automatically tuned using the Ziegler-Nichols method provided inside the PID control block. It should noted that there are several tuning methods for the PID controller other than the Ziegler-Nichols and Tyreus-Luyben method, there is the Cohen-Coon method which has resulted in identical outcomes in the PID performance. The FLC was tuned experimentally using trial and error.

Figure (5.22) shows the transient response of the PD like FLC during early test, it can be seen that while the desired output was set to 1.55 volts, the actual output settled at 1.58 volts which means that here was a steady state error of 0.03 volts.

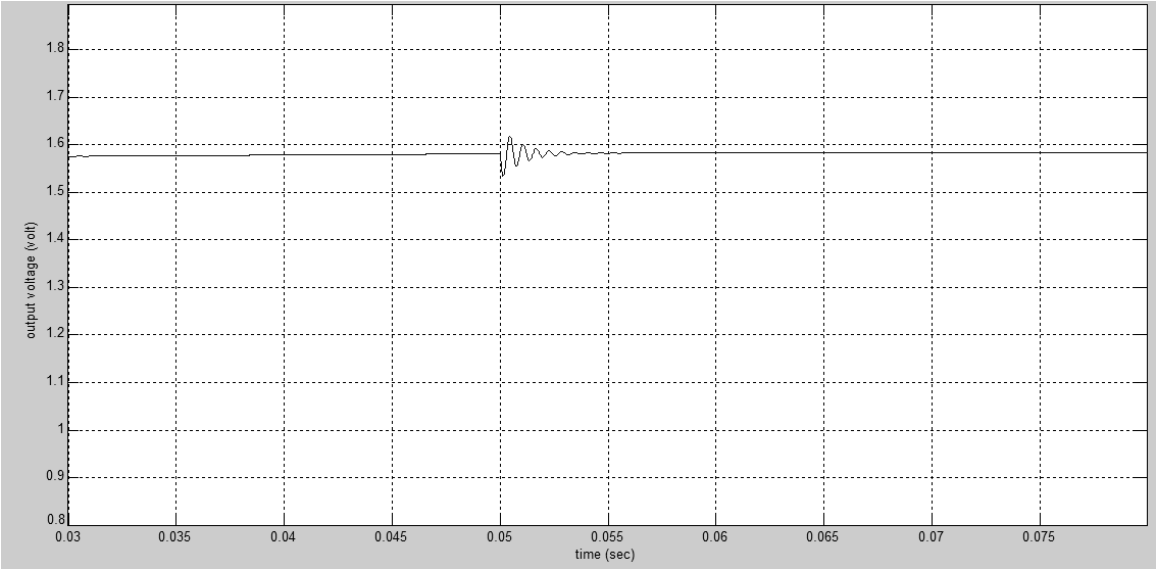


Figure (5.22) The response of the PD like FLC to 50% step increase in load at early tuning stages.

Next figure (5.23) was obtained from final tuning stages taken from experiments done on the tuned PID model and the PD like FLC in transient response to load changes, the controllers were subjected to load changes from light load (CPU core idle I_{Load}=167mA) to heavy load (CPU core full activity I_{Load}=597mA) as this would be the worst case condition expected by real life applications.

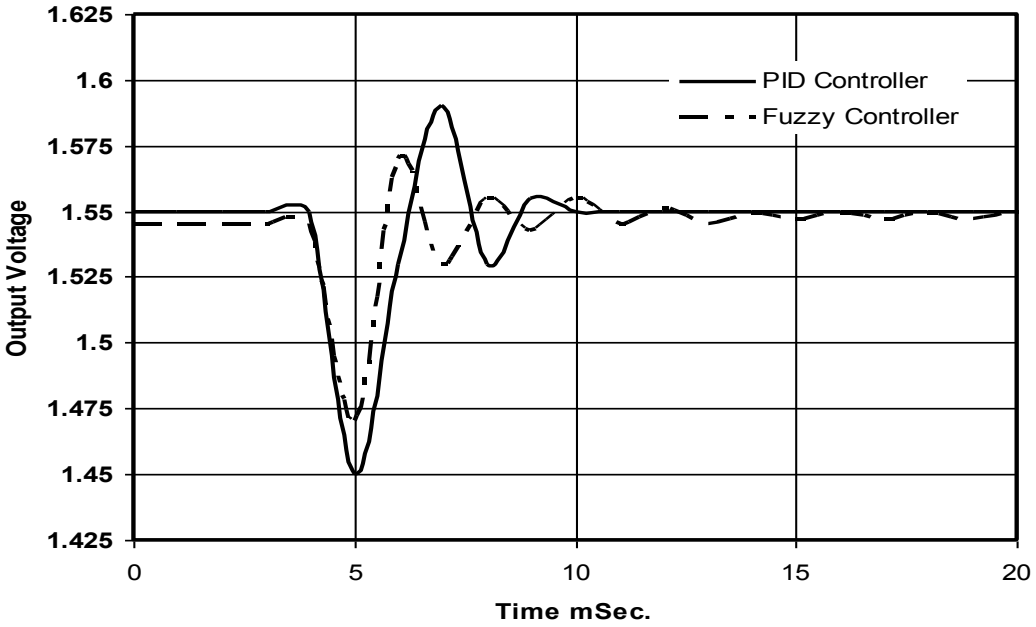


Figure (5.23) The transient response of the PID and FLC Controllers for a step change in load current from 167mA to 597mA representing light load to full load operation of the target processor core.

The same test was repeated but with the step in current moving from high load of 597 mA to light load of 167mA.

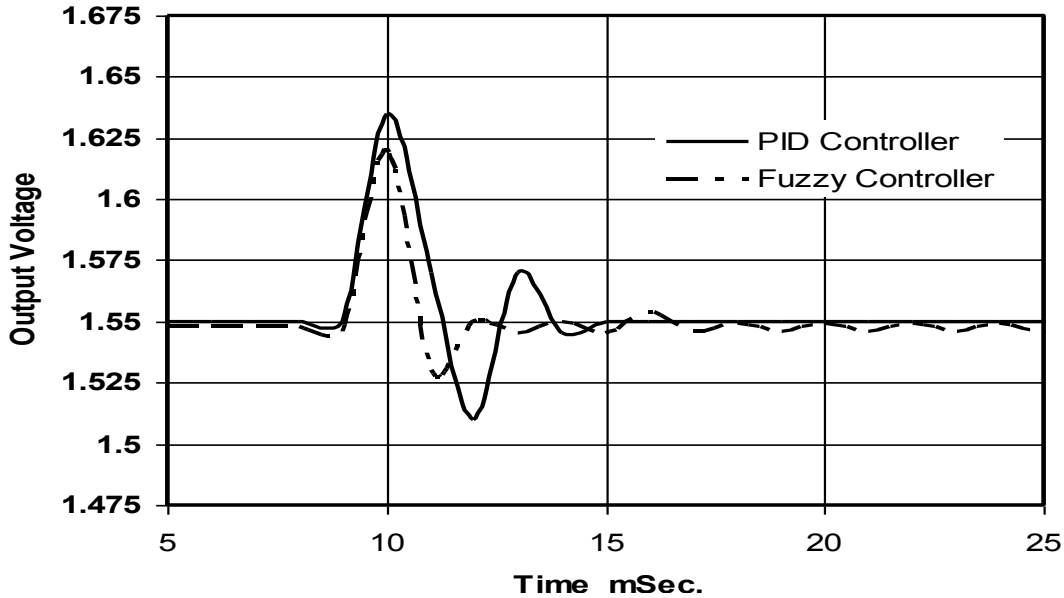


Figure (5.24) The transient response of the PID and FLC Controllers for a step change in load current from 597mA to 167mA representing light load to full load operation of the target processor core

The following differences were observed: the PID controller was tuned to have response characteristics that make the end response fast with an overshoot that would be lower than the limit set by the processor manufacturer. The resulting controller had an overshoot of about 6.5% form the steady state output. It was within the allowable limits set by the target load electrical specifications [43]. Steady state output was reached after 4.6milliSeconds and there was no measurable error in steady state output. The fuzzy controller had a Lower overshoot that was 4.8% of the output and reached steady state after about 4.75 milliseconds and had a steady state error figure of less than 0.3%. From these results, it can be concluded that:

- The Fuzzy controller had a little slower response than the PID controller.
- The Fuzzy controller had smaller overshoot than the PID controller.
- The Fuzzy controller had a small steady state error while the PID controller showed no steady state error.

5.6. Chapter Summary

This chapter contains the mathematical analysis carried on an equivalent circuit for the pulse width modulated buck converter section of the smart voltage regulating module. A mathematical model was derived for the equivalent circuit and then standard analytical procedure was carried out using Matlab program and the obtained results were analyzed and found that the system under hand is essentially stable. A simulation model was built using Matlab/Simulink to test a PID controller simulation against a PD like FLC and results obtained were compared and a conclusion was reached that PD like FLC can be implemented on the selected platform, control the PWM buck converter, and deliver the response that conforms with target load requirements.

Chapter Six

Experimental Work

6.1. Introduction

This chapter covers the experimental work done on the design of the smart VRM. It will include the circuit design, circuit assembly work, the microcontroller programming, and the lab work done to verify and measure the working parameters of the accomplished design.

6.2. The VRM Circuit Design

In this section the design of the VRM is explained. The design has followed the methodology explained in Chapter three and four. Figure (6.1) shows the steps followed in designing the target Circuit.

The process of designing the target System started with component selection which was based on the knowledge acquired about modern semiconductor devices, new passive components with advanced specifications, low power micro controllers, advance drive circuits for power switching devices.

Most of modern electronic circuit components and passive components are supplied in small outline packages intended for surface mounting on PCB that are prepared for wave soldering technique.

These components are not suitable for prototyping on bread board where changes can be made easily during the experimenting and testing phase. For this reason small printed circuit boards were designed and manufactured to accommodate the discrete electronic components and offer suitable extensions that promotes their implementation on prototyping bread board. Figure (6.2) shows the PCB design for these adapter boards along with picture of the assembled ones.

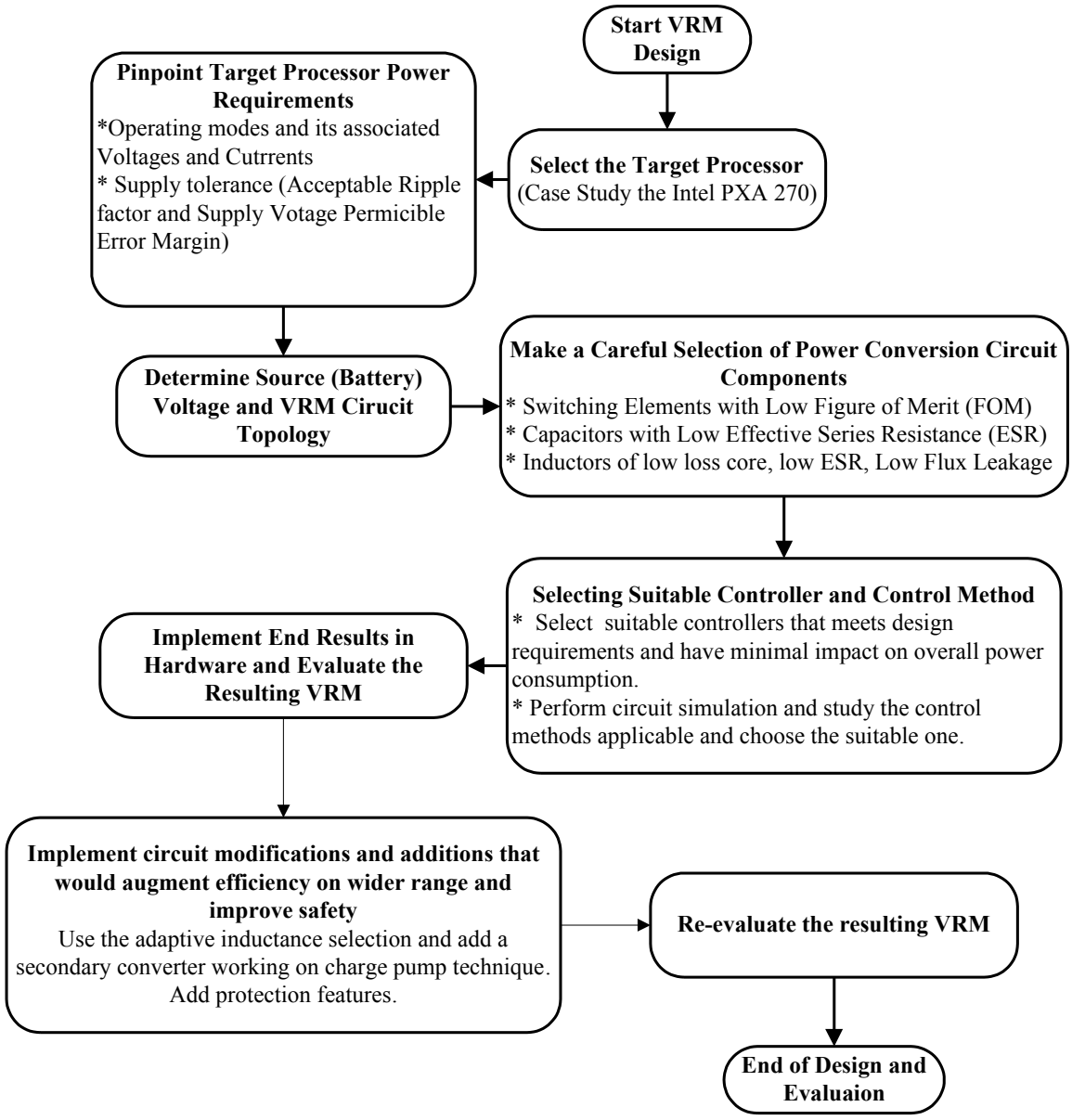


Figure (6.1) Steps followed during the course of designing and implementing the smart VRM system.

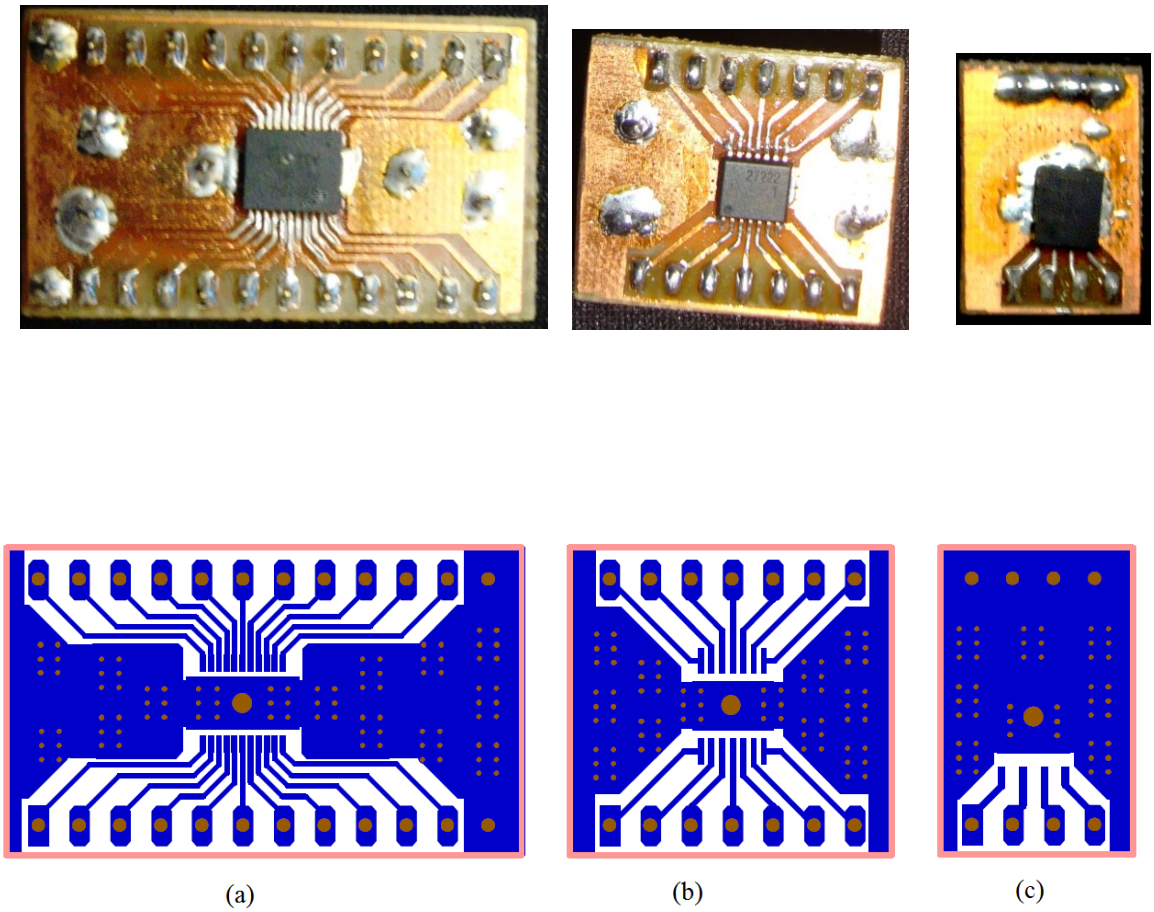


Figure (6.2) PCB design of adapter boards and their assembled pictures

6.2. 1. Design Components Selection

In this sub section a description for the selected components is given. The selection process included passive and active components.

The search for active components started with MOSFET devices. The search included several products from several manufacturing firms like the HEXFET series from International Rectifier like the IRF6609 [a], the OPTIMOS series from Infineon like the BSC046N02KS [b], and the Texas Instruments NEXFET series like the CSD17312Q5.

The choice was made regarding their ON resistance and switching losses for the PWM control MOSFET and the synchronous rectifier MOSFET. While the Switching devices

used for adaptive inductor selection were chosen regarding their ON resistance only since their switching rate is very low compare to the ones mentioned before.

Upon this selection criterion, the NEXFET series [70] from TI showed the most promising characteristics where the CSD17305Q5A [71] and CSD16321Q5 [72], are chosen for the PWM control device and Synchronous rectifier device respectively. The CSD16401Q5 [73] was chosen for the adaptive inductor selection switches for its very low on channel resistance.

The UCC27222 [63] was selected for the predictive delay gate drive device as its implementation promises better efficiency as it adapts a method that eliminates cross current conduction and body diode forward biasing.

Next, the passive devices selection is covered. The capacitors in search for were to be characterized by low ESR value along with higher temperature ratings and tighter tolerance. Capacitors and inductors from several manufacturing firms were examined for their characteristics. Manufacturing firms like Taiyo Yuden, Panasonic, TDK, NIC, and AVX were searched for the product required. Three types of capacitors were selected for the purpose of testing the effect of their rated ESR figure on designed converter ripple read outs. The experimentation was done using tantalum capacitor with conductive polymer cathode the NTP686M6.3TRB(55)F from NIC corporation [74], niobium capacitor the NOSC686M006R0200 from AVX corporation [75], and an aluminium solid electrolytic capacitor the AFK686M16D16T-F from Cornell Dubilier electronics [76]. TPSD226K035R0125 22µF low ESR tantalum capacitor from AVX is used for input capacitor.

Inductors selected were NPIS3P470MTRF and the NPIS2P330MTRF from NIC Corporation [77], and LMXS131JM220FTAS from AVX [78]

The basic Converter circuit used the 47µH inductor from NIC with the low ESR tantalum Capacitor.

The choice of microcontroller was to be made from the low power 8bit category while keeping in mind the required integrated peripheral devices, the performance required to accomplish the desired control action, and the size of memory needed to accommodate

program and data. Microcontrollers from Atmel® and Microchip® were considered and the selected microcontroller was the PIC16F1509 from Microchip for having the needed peripheral devices operating at the required performance and the overall power consumption of the device was lower than its Atmel counterpart. Figure (6.3) shows the block diagram of the needed peripheral devices of the PIC16F1509.

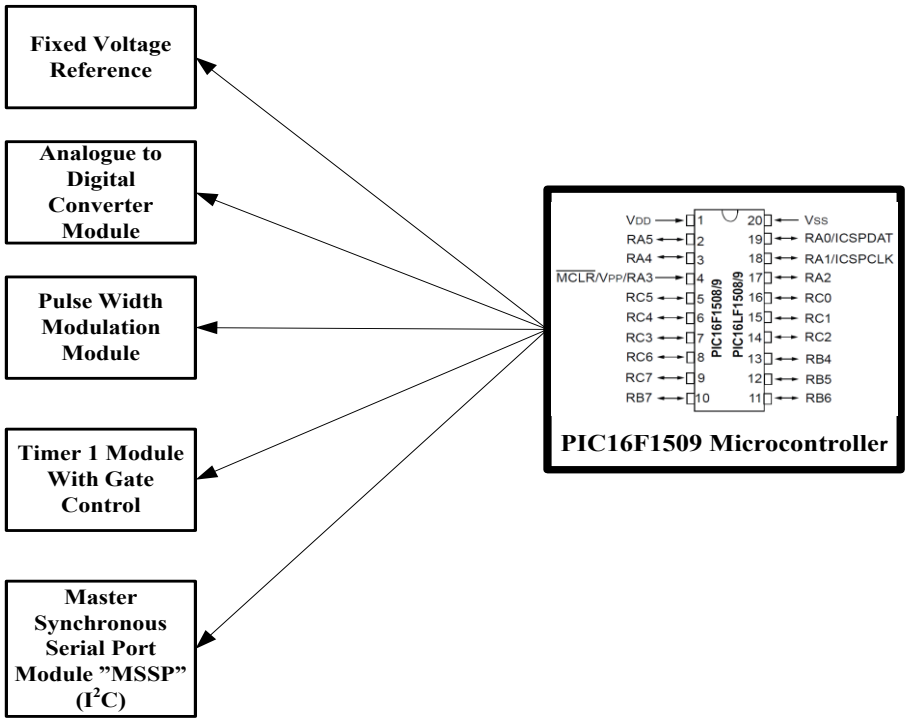


Figure (6.3) The PIC16F1509 peripheral devices needed in smart VRM design

While in the initial experimentation stage, the VRM circuit was assembled on a bread board to ease component replacement, figure (6.4) shows the circuit diagram of the basic converter.

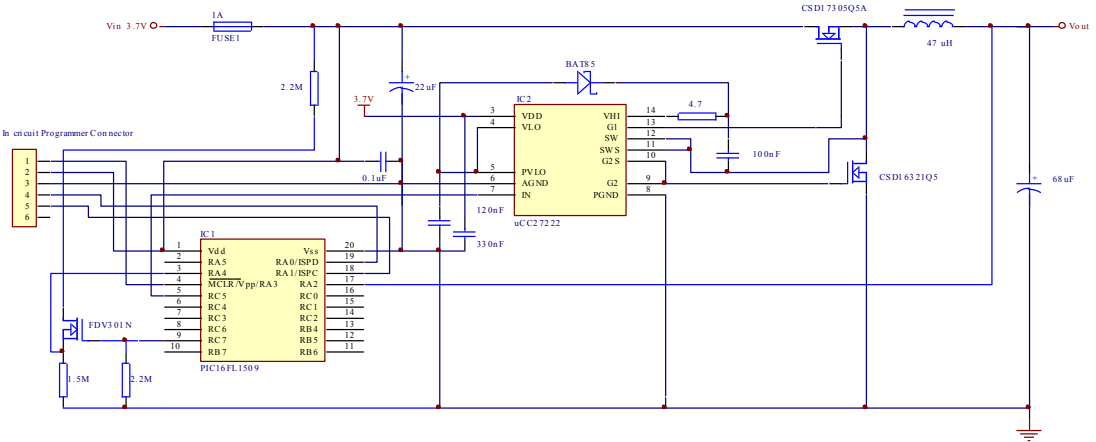


Figure (6.4) The circuit diagram for the buck converter section with microcontroller.

6.2. 2. Experimental Work on the Designed VRM

This circuit was assembled on bread board and connected to the test setup arranged to carry out tests and measurements on the designed system the test setup consisted of the following equipments:

- Tektronix TDS2004 digital storage oscilloscope with 1GHz Sample rate with 4 input channels.
- HAMEG HM8012 digital multimeter with 4¾- digit display. Four units were used in the experimental setup.
- HAMEG HM8040-3 power supply with three outlets one fixed and two variable outputs. This power supply was used to power the auxiliary circuits required to conduct the experiments.
- KIETHLEY Model 2304A high speed power supply. This unit is a precision power supply digitally controlled with digital readouts of current and voltage. It also incorporates a programmable current limiting function.
- PICKit 3 is an in-circuit programming tool for the PIC microcontroller family.
- A Windows based Computer with MPLAB- X software installed.

Figure (6.5) shows the test setup for conducting the tests on the designed power module.

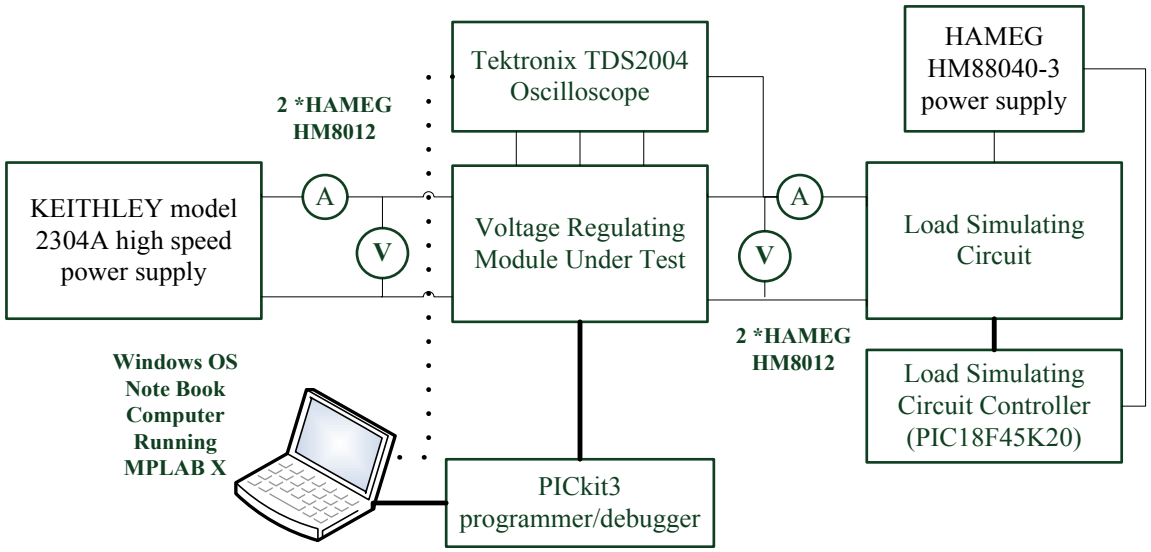


Figure (6.5) The test setup for conducting experiments on the designed VRM module.

Figure (6.6) shows a picture of the test setup and the prototyping board on which the preliminary converter circuit is constructed.

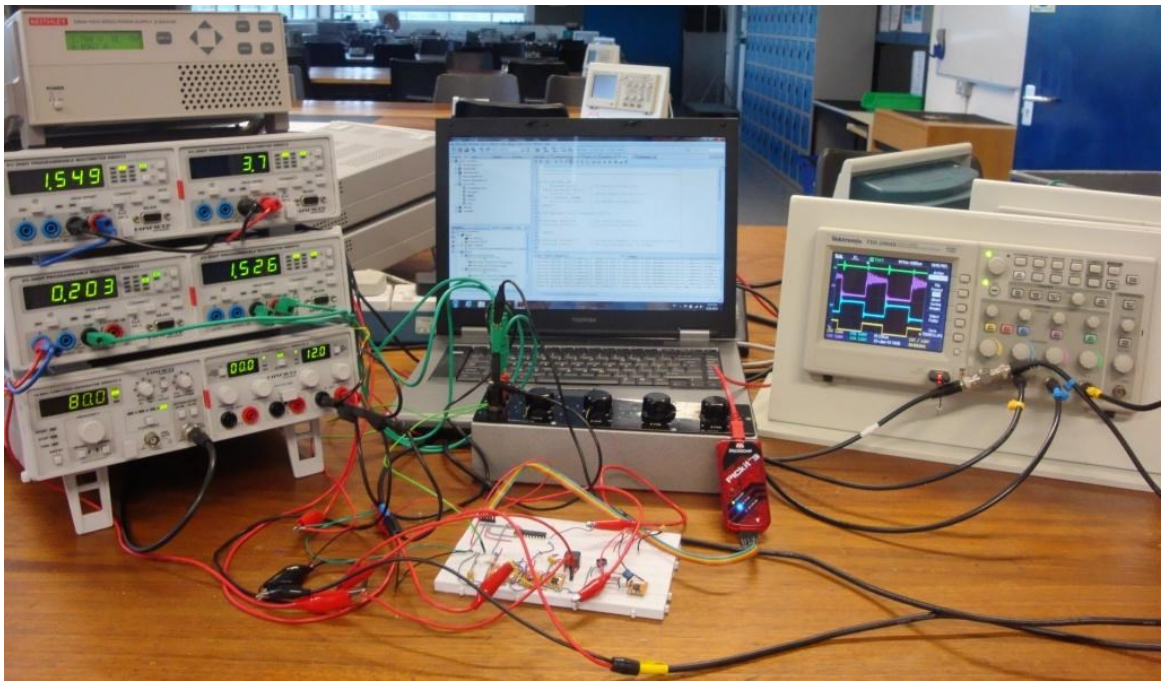


Figure (6.6) Picture of the test setup and the prototyping board of the designed buck converter circuit of figure (6.4)

It is important to notice that the arrangement of ammeters is to exclude the amount of drop in voltage on the ammeter from being included in the power measurement knowing that output voltage can be as low as 0.85 volts. So at the output side of the converter, the ammeter is included in the load subjected to the converter, effectively it will have no contribution measurement error due to internal measuring equipment resistance. Conversely at input the voltage drop on the ammeter is excluded from the measurement of input voltage to the converter.

Before discussing the test results obtained, table 6.1 shows the power losses calculated for the implemented components using figures from component datasheets and the methods reviewed in chapter 3 and 4. It also includes the resulting expected operating efficiency of the converter.

Table 6.1: Power loss calculations for the designed VRM

V_{IN}=3.7 Volts, V_{OUT}=1.55 Volts, P_{LOAD}=925mWatts, F_{PWM}=78.12KHz	
Component	Power loss
MOSFET Switch CSD17305Q5 (Gate charge losses + Conduction losses)	5.308mWatts
MOSFET Sync. RECT. CSD16312q5 (Gate charge losses + Conduction losses)	4.714mWatts
Inductor L (ESR=20.02mΩ)	6.724mWatts
Capacitor C (ESR=55mΩ)	4.52mWatts
Gate Driver UCC27222	15.6mWatts
RISC Microcontroller PIC16F1509	55.21mWatts
Total Loss	73.569mWatts
Efficiency	90.94%

The expected efficiency of the designed converter is about 91%, when this converter was put to test under real working conditions the resulting maximum efficiency of the system has been measured to reach 89.6 % as can be seen in the measurements conducted and documented in appendix A.

The conducted tests showed the empirical results for the relation between the operation parameters of the buck converter

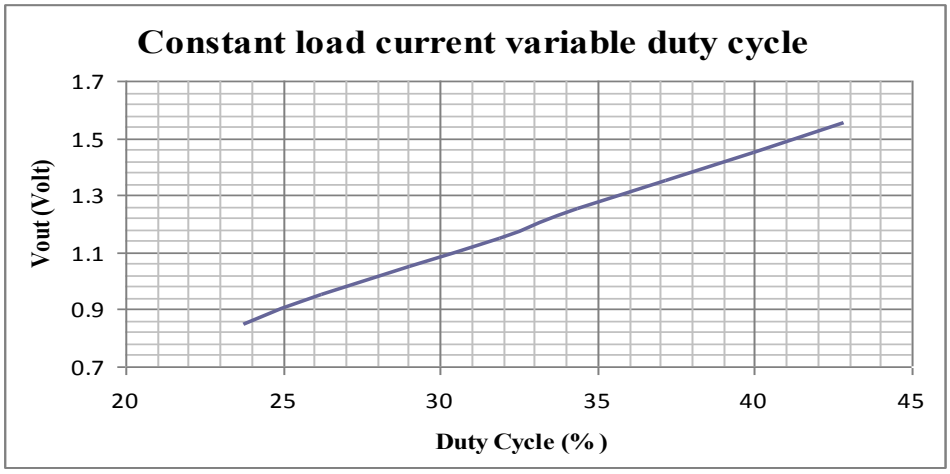


Figure (6.7) The relation between duty cycle and output voltage at constant output current.

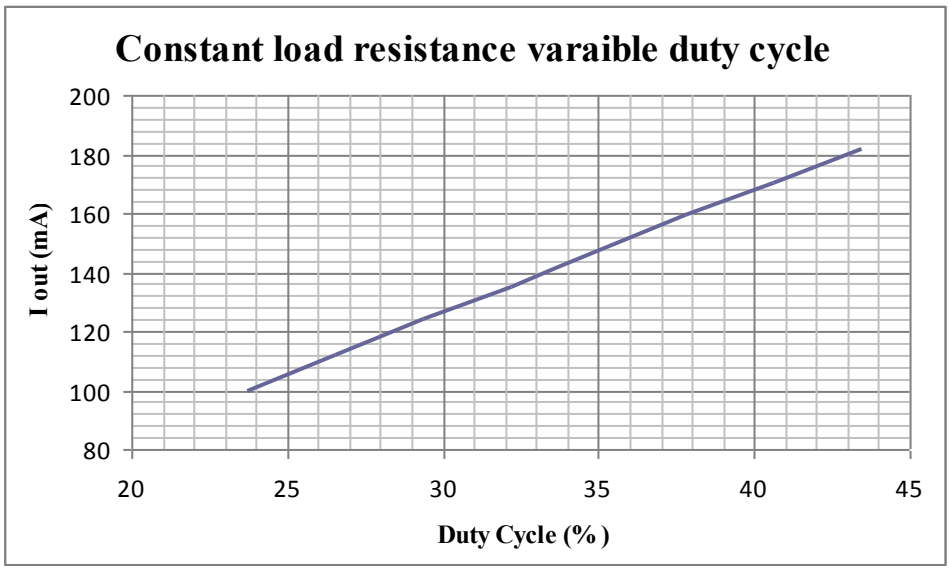


Figure (6.8) The relation between duty cycle and o/p current at constant o/p voltage.

Figures (6.7) and (6.8) show that the relation between duty cycle change and current change is linear when output voltage is constant. Similarly the relation between duty cycle change and voltage change is constant for constant current loads.

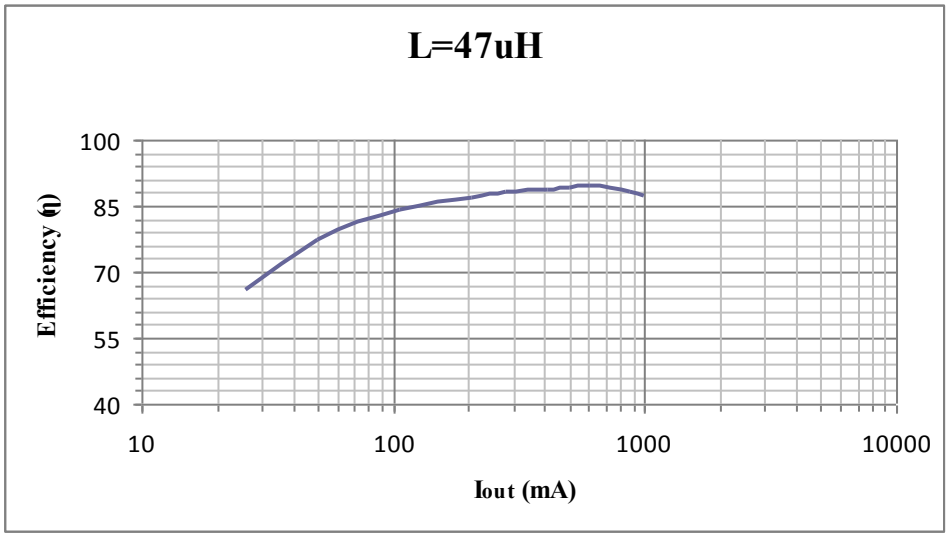


Figure (6.9) Efficiency change with load current for the designed converter.

Figure (6.9) shows the relation between load current and efficiency for the converter operating with 3.7 volts input supply voltage. It can be noticed that the peak efficiency is obtained near designed load current and tends to drop off upon leaving this point.

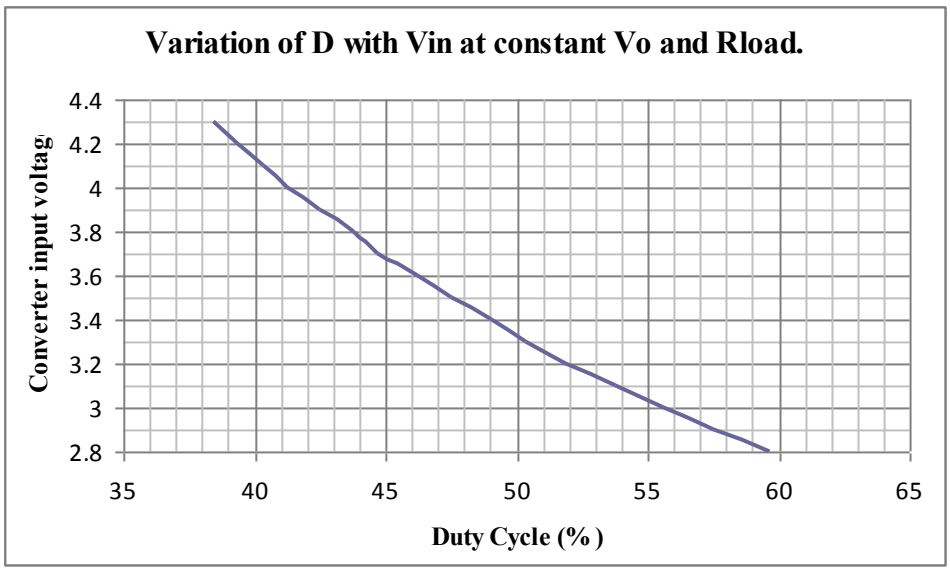


Figure (6.10) The relation between converter supply voltage change with duty cycle at constant load and output voltage.

The relation between variation in input voltage and duty cycle (figure (6.9)) for a constant output voltage and load is somewhat not linear and this has to be dealt with while preparing the control tables for the designed FLC.

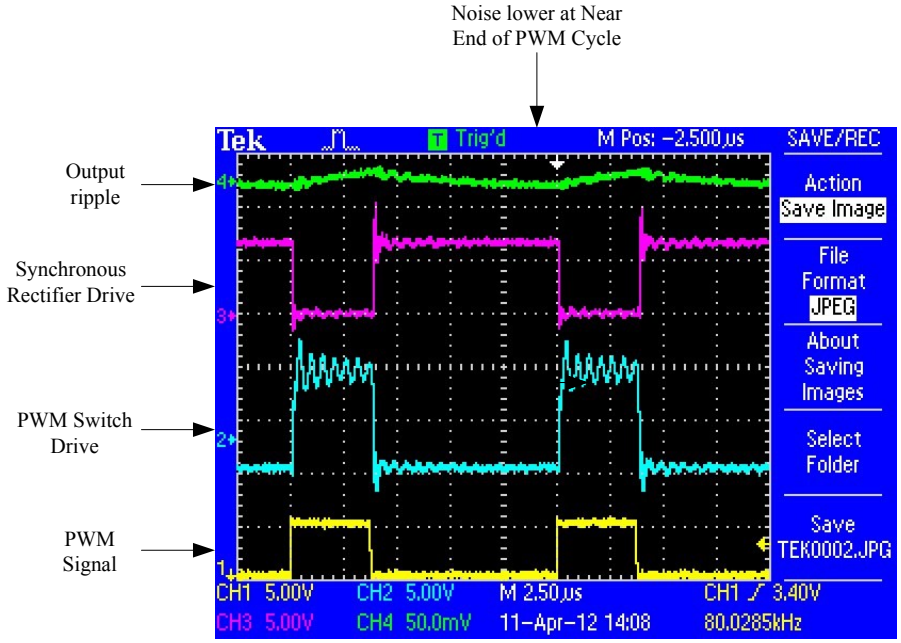


Figure (6.11) Buck Converter control Signal and output ripple for the circuit under test

Figure (6.11) shows the control signals of the buck converter taken from the TEK2004 oscilloscope, the yellow signal is the input PWM signal to the UCC27222 drive circuit, the cyan signal shows the PWM MOSFET drive signal with some ripple due to the dithering operation that is part of the predictive delay generation of the drive circuit, the purple signal is the synchronous rectifier drive signal, and finally the green signal shows the output of the PWM converter ripple. It can be noticed that at the near end of the switching cycle the noise is minimal in the output. This is the point where the ADC of the microcontroller takes the sample for its conversion cycle. Taking the sample at other points could result in noise added to the measured value of the output voltage resulting in erroneous operation of the converter.

The next set of pictures show the different ripple voltage levels obtained from implementing different types of capacitors at the output of the VRM circuit. Three types of capacitors were used, the tantalum capacitor with conductive polymer cathode, the niobium capacitor, and the aluminium solid electrolytic capacitor.

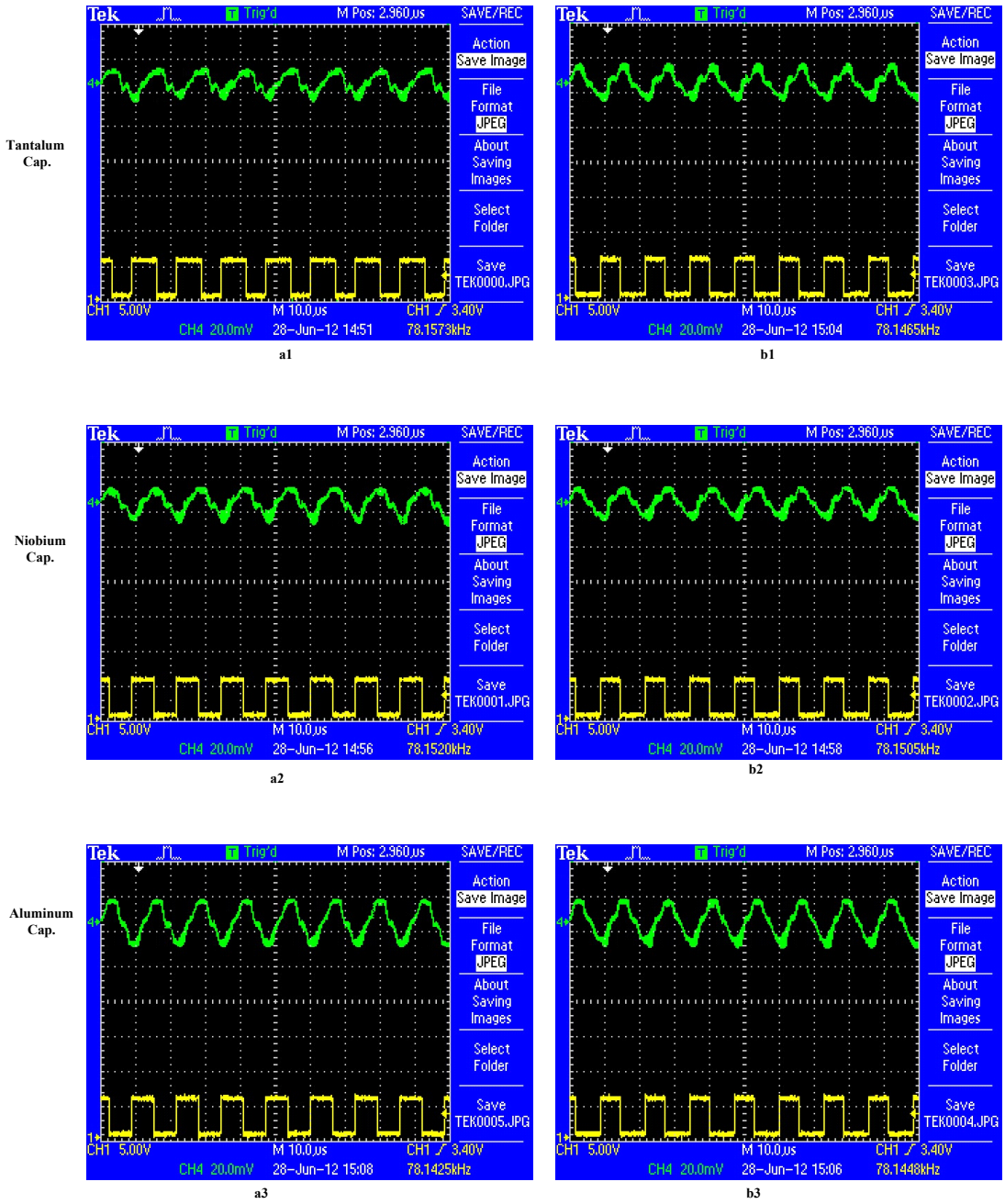


Figure (6.12) The ripple wave forms observed at VRM output for different types of capacitors, (a) at high output current, (b) at low output current.

On observing figure (6.12) it is evident that the ripple at the output is at its lowest value when using the tantalum capacitor as output capacitor of the converter circuit, while the niobium capacitor is very close in ripple level produced by implementing the tantalum capacitor although it is marginally larger. The aluminium solid electrolytic capacitor produced a higher ripple level that can be acceptable in some application for costwise reasons. It is also evident that loading the converter has little effect on ripple level but the waveform becomes a little bit more distorted as the load current increases.

The efficiency tests were repeated for two other sets of calculations that were conducted for target load current of 400mA and 200mA. The design was carried out while keeping output capacitor value unchanged. Two values for converter inductance were selected to be 33µH and 22µH respectively. Rerunning the efficiency test resulted in the responses seen on figure (6.13) and (6.14).

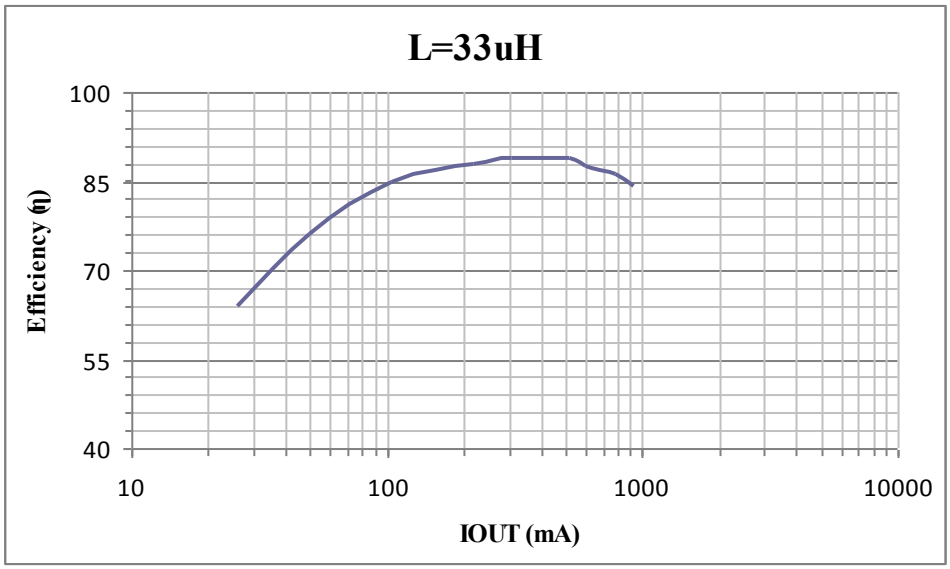


Figure (6.13) Efficiency change with load current for the VRM operating with 33µH inductor.

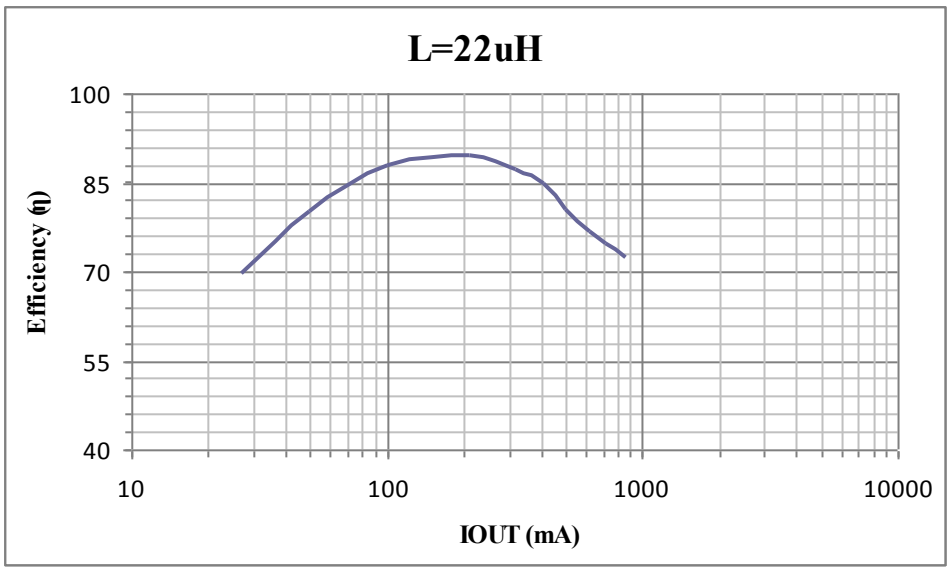


Figure (6.14) Efficiency change with load current for the VRM operating with 22µH inductor.

6.3. Designing the Adaptive Inductor Selecting VRM.

It is evident that if these three efficiency responses were to be overlapped then if the inductor is changed from higher to lower value at the intersection point, the overall efficiency at mid and lower load would have been enhanced. This fact can be utilized by monitoring the load current and switching inductor in a sequence that will ensure smooth transition, a gain in overall efficiency would be possible. Figure (6.15) shows a simplified diagram for an adaptive inductance selecting buck converter.

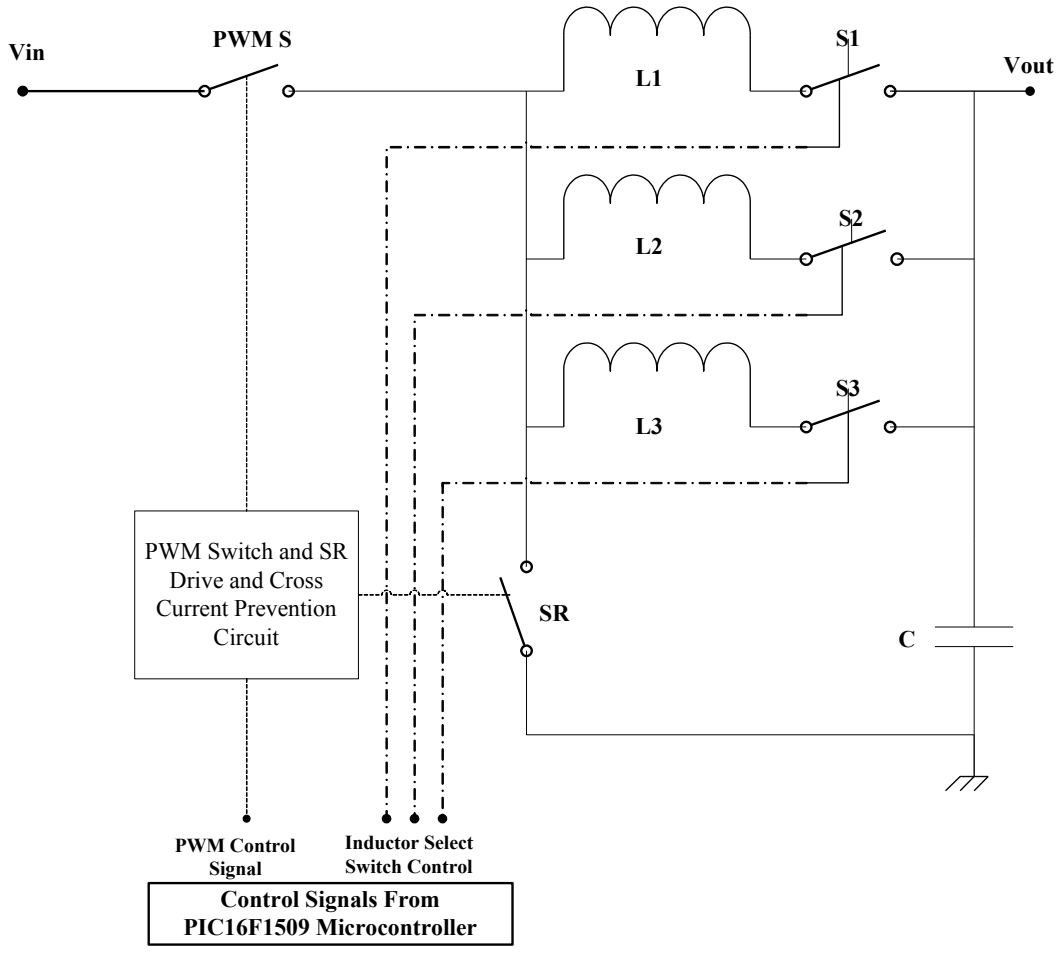


Figure (6.15) The simplified diagram for an adaptive inductance selecting buck converter.

Circuit hardware is almost the same with only the new addition of three switching MOSFET power transistors in addition to two more inductors . The switching MOSFETs implemented for the adaptive inductance switching operations are selected for having the smallest value for $R_{DS(ON)}$. The gate charge capacitance value required to switch on the

transistor is not an important issue here as the switching rate of these transistors is extremely low as compared to those implemented for the PWM switch or the synchronous rectifier. An important operational function has been incorporated inside the adaptive inductor selection control program is that the switch over operation takes place near the end of the PWM cycle and in a Make-Before-Break fashion to reduce inductor exchange noise and to reduce switching stress effects on the MOSFET switching transistor used to furnish this function.

On observing figure (6.14), it is perceived that despite the improvement made in mid value loads, still the efficiency figure drops rapidly at lower load current values. This is the region where the processor core which represents the target load of the design of the smart VRM when it goes to lower power operating states like the standby and the sleep mode. At these levels it is possible to operate the processor core from a secondary power source provided by a simpler voltage regulating module that can operate more efficiently at these output power level requirements. Here a switched capacitor voltage regulator was selected for this purpose, namely the TPS60500 from Texas instruments delivers high efficiency figure at low load current rates [79]. In addition to that it can continue operating as an LDO for higher current rating which allows for smooth transition from primary converter to secondary converter operation and vice versa. The TPS 60500 has operation input control signal that can be used to control device functioning.

Figure (6.16) shows the circuit diagram of the VRM module with the adaptive inductor switching features along with the secondary converter circuit.

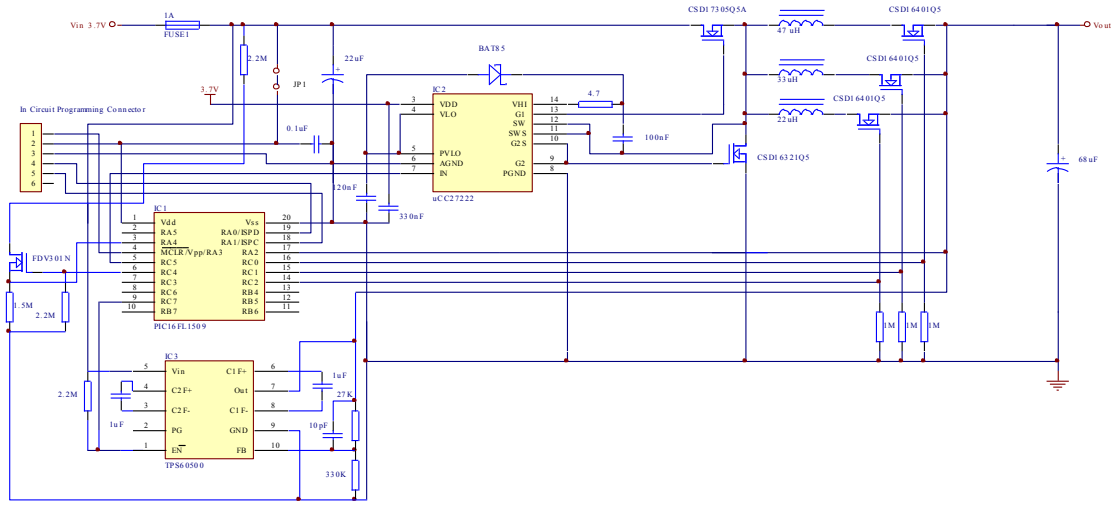


Figure (6.16) The complete circuit diagram of the smart VRM module.

The PCB board for this circuit is shown below in figure (6.17) along with the assembled circuit.

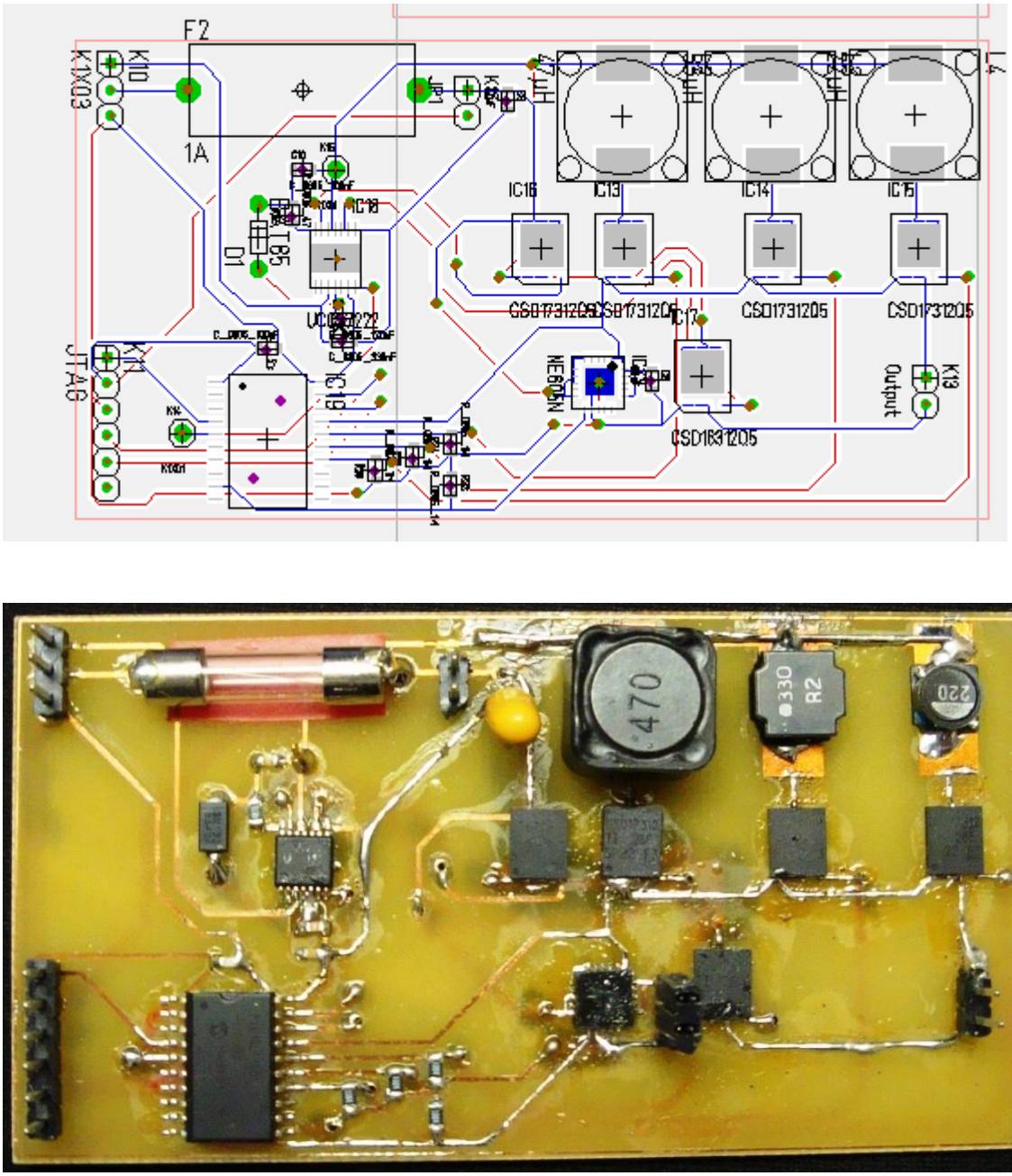
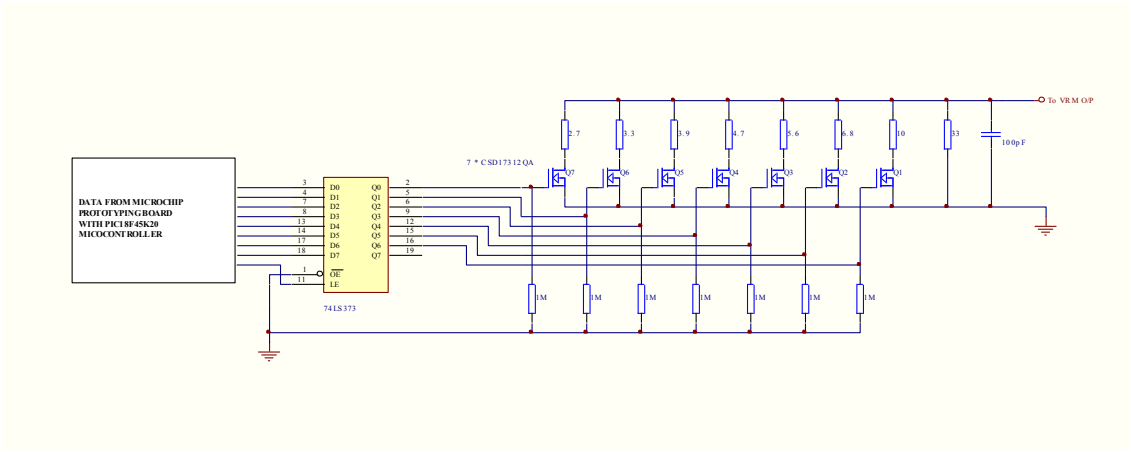


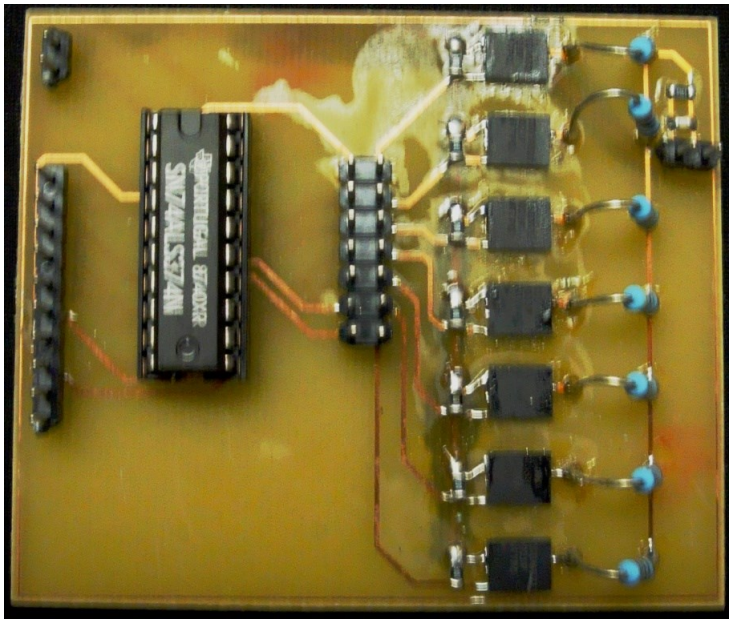
Figure (6.17) The complete assembled circuit of the smart VRM with the PCB drawing.

The TARGET 3001 software was used in the process of preparing the printed circuit boards required in this work.

Additional circuits are required for the performing the required tests, these will include a micro controller based load control circuit that will enable the conduction of tests that shows the transient response feature for the circuit under test. Figure (6.17) shows the circuit diagram and assembled PCB of the load test circuit. A second circuit is required to be built to test an industry standard VRM control integrate circuit namely the TPS62040 from Texas instruments [80]. Figure (6.18) shows the circuit diagram and the assembled PCB for this device.

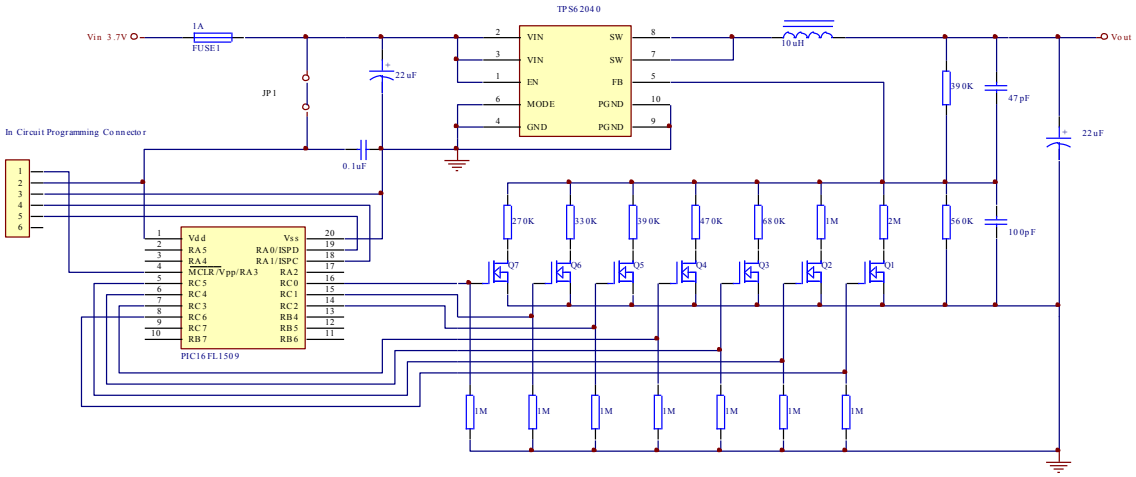


(a)

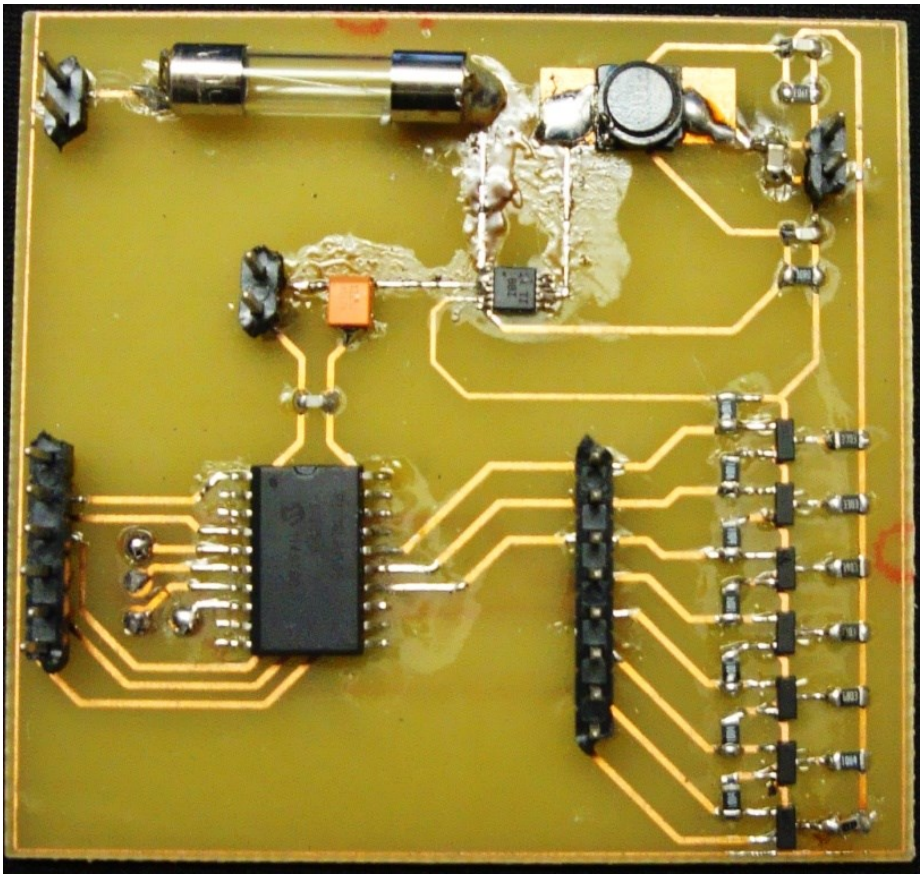


(b)

Figure (6.18)The load test circuit, (a) the circuit diagram, (b) the assembled PCB.



(a)



(b)

Figure (6.19) The TPS62040 industry standard converter module, (a) the circuit diagram, (b) the assembled PCB.

Figure (6.20) shows the prototyping board from Microchips holding the PIC18F45K20 microcontroller fully assembled and can be programmed by MPLAB X software using the PICit3 programming and debugging device.

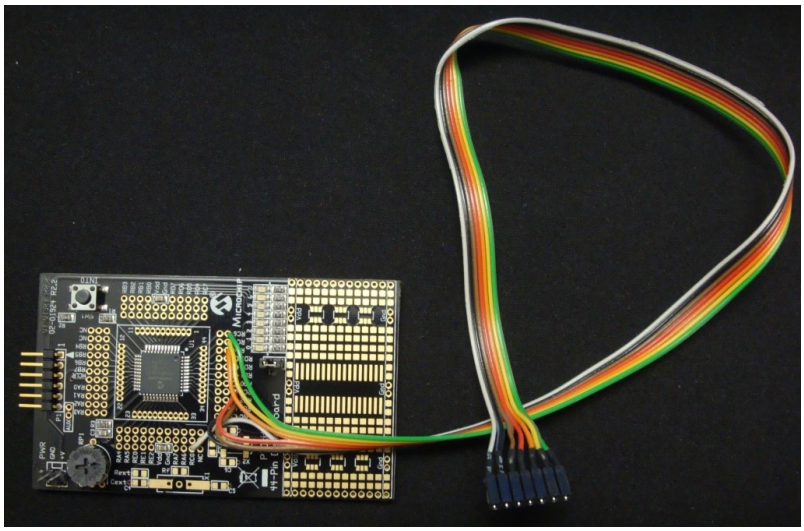


Figure (6.20) The PIC18F45K20 microcontroller evaluation board used in the experimentation.

This evaluation board is used in controlling the load test circuit and performing the load test as well as testing the voltage changing function of the designed VRM as part of the requirement of a DVS system, where the controller on this board was programmed to send voltage change commands to the smart VRM controller via the I^2C serial bus.

Figure (6.21) shows the complete lab experimental setup used in conducting experiments on the designed VRM and to develop the control software for it. The lab set up was used to evaluate the performance of the TPS62040 based VRM against the smart VRM developed during the course of this work. The efficiency figures obtained from both modules were drawn in figure (6.22) together to visualize the features obtained from the developed system.

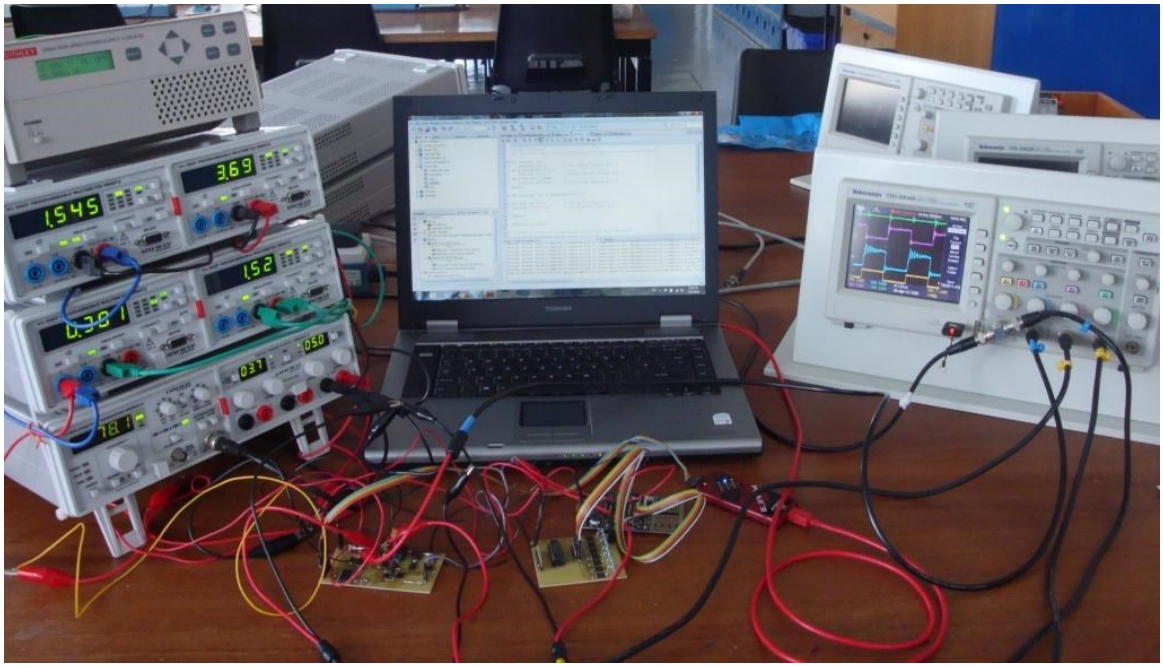


Figure (6.21) The lab test setup used to develop and evaluate the designed smart VRM.

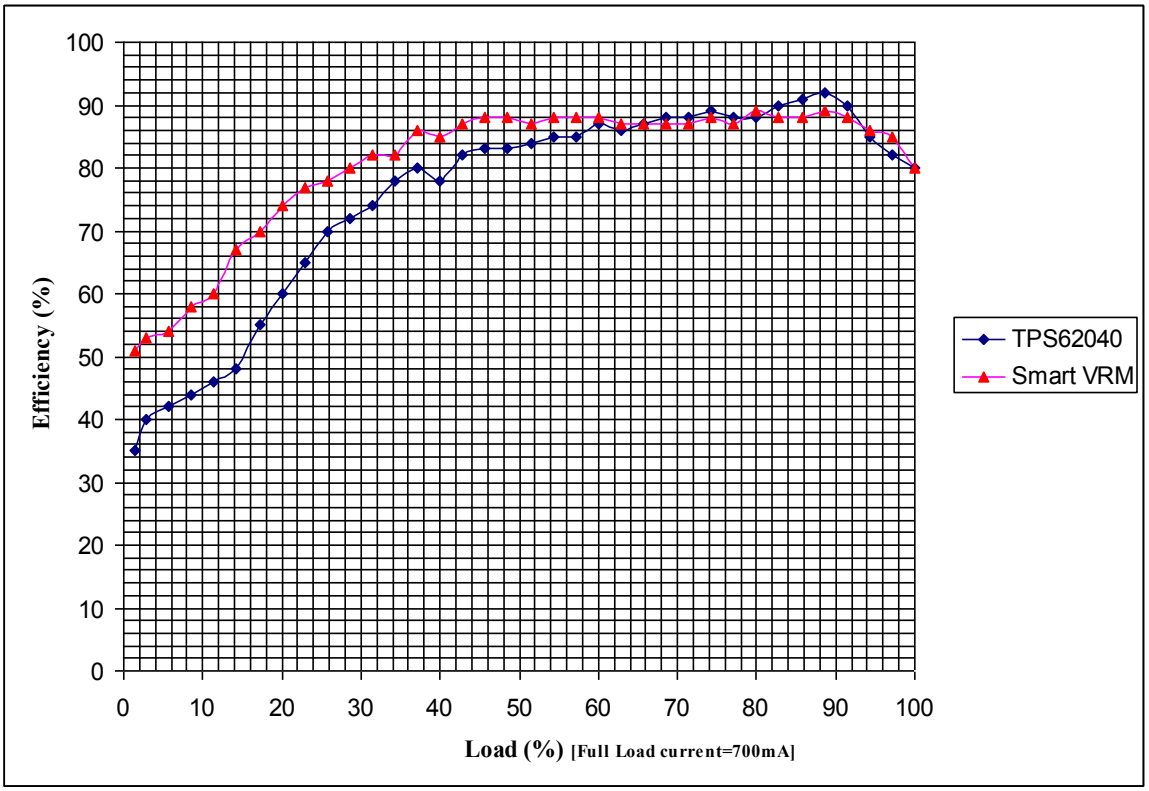


Figure (6.22) Efficiency test for TPS62040 based VRM and designed VRM.

Figure (6.23) shows how the designed VRM changes its output voltage upon receiving load voltage increment or decrement command from the PIC18F45K20 microcontroller evaluation board as if they were received from the PXA 270 microprocessor. The initial test started at 0.85 volts then climbed up to 1.55 volts in 0.1 volt steps then afterwards climbed down in 0.2 volt steps thus demonstrating its DVS function.

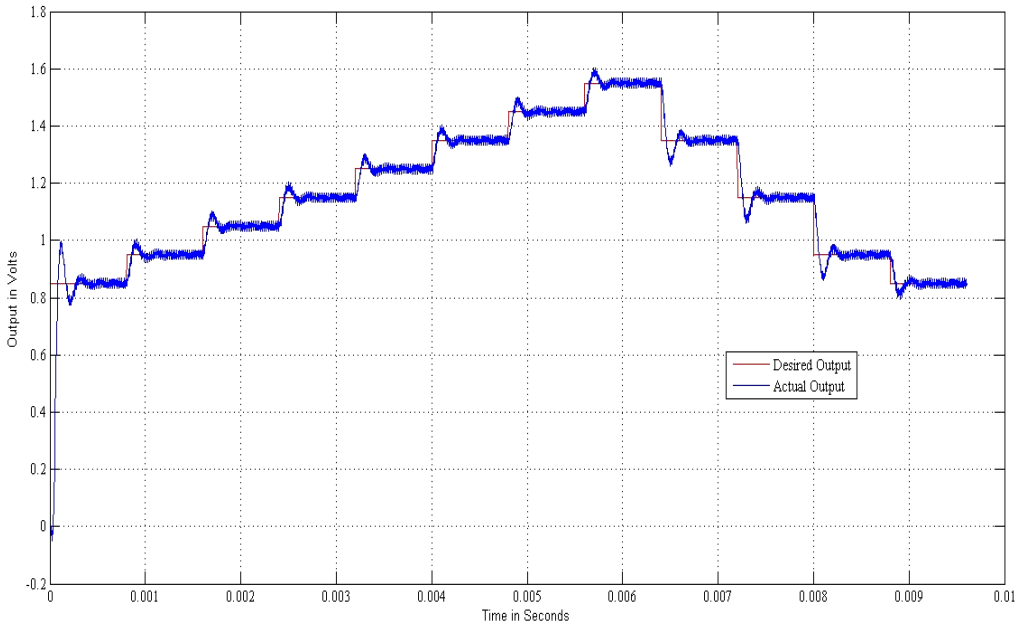


Figure (6.23) The output voltage tracking function of the Designed VRM

6.4. Description of PIC16F1509 Programming

The programming of the PIC16F1509 micro controller was done using the PICit3 programming and debugging tool along with the MPLAB X version 1.1. The MPLABX is an integrated design environment that can be used to develop and debug programs written to the microchip PIC family of microcontrollers. It comes with a C compiler and online debugging facilities that aid watching program variable and microcontroller status simultaneously. Figure (6.24) shows the MPLAB X environment desktop.

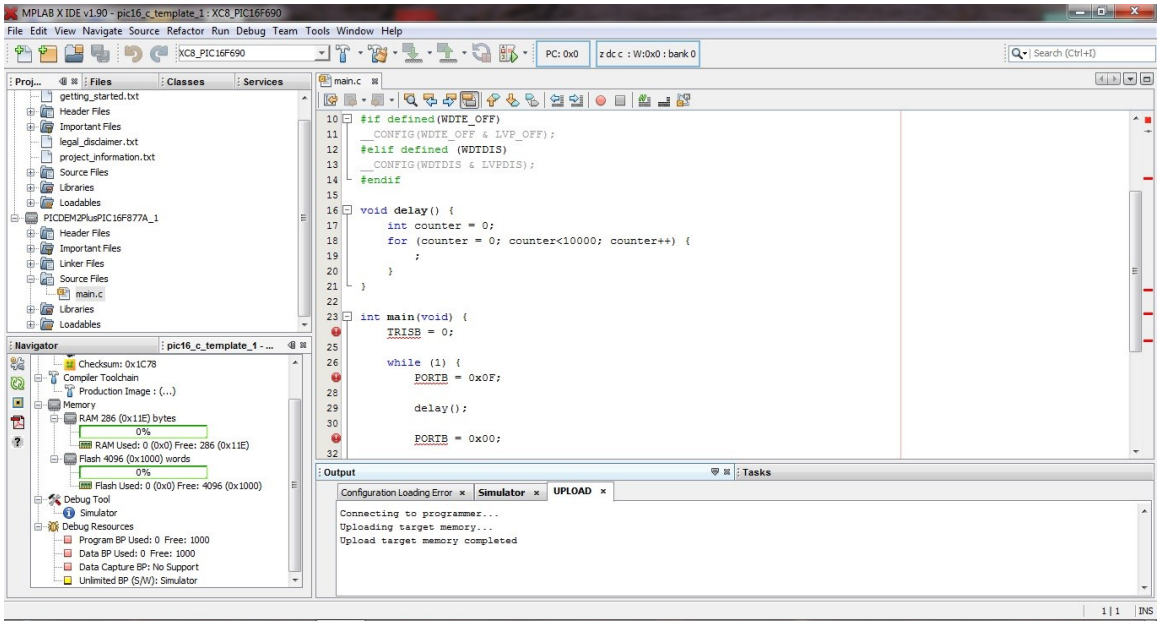


Figure (6.24) The MPLAB X IDE environment desktop.

The software that was written to perform the fuzzy control function has been written while keeping in mind to remove most of the computational complexity in order to reduce software overload thus making the implementation of the smart VRM feasible on this 8 bit microcontroller. Several modifications to the fuzzy control algorithm were made for this purpose the first of which deals with the inputs to the fuzzy controller which are the error and the change in error. These inputs can have negative physical values, to avoid this situation the digital representation of the error and the change in error was biased by (7FHex.) thus avoiding negative values. The next thing done was quantizing the readouts of the ADC so as to define a limited number of variations that will be dealt within the fuzzy inference process. For each value of source voltage from 3.4 volts to 4.2 volts in steps of 0.1 volt a table was constructed that accommodates all the changes that were needed to be done for the duty cycle in a given range of load current changes. In addition to these tables, for each 0.1 volt increment in load voltage from 0.85 volts to 1.55 volts, three look up tables were constructed to deal with possible anticipated load variations, these are for large, middle, and small variations in load current. These look up tables were arranged to aid the operation of the adaptive inductance switching as well as the voltage regulation function, where an estimate of load current is made from monitoring the value of the steady state duty cycle, supply input voltage and the desired output voltage currently under control. The main program flow chart is shown in figure (6.25).

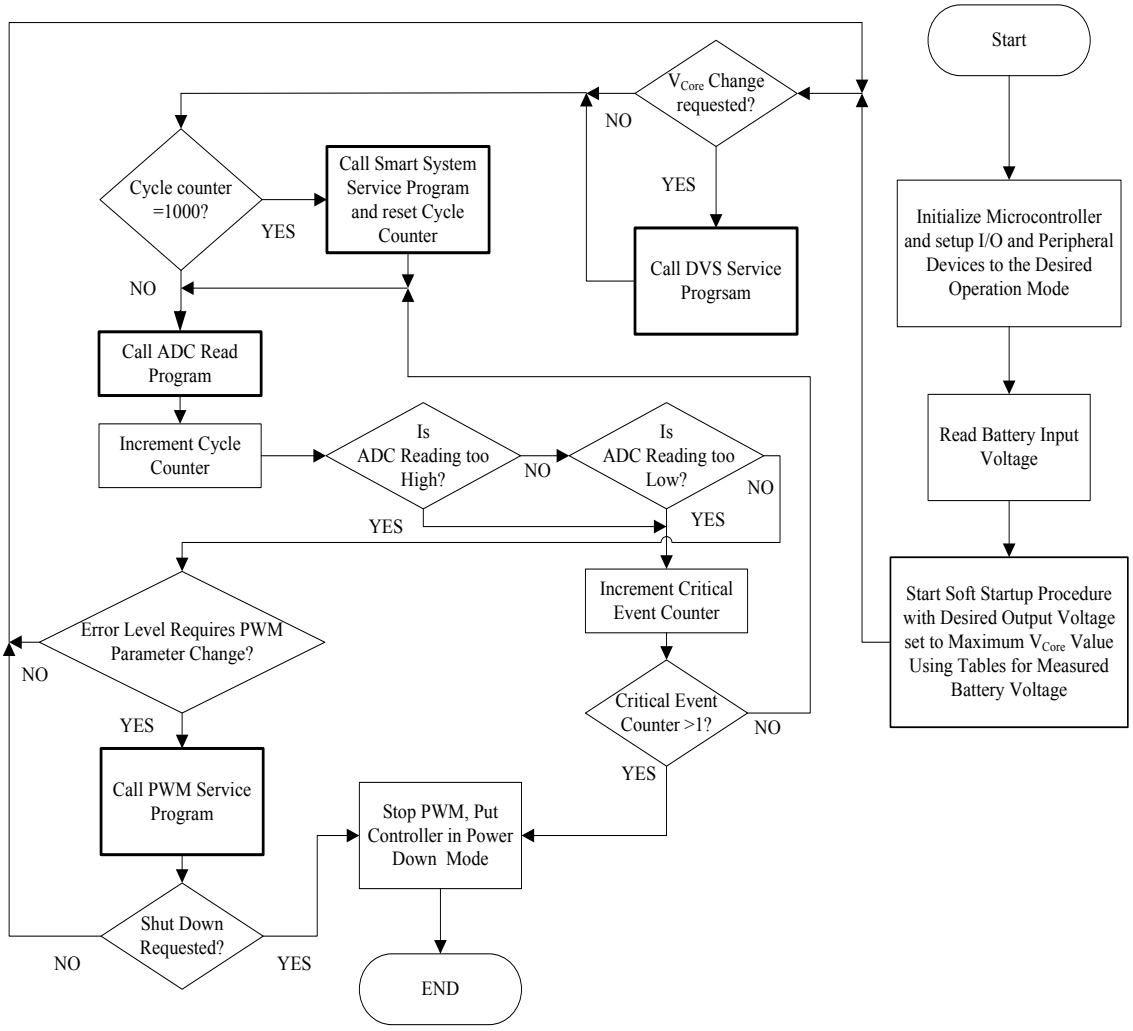


Figure (6.25) The flowchart of the main program of the smart VRM system.

Operation protection features were incorporated in the control software design to make the operation of the designed VRM safe. These safety features are provided in terms of over current and over voltage protection.

The over current protection is achieved by monitoring the load voltage while PWM duty cycle might be at its value that corresponds to the highest load current expected to be delivered by the VRM. When this ADC reading goes below expected Vout value at around 50% for more than ten readings, the case is considered as an overload due to failure in load circuitry and a shut down procedure commences.

Over-voltage protection is supplied by two means the first is when an over voltage condition is detected by getting a reading from ADC that is larger than that expected for the current operation mode, the PWM signal is stopped from being delivered to the drive circuit of the main switching transistor and the synchronous rectifier. Thus stopping the VRM from delivering any supply to the load.

6.5. Chapter Summary

This chapter detailed the steps taken in the design process to realize the smart voltage regulating module. The start was with basic design layout where only the essential parts were included, then the controller was programmed to generate PWM control signal to be fed to the power switching drive circuit and to monitor the output voltage while implementing a proportional control algorithm. The basic system components were of the surface mounted type for which small printed circuit boards were designed and manufactured so as to use these components on a prototyping board to conduct the experimental work. The experimental lab setup explained inside the chapter was used to verify the operation and performance of the circuits under test. The final circuit was assembled on a PCB for final performance verification with another VRM product built around an industry standard product, the Ti TPS60500 which was assembled on a PCB along with the additional parts and controller to work with a DVS ready processor. Final test results showed that the designed circuit provided high efficiency for wider load ranges than that obtained from the TPS 60500 which delivered the high efficiency on lower load current range. The better efficiency gain was made at the lower current load due to the adaptation of auxiliary VRM working on switched capacitor concept and the main VRM was stopped.

Chapter Seven

Conclusions and Suggested Future Work

7.1. Conclusions

In this work, a design for a voltage regulating module in buck topology suitable for supplying the core of a DVS ready processor (PXA270) was proposed and investigated. A careful selection of components had its impact on boosting converter efficiency. Modern small size low ESR capacitor and low leakage inductors with flat conductor and enhanced magnetic core made it possible to operate the buck converter at lower frequencies without requiring relatively larger space, in addition to selecting MOS devices with very low FOM to minimize power loss that is augmented by operating the converter at relatively lower frequency. Furthermore, the MOS gate driver device has a unique feature of dynamically selecting dead zone between gating the MOS switch and the MOS synchronous rectifier using the predictive approach thus resulting in better cross current prevention in addition to maintaining higher efficiency. The selected microcontroller (PIC16FL1509) has a low operating power that had smaller impact on overall efficiency in addition to a powerful RISC design that permits performing good control function which is being implemented using a fuzzy controller. This microcontroller has several types of serial buses; this feature eases the transaction between the main processor and the microcontroller through the I^2C bus in implementing DVS functions. The proposed fuzzy controller performance was compared against an optimized tuned PID controller. The results promoted using the PD like fuzzy controller with much better implementation flexibility on a low power microcontroller with lower software overhead than the case if another more complex controller type would be considered. The overall system efficiency is over 89% and the system maintained higher efficiency that comparable systems could not over a wide range of operating conditions due to the following circuit enhancements:

- Adaptive inductor selection: the controller estimates load current requirement from duty cycle (PWM register contents) and accordingly if the load current comes within the range values of a specific inductor, the switching over is made to select the inductor suitable for this current range.

- Auxiliary converter is started when operating current reaches that required for standby condition or lower power states. The main converter is stopped and main controller goes to lower power state order to reduce overall quiescent losses for better efficiency figure can be achieved

These circuit enhancements along with careful component selection and the employment of the predictive gate delay technique which effectively prevents cross current and body diode conduction resulted in better efficiency figures than those obtainable from industry standard type like the TPS62040 or ISL85418.

The size issue can be curbed by using stackable low profile inductors that can be evenly distributed on a multilayer printed circuit board to minimize overall size.

7.2. Suggested Future Work

The following points are suggested for the development of the work done in this thesis such as:

1- Conducting simulation on different versions of the proposed controller applied to another type of VRM control methodology, such as a current controlled and mixed signal controlled models.

2- Using additional details on components nonlinearities and incorporate these into the simulation model built can more near life response to the simulation.

3- Investigate in other fuzzy logic controllers besides the PD like version like PI like and PID like FLC.

The following points are suggested for future work:

1- Using interleaved converter topology promoting the implementation of smaller inductors resulting in faster dynamic response from the VRM with much lower ripple voltage levels.

2- Using a hybrid approach by implementing a linear PWM generating device will enable operating the buck converter inside the design smart VRM to operate at higher switching frequencies resulting in implementing smaller inductors yielding lighter and smaller product.

3- Developing the current VRM to accept input from energy harvesting units and fuel cell systems that might be included inside future models of mobile computing applications.

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Appendices

Appendix A

Excerpts from lab experiment results and the fuzzy set crisp output control action low resolution table.

Page No: 1 Cap.: Tantalum 68µF Ind.: 47µH

Vin:4.2Volts		PWM Freq.:80KHz, T=12.5 µS.		Vload:1.55Volts	
P_{IN} (mW)	I_{IN} (mA)	τ (µ Sec.)	Duty Cycle (%)	I_{OUT} (mA)	P_{OUT}(mW)/η
63	15	4.76	38.08	26	40.3 (64)
102.06	24.3	4.8	38.44	50	77.5 (76)
187.74	44.7	4.84	38.72	105	162.75 (86.7)
389.76	92.8	5.0	40	220	341 (87.5)
551.88	131.4	5.12	40.96	307	475.85 (86.2)
1024.8	244	5.44	43.52	523	810.65 (79.1)
1228.92	292.6	5.6	44.8	604	936.2 (76.2)
1678.32	399.6	5.88	47.04	788	1221.4 (72.7)
2045.4	487	6.08	48.64	932	1444.6 (70.6)
Vin: 3.7Volts					
P_{IN}(mW)	I_{IN} (mA)	τ (µ Sec.)	Duty Cycle (%)	I_{OUT} (mA)	P_{OUT}(mW)/η
59.94	16.2	5.36	42.88	27	41.85 (69.8)
96.94	26.2	5.4	43.2	50	77.5 (79.95)
178.34	48.2	5.44	43.52	101	156.55 (87.8)
363.34	98.2	5.64	45.12	210	325.5 (89.6)
565.36	152.8	5.88	47.04	318	492.9 (87.2)
734.08	198.4	6.04	48.32	410	635.5 (86.6)
968.29	261.7	6.24	49.92	503	779.65 (80.5)
1267.62	342.6	6.44	51.52	626	970.3 (76.6)
1483.7	401	6.6	52.28	716	1109.8 (74.8)
1857.4	502	6.88	55.04	868	1345.4 (72.5)
Vin:3.4Volts					
P_{IN}(mW)	I_{IN} (mA)	τ (µ Sec.)	Duty Cycle (%)	I_{OUT} (mA)	P_{OUT}(mW)/η
59.16	17.4	5.84	46.72	26	40.3 (68.12)
94.52	27.8	5.88	47.04	50	77.5 (82)
185.98	54.7	6.0	48	106	164.3 (88.35)
357.68	105.2	6.2	49.6	206	319.3 (89.27)
496.06	145.9	6.36	50.88	282	437.1 (88.15)
757.86	222.9	6.6	52.28	413	640.15 (84.5)
975.12	286.8	6.8	54.4	507	785.85 (80.1)
1199.86	352.9	6.96	55.68	603	934.65 (77.9)
1567.06	460.9	7.28	58.24	868	1345.4 (55.4)

Page No: 2 Cap.: Tantalum 68µF Ind.: 47µH

Vin:4.2Volts		PWM Freq.:78.12KHz, T=12.8 µS.			Vload:1.15Volts
P_{IN} (mW)	I_{IN} (mA)	τ (µ Sec.)	Duty Cycle (%)	I_{OUT} (mA)	P_{OUT} (mW)/η
56.7	13.3	3.52	27.5	25	28.75
84.42	20.1	3.54	27.66	50	57.5 (68.11)
143.22	34.1	3.6	28.13	100	115 (80.3)
267.12	63.6	3.72	29.06	201	231.15 (86.5)
403.62	96.1	3.8	29.7	306	351.9 (87.2)
534.24	127.2	3.92	30.63	401	461.15 (86.32
684.6	163	4.0	31.25	506	581.9 (84.99)
850.08	202.4	4.12	32.19	614	706.1 (83.06)
1068.48	254.4	4.24	33.13	731	840.65(78.68)
Vin: 3.7Volts					Vload:1.15Volts
P_{IN} (mW)	I_{IN} (mA)	τ (µ Sec.)	Duty Cycle (%)	I_{OUT} (mA)	P_{OUT} (mW)/η
49.58	13.4	4	31.25	25	28.75(57.99)
78.81	21.3	4.02	31.41	50	57.5 (72.96)
138.01	37.3	4.08	31.88	100	115 (83.33)
260.85	70.5	4.2	32.81	201	231.15(88.62)
388.87	105.1	4.32	33.75	298	342.7 (88.13)
530.21	143.3	4.44	34.69	401	461.15(86.98)
683.76	184.8	4.56	35.63	507	583.05(85.27)
851.37	230.1	4.72	36.88	615	707.25(83.07)
1037.11	280.3	4.84	37.82	732	841.8 (81.17)
Vin:3.4Volts					Vload:1.15Volts
P_{IN} (mW)	I_{IN} (mA)	τ (µ Sec.)	Duty Cycle (%)	I_{OUT} (mA)	P_{OUT} (mW)
46.24	13.6	4.32	33.75	25	28.75 (62.18)
75.48	22.2	4.36	34.06	50	57.5 (76.18)
134.3	39.5	4.44	34.69	100	115 (85.63)
259.08	76.2	4.6	35.94	201	231.15(89.22)
395.42	116.3	4.72	36.88	305	350.75 (88.7)
525.64	154.6	4.84	37.82	401	461.15(87.73)
682.72	200.8	5.0	39.06	507	583.05(85.4)
845.58	248.7	5.12	40.00	614	706.1 (83.51)
1030.2	303	5.28	41.25	730	839.5 (70.86)

Page No: 3 Cap.: Tantalum 68µF Ind.: 47µH

Vin:4.2Volts	PWM Freq.:78.12KHz, T=12.8 µS.			Vload:0.85Volts	
P_{IN}(mW)	I_{IN} (mA)	τ (µ Sec.)	Duty Cycle (%)	I_{OUT} (mA)	P_{OUT} (mW)/η
47.04	11.2	2.6	20.32	25	21.25(45.18)
67.2	16	2.62	20.47	50	42.5 (63.25)
111.72	26.6	2.68	20.94	100	85 (76.08)
202.86	48.3	2.76	21.56	200	170 (83.8)
299.46	71.3	2.88	22.50	298	253.3 (84,6)
418.74	99.7	3	23.44	410	348.5 (83.23)
524.58	124.9	3.08	24.07	507	430.95(82.2)
Vin: 3.7Volts				Vload:0.85Volts	
P_{IN}(mW)	I_{IN} (mA)	τ (µ Sec.)	Duty Cycle (%)	I_{OUT} (mA)	P_{OUT} (mW)/η
41.44	11.2	2.96	23.13	25	21.25 (51.28)
61.79	16.7	2.97	23.20	50	42.5 (68.8)
105.08	28.4	3.04	23.75	100	85 (80.9)
198.69	53.7	3.16	24.70	201	170.85 (86)
305.25	82.5	3.28	25.63	307	260.95 (85.5)
412.92	111.6	3.4	26.63	409	347.65 (84.2)
522.81	141.3	3.48	27.20	507	430.95(82.43)
Vin:3.4Volts				Vload:0.85Volts	
P_{IN}(mW)	I_{IN} (mA)	τ (µ Sec.)	Duty Cycle (%)	I_{OUT} (mA)	P_{OUT} (mW)/η
37.4	11	3.2	25.00	25	21.25 (56.82)
58.48	17.2	3.24	25.31	50	42.5 (72.67)
102.68	30.2	3.32	25.94	100	85 (82.78)
194.82	57.3	3.44	26.88	200	170 (87.26)
302.6	89	3.56	27.81	307	260.95(86.24)
412.76	121.4	3.68	28.75	410	348.5 (84.43)
525.3	154.5	3.84	30.00	507	430.95(82.04)

Page No: 4 Cap.: Tantalum 68µF Ind.: 47µH

Vin:3.7Volts	PWM Freq.:78.12KHz, T=12.8µS.		Constant Load Current	
I_{IN} (mA)	τ (µ Sec.)	Duty Cycle (%)	I_{OUT} (mA)	V_{OUT} (Volts)
29.3	3.04	23.75	100	0.85
32	3.36	26.25	100	0.95
34.5	3.72	29.06	100	1.05
37.5	4.08	31.87	100	1.15
40.3	4.4	34.37	100	1.25
43.2	4.76	37.18	100	1.35
46	5.12	40.00	100	1.45
48.9	5.48	42.81	100	1.55

Vin: 3.7Volts	Constant Load with Variable Duty Cycle R_{Load}= 85Ω			
I_{IN} (mA)	τ (µ Sec.)	Duty Cycle (%)	I_{OUT} (mA)	V_{OUT} (Volts)
29.1	3.04	23.75	100	0.85
35	3.4	26.56	112	0.95
41.6	3.76	29.37	124	1.05
49	4.12	32.18	135	1.15
57	4.48	35.00	147	1.25
65.7	4.84	37.81	159	1.35
74.8	5.2	40.62	170	1.45
84.8	5.56	43.43	182	1.55

Page No: 5 Cap.: Tantalum 68µF Ind.: 47µH

V_{IN}:4.3-2.8 V	PWM Freq:78.12KHz, T=12.8 µS		V_{Load}: 1.55V	I_{Load}:300mA
V_{IN} (Volts)	I_{IN} (mA)	P_{IN} (mW)	T (µ Sec.)	Duty Cycle (%)
4.3	121.8	523.74	4.92	38.44
4.2	124.5	522.9	5.04	39.38
4.1	127	520.7	5.16	40.31
4.0	130.1	520.4	5.28	41.25
3.9	133.3	519.87	5.44	42.5
3.8	136.5	518.7	5.6	43.8
3.7	139.8	517.26	5.72	44.69
3.6	143.3	515.88	5.92	46.25
3.5	147.1	514.85	6.08	47.5
3.4	151.4	514.76	6.28	49.06
3.3	155.5	513.15	6.44	50.32
3.2	160.1	512.32	6.64	51.88
3.1	164.9	511.19	6.88	53.75
3.0	170.2	510.6	7.12	55.63
2.9	175.8	509.82	7.36	57.5
2.8	181.7	508.76	7.64	59.69

Fuzzy Set Control Action Crisp Output in 8bit Low Resolution Table

Change in Error \ Error	0	8	16	24	32	40	48	56	64	72	80	88	96	104	112	120
0	14	14	15	16	14	14	14	15	17	16	17	19	20	23	23	23
8	14	14	15	16	14	14	14	15	17	16	17	21	26	29	28	28
16	15	15	15	16	15	15	15	15	17	17	19	24	30	34	34	35
24	16	16	16	16	16	16	16	17	18	18	20	25	31	36	40	41
32	14	14	15	16	16	16	16	16	19	18	20	24	29	37	42	45
40	14	14	15	16	16	18	18	19	23	21	23	27	33	39	44	48
48	14	14	15	16	16	18	23	25	29	26	27	33	39	44	48	51
56	15	15	15	17	16	19	25	30	34	31	34	39	46	51	54	57
64	17	17	17	18	19	23	29	34	38	38	40	44	50	57	62	66
72	16	16	17	18	18	21	26	31	38	43	45	48	53	60	69	74
80	17	17	19	20	20	23	27	34	40	45	48	51	56	64	73	81
88	19	21	24	25	24	27	33	39	44	48	51	56	60	68	76	84
96	20	26	30	31	29	33	39	46	50	53	56	60	67	74	82	90
104	23	29	34	36	37	39	44	52	57	60	64	68	74	82	89	97
112	23	28	34	40	42	44	49	54	62	69	73	76	82	89	96	104
120	23	28	35	41	45	48	51	57	66	74	81	84	90	97	104	111
128	28	32	39	44	48	51	55	61	69	78	86	93	98	105	113	120
136	32	40	45	49	52	55	61	67	74	82	90	99	106	113	121	128
144	39	45	53	56	59	62	67	74	81	89	97	105	113	121	128	135
152	44	49	56	63	67	71	75	82	88	96	105	113	121	128	135	143
160	48	52	59	67	76	79	83	89	96	104	112	121	128	135	143	150
168	51	55	62	71	79	88	91	97	105	113	120	128	135	143	151	157
176	55	61	67	75	83	91	100	105	113	121	128	136	144	151	159	166
184	61	67	74	82	89	97	105	114	121	128	135	143	152	160	167	174
192	69	74	81	88	96	105	113	121	128	135	143	151	160	168	175	182
200	78	82	89	96	104	113	121	128	135	142	151	159	167	174	182	189
208	86	90	97	105	112	120	128	135	143	151	156	165	173	181	189	195
216	94	99	105	113	121	128	136	143	151	159	165	168	177	185	194	201
224	100	106	113	121	128	135	144	152	160	167	173	177	180	189	197	204
232	108	114	121	128	135	143	151	160	168	175	181	185	189	193	200	207
240	116	121	128	135	143	151	159	167	175	182	189	194	197	200	203	211
248	123	128	135	142	150	157	166	174	182	189	195	201	204	207	211	216
256	128	133	139	148	156	162	170	178	187	195	201	205	208	212	217	224

Part 1

Change in Error \ Error	128	136	144	152	160	168	176	184	192	200	208	216	224	232	240	248
0	28	32	39	44	48	51	55	61	69	78	86	94	28	32	39	44
8	32	40	45	49	52	55	61	67	74	82	90	99	32	40	45	49
16	39	45	53	56	59	62	67	74	81	89	97	105	39	45	53	56
24	44	49	56	63	67	71	75	82	88	96	105	113	44	49	56	63
32	48	52	59	67	76	79	83	89	96	104	112	121	48	52	59	67
40	51	55	62	71	79	88	91	97	105	113	120	128	51	55	62	71
48	55	61	67	75	83	91	100	105	113	121	128	136	55	61	67	75
56	61	67	74	82	89	97	105	114	121	128	135	143	61	67	74	82
64	69	74	81	88	96	105	113	121	128	135	143	151	69	74	81	88
72	78	82	89	96	104	113	121	128	135	142	151	159	78	82	89	96
80	86	90	97	105	112	120	128	135	143	151	156	165	86	90	97	105
88	93	99	105	113	121	128	136	143	151	159	165	168	93	99	105	113
96	98	106	113	121	128	135	144	152	160	167	173	177	98	106	113	121
104	105	113	121	128	135	143	151	160	168	175	181	185	105	113	121	128
112	113	121	128	135	143	151	159	167	175	182	189	194	113	121	128	135
120	120	128	135	143	150	157	166	174	182	189	195	201	120	128	135	143
128	128	136	143	151	158	163	170	178	187	195	201	205	128	136	143	151
136	136	145	152	159	166	172	175	182	190	199	205	208	136	145	152	159
144	143	152	160	167	174	180	183	187	194	202	208	212	143	152	160	167
152	151	159	167	174	182	188	192	196	199	205	212	217	151	159	167	174
160	158	166	174	182	189	196	200	203	206	210	217	223	158	166	174	182
168	163	172	180	188	196	200	205	208	212	217	223	229	163	172	180	188
176	170	175	183	192	200	205	208	211	216	222	229	233	170	175	183	192
184	178	182	187	196	203	208	211	213	218	225	230	235	178	182	187	196
192	187	190	194	199	206	212	216	218	218	222	227	233	187	190	194	199
200	195	199	202	204	210	217	222	225	222	226	231	237	195	199	202	204
208	201	205	207	212	217	223	229	230	227	231	233	238	201	205	207	212
216	205	208	212	217	223	229	233	235	233	237	238	238	205	208	212	217
224	208	211	214	219	227	232	236	238	237	240	240	240	208	211	214	219
232	212	215	216	220	225	231	236	238	238	239	240	240	212	215	216	220
240	217	221	222	222	226	232	237	239	239	241	241	241	217	221	222	222
248	224	228	228	227	230	235	239	240	239	241	242	242	224	228	228	227
256	228	233	233	233	236	237	239	240	239	241	242	242	228	233	233	233

Part 2

Appendix B

Excerpts from main components data sheets

PIC16(L)F1508/9

20-Pin Flash, 8-Bit Microcontrollers with nanoWatt XLP Technology

High-Performance RISC CPU:

- C Compiler Optimized Architecture
- Only 49 Instructions
- Up to 14 Kbytes Linear Program Memory Addressing
- Up to 512 bytes Linear Data Memory Addressing
- Operating Speed:
  - DC – 20 MHz clock input
  - DC – 200 ns instruction cycle
- Interrupt Capability with Automatic Context Saving
- 16-Level Deep Hardware Stack with Optional Overflow/Underflow Reset
- Direct, Indirect and Relative Addressing modes:
  - Two full 16-bit File Select Registers (FSRs)
  - FSRs can read program and data memory

Flexible Oscillator Structure:

- 16 MHz Internal Oscillator Block:
  - Factory calibrated to ±1%, typical
  - Software selectable frequency range from 16 MHz to 31 kHz
- 31 kHz Low-Power Internal Oscillator
- Three External Clock modes up to 20 MHz

Special Microcontroller Features:

- Operating Voltage Range:
  - 1.8V to 3.6V (PIC16LF1508/9)
  - 2.3V to 5.5V (PIC16F1508/9)
- Self-Programmable under Software Control
- Power-on Reset (POR)
- Power-up Timer (PWRT)
- Programmable Low-Power Brown-Out Reset (LPBOR)
- Extended Watchdog Timer (WDT):
  - Programmable period from 1 ms to 256s
- Programmable Code Protection
- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- Enhanced Low-Voltage Programming (LVP)
- In-Circuit Debug (ICD) via two pins
- Power-Saving Sleep mode:
  - Low-Power Sleep mode
  - Low-Power BOR (LPBOR)
- Integrated Temperature Indicator
- 128 Bytes High-Endurance Flash
  - 100,000 write Flash endurance (minimum)

Extreme Low-Power Management with nanoWatt XLP (PIC16LF1508/9):

- Standby Current:
  - 25 nA @ 1.8V, typical
- Watchdog Timer Current:
  - 300 nA @ 1.8V, typical
- Operating Current:
  - 30 μA/MHz @ 1.8V, typical
- Timer1 Oscillator Current:
  - 600 nA @ 32 kHz, 1.8V, typical

Peripheral Features:

- Analog-to-Digital Converter (ADC):
  - 10-bit resolution
  - 12 external channels
  - 3 internal channels:
    - Fixed Voltage Reference
    - Digital-to-Analog Converter
    - Temperature Indicator channel
  - Auto acquisition capability
  - Conversion available during Sleep
- 2 Comparators:
  - Rail-to-rail inputs
  - Power mode control
  - Software controllable hysteresis
- Voltage Reference module:
  - Fixed Voltage Reference (FVR) with 1.024V, 2.048V and 4.096V output levels
  - Up to 1 rail-to-rail resistive 5-bit DAC with positive reference selection
- 18 I/O Pins (1 Input-only Pin):
  - High current sink/source 25 mA/25 mA
  - Individually programmable weak pull-ups
  - Individually programmable interrupt-on-change (IOC) pins
- Timer0: 8-Bit Timer/Counter with 8-Bit Programmable Prescaler
- Enhanced Timer1:
  - 16-bit timer/counter with prescaler
  - External Gate Input mode
- Timer2: 8-Bit Timer/Counter with 8-Bit Period Register, Prescaler and Postscaler
- Four 10-bit PWM modules
- Master Synchronous Serial Port (MSSP) with SPI and I^2C™ with:
  - 7-bit address masking
  - SMBus/PMBus™ compatibility

PIC16(L)F1508/9

Peripheral Features (Continued):

- Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)
  - RS-232, RS-485 and LIN compatible
  - Auto-Baud Detect
  - Auto-wake-up on Start
- 4 Configurable Logic Cell (CLC) modules:
  - 16 selectable input source signals
  - Four inputs per module
  - Software control of combinational/sequential logic/state/clock functions
  - AND/OR/XOR/D Flop/D Latch/SR/JK
  - External or internal inputs/outputs
  - Operation while in Sleep
- Numerically Controlled Oscillator (NCO):
  - 20-bit accumulator
  - 16-bit increment
  - True linear frequency control
  - High-speed clock input
  - Selectable Output modes
    - Fixed Duty Cycle (FDC) mode
    - Pulse Frequency (PF) mode
- Complementary Waveform Generator (CWG):
  - 8 selectable signal sources
  - Selectable falling and rising edge dead-band control
  - Polarity control
  - 4 auto-shutdown sources
  - Multiple input sources: PWM, CLC, NCO

PIC12(L)F1501/PIC16(F)L150X Family Types

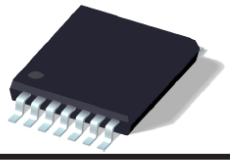
Device	Data Sheet Index	Program Memory Flash (words)	Data SRAM (bytes)	I/O's(2)	10-bit ADC (ch)	Comparators	DAC	Timers (8/16-bit)	PWM	EUSART	MSSP (I^2C/SPI)	CWG	CLC	NCO	Debug(1)	XLP
PIC12(L)F1501	(1)	1024	64	6	4	1	1	2/1	4	—	—	1	2	1	H	—
PIC16(L)F1503	(2)	2048	128	12	8	2	1	2/1	4	—	1	1	2	1	H	—
PIC16(L)F1507	(3)	2048	128	18	12	—	—	2/1	4	—	—	1	2	1	H	—
PIC16(L)F1508	(4)	4096	256	18	12	2	1	2/1	4	1	1	1	4	1	I/H	Y
PIC16(L)F1509	(4)	8192	512	18	12	2	1	2/1	4	1	1	1	4	1	I/H	Y

Note 1: I - Debugging, Integrated on Chip; H - Debugging, Requires Debug Header.
2: One pin is input-only.

Data Sheet Index: (Unshaded devices are described in this document.)

1:	Future Product	PIC12(L)F1501 Data Sheet, 8-Pin Flash, 8-bit Microcontrollers.
2:	DS41607	PIC16(L)F1503 Data Sheet, 14-Pin Flash, 8-bit Microcontrollers.
3:	DS41586	PIC16(L)F1507 Data Sheet, 20-Pin Flash, 8-bit Microcontrollers.
4:	DS41609	PIC16(L)F1508/1509 Data Sheet, 20-Pin Flash, 8-bit Microcontrollers.

TEXAS INSTRUMENTS



UCC27221
UCC27222

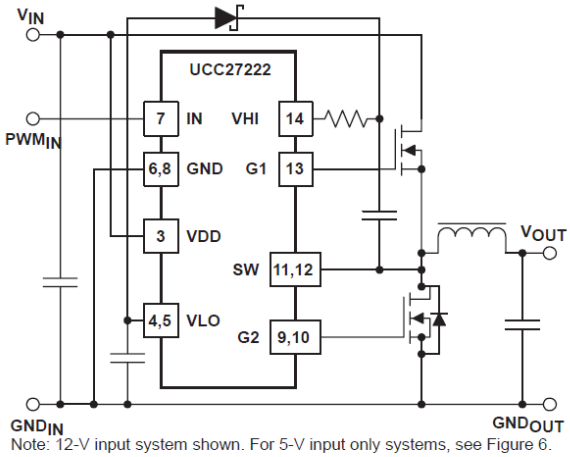
SLUS486B – AUGUST 2001 – REVISED JULY 2003

HIGH-EFFICIENCY PREDICTIVE SYNCHRONOUS BUCK DRIVER

FEATURES

- **Maximizes Efficiency by Minimizing Body-Diode Conduction and Reverse Recovery Losses**
- **Transparent Synchronous Buck Gate Drive Operation From the Single Ended PWM Input Signal**
- **12-V or 5-V Input Operation**
- **3.3-V Input Operation With Availability of 12-V Bus Bias**
- **On-Board 6.5-V Gate Drive Regulator**
- **±3.3-A TrueDrive™ Gate Drives for High Current Delivery at MOSFET Miller Thresholds**
- **Automatically Adjusts for Changing Operating Conditions**
- **Thermally Enhanced 14-Pin PowerPAD™ HTSSOP Package Minimizes Board Area and Junction Temperature Rise**

FUNCTIONAL APPLICATION DIAGRAM



Note: 12-V input system shown. For 5-V input only systems, see Figure 6.

APPLICATIONS

- **Non-Isolated Single or Multi-phased DC-to-DC Converters for Processor Power, General Computer, Telecom and Datacom Applications**

DESCRIPTION

The UCC27221 and UCC27222 are high-speed synchronous buck drivers for today's high-efficiency, lower-output voltage designs. Using Predictive Gate Drive™ (PGD) control technology, these drivers reduce diode conduction and reverse recovery losses in the synchronous rectifier MOSFET(s). The UCC27221 has an inverted PWM input while the UCC27222 has a non-inverting PWM input.

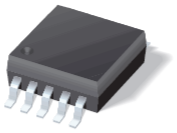
Predictive Gate Drive™ technology uses control loops which are stabilized internally and are therefore transparent to the user. These loops use no external components, so no additional design is needed to take advantage of the higher efficiency of these drivers.

This closed loop feedback system detects body-diode conduction, and adjusts deadtime delays to minimize the conduction time interval. This virtually eliminates body-diode conduction while adjusting for temperature, load- dependent delays, and for different MOSFETs. Precise gate timing at the nanosecond level reduces the reverse recovery time of the synchronous rectifier MOSFET body-diode, reducing reverse recovery losses seen in the main (high-side) MOSFET. The lower junction temperature in the low-side MOSFET increases product reliability. Since the power dissipation is minimized, a higher switching frequency can also be used, allowing for smaller component sizes.

The UCC27221 and UCC27222 are offered in the thermally enhanced 14-pin PowerPAD™ package with 2°C/W θ_{jc}.

Predictive Gate Drive™ and PowerPAD™ are trademarks of Texas Instruments Incorporated.

TEXAS INSTRUMENTS



TPS60500, TPS60501
TPS60502, TPS60503

SLVS391B – OCTOBER 2001 – REVISED FEBRUARY 2002

HIGH EFFICIENCY, 250-mA STEP-DOWN CHARGE PUMP

FEATURES

- Regulated 3.3-V, 1.8-V, 1.5-V, or Adjustable Output Voltage
- Up to 250-mA Output Current
- 1.8-V to 6.5-V Input Voltage
- Up to 90% Efficiency
- Output Voltage Tolerance 3% Over Line, Load, and Temperature Variation
- Device Quiescent Current Less Than 40 μA
- Output Voltage Supervisor Included (Power Good)
- Internal Soft Start
- Load Isolated From Battery During Shutdown
- Overtemperature and Overcurrent Protected
- Micro-Small 10-Pin MSOP Package
- EVM Available, TPS60500EVM-193

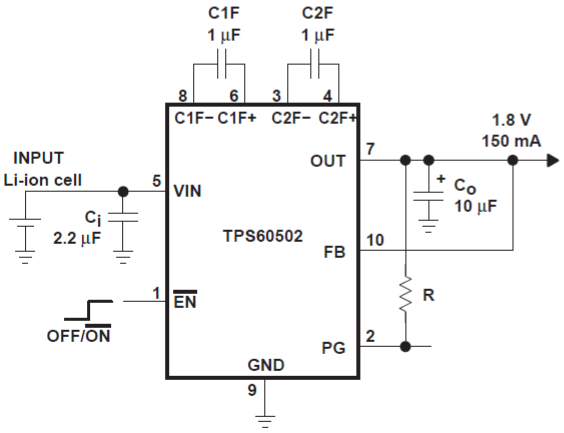
APPLICATIONS

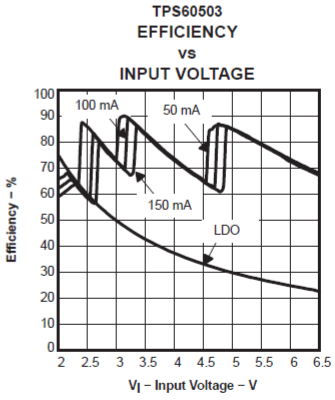
- Personal Digital Assistants
- DSP Core Supply
- Cellular Phones
- Portable Instruments
- Internet Audio Player
- PC Peripherals
- USB Powered Applications

DESCRIPTION

The TPS6050x devices are a family of step-down charge pumps that generate a regulated, fixed 3.3-V, 1.8-V, 1.5-V, or adjustable output voltage. Only four small ceramic capacitors are required to build a complete high efficiency dc/dc charge pump converter. To achieve the high efficiency over a wide input voltage range, the charge pump automatically selects between three different conversion modes. The output can deliver a maximum of 250-mA output current. The power good function supervises the output voltage and goes high when the output voltage rises to 97% of its nominal value.

Typical Application Circuit





List of Publications

1- Monaf S. Tapou, Hamed S. Al-Raweshidy, Maysam Abbod, Manal J. Al-Kindi; "A Buck Converter for DVS Compatible Processors in Mobile Computing Applications Using Fuzzy Logic implemented in a RISC based Microcontroller," *Proceedings of the 2nd International Conference on Circuits, Systems, Control, Signals (CSCS'11)*, 26-28 Sep. 2011. Prague, Czech Republic.

2- Monaf S. Tapou, Hamed S. Al-Raweshidy:" A RISC Microcontroller Based Voltage Regulator Module with Fuzzy Logic Controller for Processor Core in Mobile Systems," *Proceedings of the First International Conference on Future Communication Networks (ICFCN'12)*. 10-12 April 2012, Baghdad Iraq.

3- Monaf S. Tapou, Hamed S. Al-Raweshidy," High Efficiency Smart Voltage Regulating Module for Modern Mobile Microprocessor Core: *Submitted to the IEEE Circuits and Systems Magazine*, Pending Reviewing.