HIGH FREQUENCY LINK UPS SYSTEM

A thesis submitted for the degree of Master of Philosophy

By

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Dedicated to:

My beloved family, wife, son and daughters

ABSTRACT

The main aim of this thesis is to propose, design, simulate and build a new UPS system which can be used for compact applications. The idea of the proposed system is to operate the transformers within the UPS at high frequency so that the size and the weight are kept to minimum. In order to achieve this aim, the transformer within the UPS system is operated at high frequency; however it also carries two 50 Hz waveforms at 180 phase shift so that the transformer does not see this 50 Hz frequency. A cycloconverter is then used to reconstruct the 50 Hz waveform for the UPS output.

The UPS system is simulated using PSPICE software at high frequency link of 500 Hz, 1 kHz, 5 kHz and 10 kHz. The simulation results show that the transformer only passes the high frequency component while the 50 Hz frequency is 'hidden' within the transformer. The proposed UPS system is then built using MOSFETs IRF740 as the main switches for the inverter and cycloconverter circuits. A Chipkit-uno32-development-board is used to control the MOSFET switches. Simulated and practical results show the viability of the proposed UPS system.

ACKNOWLEDGEMENTS

First and foremost I offer my sincerest gratitude to my first supervisor, Dr M. Darwish, who has supported me throughout my research with his endurance and knowledge whilst permitting me the opportunity to work by my own. I attribute the level of my Masters Philosophy degree to his encouragement and effort and without him this thesis, too, would not have been completed or written. One simply could not wish for a better or friendlier supervisor.

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ABBREVIATIONS

AC:	Alternating Current
DC:	Direct Current
EMI:	Electro Magnetic Interference
$f_{c:}$	Carrier (link) frequency
$f_{s:}$	Switching frequency
MOSFET:	metal–oxide–semiconductor field-effect transistor
PLL:	Phase-Locked Loop
PSPICE:	Personal Simulation Program with Integrated Circuit Emphasis
RMS:	Root Mean Square
S:	Semiconductor switch
SPWM:	Sinusoidal Pulse Width Modulation
THD:	Total Harmonic Distortion
U:	DC load voltage
UPS:	Uninterruptible Power Supply
UPWM:	Uniform Pulse Width Modulation
V:	Volt

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CHAPTER 1: INTRODUCTION

1.1 General

According to a Copper Development Association survey [1], power quality problems cost British industry £200 million/year. Consequential losses of a single failure on critical systems may easily exceed this value. In USA $50 billion per year is lost as a result of power quality breakdown [1]. This large amount of money is mainly insurance compensations due to power failure or due to poor quality of the power supplied to critical loads. With the increase number of non-linear loads (computers, TV sets, etc.), this power quality problem will only get worse. Some critical loads require zero tolerance particularly in computer systems as they are getting more and more essential in the daily life and so many critical applications (money transactions, on-line shopping, etc.) will severely be affected by any type of interruption in the power supply.

Also size of computers is getting smaller and smaller and the traditional Uninterruptable power supplies (UPS) used in large computers are not appropriate for modern compact computers. Unfortunately the rate of development in UPS systems is not as fast as the rate of development in computers, and there is urgent need for compact and light UPS systems which can be used or even integrated in modern computers.

In this thesis, a new proposed UPS system is introduced in order to fulfil the need for a small, light and compact UPS topology.

1.2 Thesis aim and objectives

The main aim of this thesis is to design and build a compact and light UPS system which can be either integrated or be used alongside modern personal computers. In order to achieve this aim, the following objective are set:

- Review existing UPS systems
- Propose some configuration
- Analyse different parts within the UPS system
- Simulate the circuits used
- Build and test the proposed circuit with the appropriate controller

1.3 Structure of the thesis

The thesis is divided into six chapters. This is the introductory chapter which gives a brief argument for the need of the proposed UPS system. This chapter also contain the aim and objectives as well as the structure of the thesis.

Chapter 2 contains the literature review on available types of UPS systems in the market. It shows the principle of operations as well as the advantages and limitations of some of the main types of UPS systems. The reviewed UPS systems are then critically analysed and presented.

In order to see how the size and weight of the UPS system can be reduced, the internal distribution of existing UPS systems is analysed and the transformer is identified as the prime target for the size reduction. Chapter 3 gives an insight view on the internal distribution in on-line UPS system, with the mathematical justification for targeting the transformer. The proposed UPS system is also introduced in the same Chapter.

Chapter 4 contains the design and simulation of the proposed HF UPS system. The chapter contains simulation results to justify the claim that the 50Hz component can be 'hidden' within the transformer and then 'revealed' at the final output.

The practical work and the microcontroller are covered in Chapter 5. The chapter contain the layout of the driver and power circuits as well as the microcontroller layout.

Chapter 6 contains the conclusions of the thesis. Difficulties encountered during the execution of this research work are also reported in the conclusions. Chapter 6 also include the future work which has been risen as a result of this research work.

A comprehensive list of references followed by 6 Appendices are given at the end of the thesis.

CHAPTER 2: LITERATURE REVIEW

2.1 Introduction

Power supply consistency demand has been the essential intention for any electrical and electronics existing or even proposal future project and as the usage of the electrical power supply rose up the significance of UPS also has increased.

This chapter contains in depth literature review on types of UPS systems. The chapter shows the evolution of rotary and static UPS systems. Also the advantages and applications of different UPS systems are critically reviewed. UPS can be classified into DC and AC UPS systems as shown in Fig. 2.1. DC UPS is well used in the communication industry, while the AC types are mainly used within the power industry. In both types the main source is an AC. In DC UPS systems the mains supply is rectified and filtered in order to provide the required DC supply. Both types are discussed in the following sections in more details.

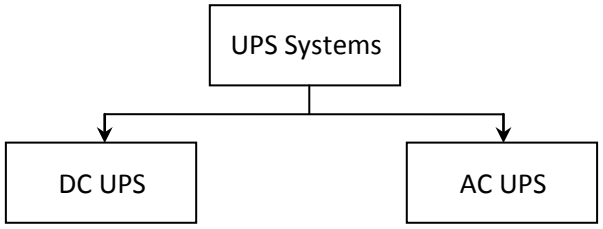


Fig. 2.1: Main classification of UPS Systems

2.2 DC UPS systems

DC UPS is mainly designed for communication devices such as hubs, switches and modems. It provides 24V DC supply from the 240V AC mains. The main aim is to ensure a stable and uninterrupted DC power to critical loads. DC UPS systems can be classified into 4 different topologies, depends on the criticality of the load. These topologies are: Battery mode; Parallel mode; Parallel mode with reducing diodes; and Changeover mode. Fig. 2.2 illustrates this classification.

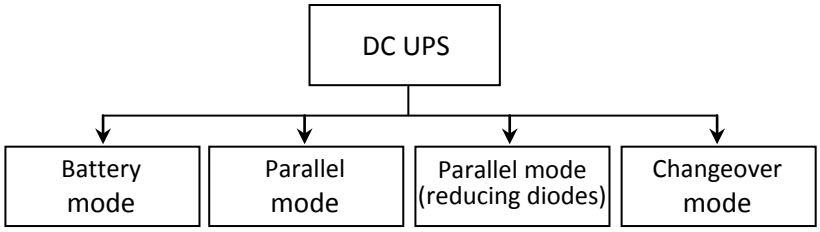


Fig. 2.2: Classification of DC UPS Systems

2.2.1 Battery mode

In this mode the mains supply feeds a rectifier circuit which is used to charge one set of batteries while the other set of batteries is supplying the load. In larger systems the rectifier circuit could be replaced with an a.c. motor coupled with d.c. generator. As it can be seen in Fig. 2.3, this configuration is a simple one; however, it is subjected to any interruption due to the finite time taken by the changeover of the two switches which are used to connect/disconnect the battery sets [2].

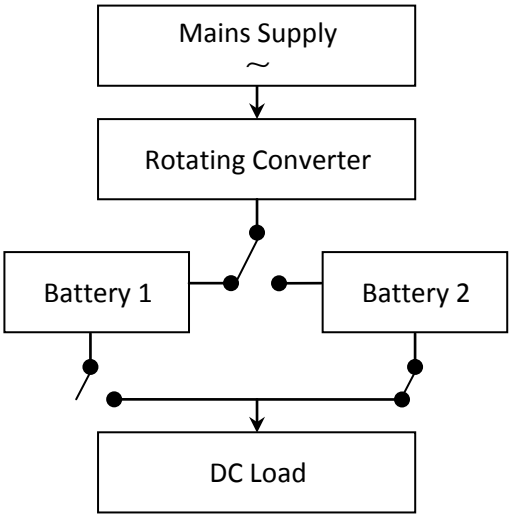


Fig. 2.3: Battery mode “Charge-discharge mode”

2.2.2 Parallel mode

In this type there are two main mode of operations; Floating mode and Standby parallel mode [2].

In the floating mode the rectifier circuit (shown in Fig. 2.4) handles the load's normal power, though it can't deal with peak power requirement. In this case the battery provides the power above the rectifier rated power or the battery can supply the rush current required by some applications.

In the standby parallel mode the rectifier always covers the load's whole power requirement. In both mode of operations, the battery operates as backup in case of power failure and the DC load is supplied directly from the battery.

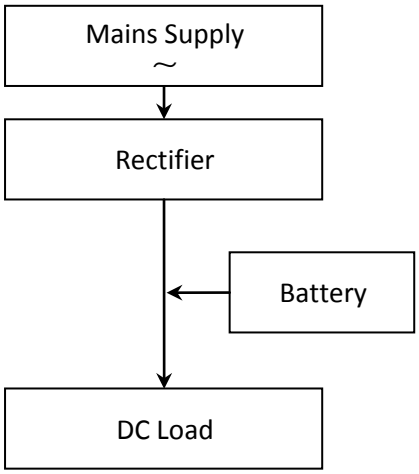


Fig. 2.4: Parallel mode

In the normal operation the rectifier is fed by mains supply at constant rate of current only and in situation of rush current the rest of current will be provided by battery set.

Standby Parallel mode: At normal operation time entire loads energy necessities is delivered by the rectifier. Fig. 2.4 demonstrates the operation in floating mode and standby parallel mode respectively.

2.2.3 Parallel mode with reducing-voltage diodes

In this mode of operation, the mains supplies the rectifier and the rectifier charges the battery as well as supplying voltage to the critical DC load via a set of reducing-voltage diodes. The battery voltage is higher than the load voltage by a value of the voltage drop across the diodes. In case of power failure, the battery voltage supplies the load and as the battery voltage drops the reducing-voltage diodes are taken out gradually to maintain an almost constant load voltage. When the power returns the reducing-voltage diodes are inserted back into the circuit gradually so maintain an almost constant load voltage. Fig. 2.5 illustrates the circuit diagram as well as the battery and load voltage waveforms [3].

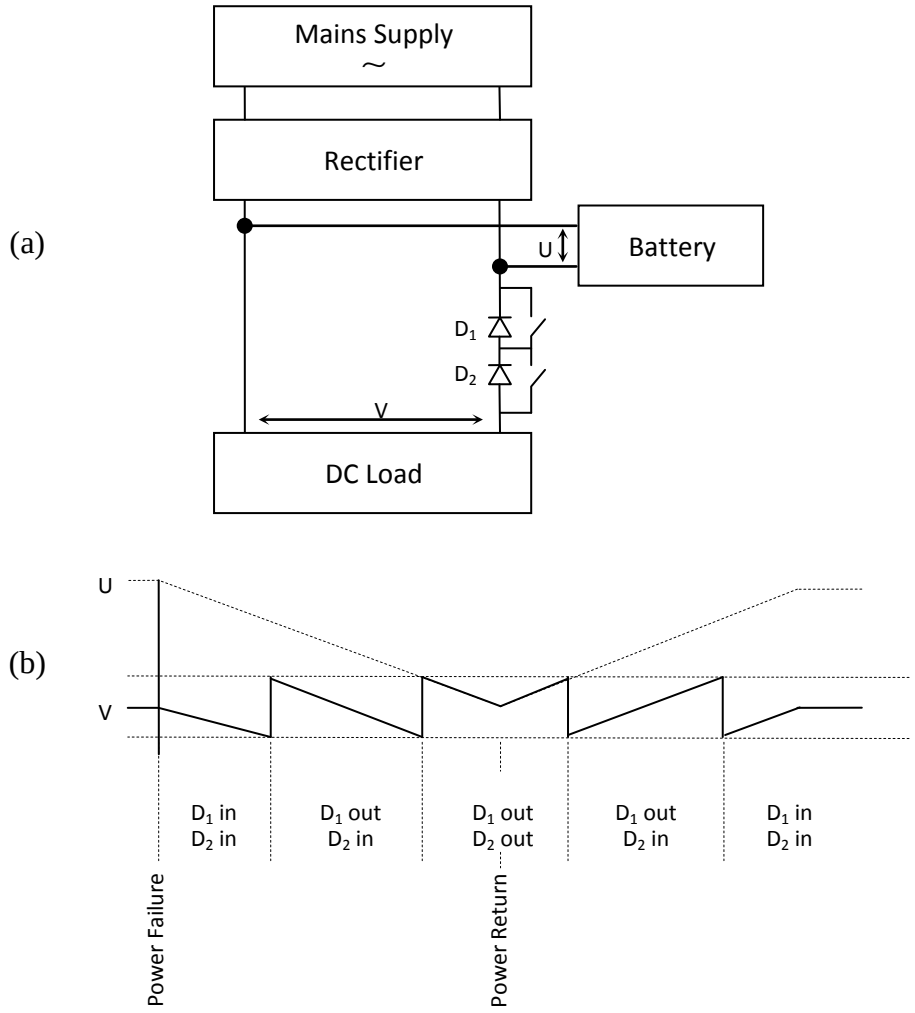


Fig. 2.5: Parallel mode (a) Circuit diagram. (b) Voltage waveforms

2.2.4 Changeover mode

In this mode the entire load energy is provided by the operating rectifier and low rate battery charging (Trickle charging) carried out by charging rectifier. The DC load is supplied by the operating rectifier and the whole battery cells are charged via the charging rectifier. In case of power failure certain sets of batteries are supplying the load; as the battery voltage drops the rest of the battery sets are inserted via switch 'S' so that the load is supplied by the entire battery sets [4]. Fig. 2.6 shows the block diagram of the changeover mode.

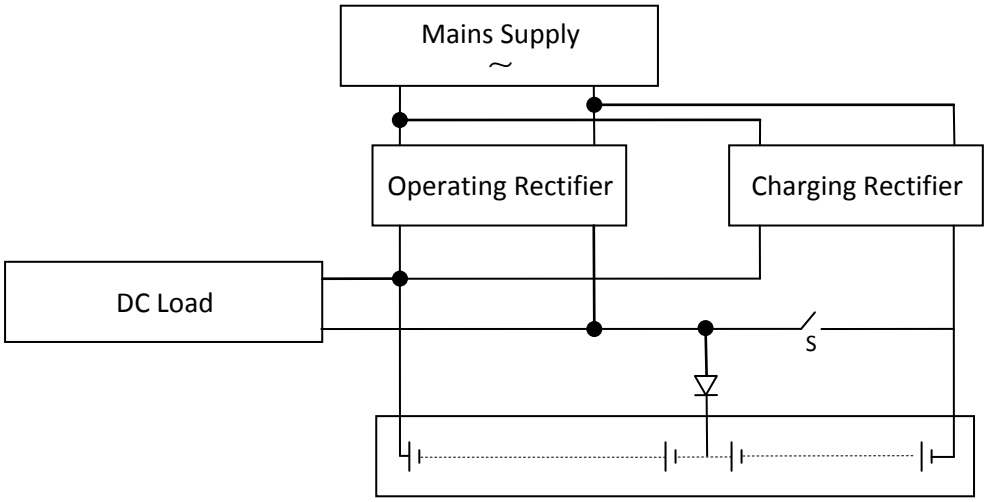


Fig. 2.6: Changeover mode with battery tap

2.3 AC UPS Systems

AC UPS system can be classified into three categories: Rotary; Hybrid and Static as shown in Fig. 2.7. They are mainly used to supply the power to critical AC loads. They could vary from a single unit which can operate as a back-up for single computer to a whole system which can be used as a back-up for an entire building (banks, hospitals, power operation

control rooms, etc.). Each of these types are discussed in the following sections with critical evaluation of each type.

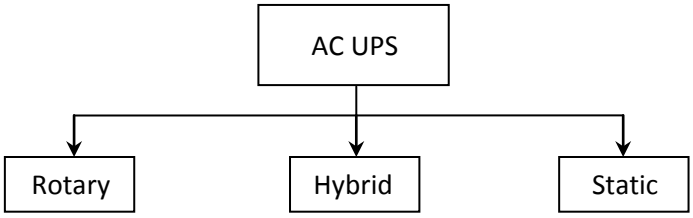


Fig. 2.7: Classification of AC UPS Systems

2.3.1 Rotary UPS Systems

In the rotary UPS system an AC motor coupled with DC machine coupled with AC Generator are used between the AC mains and the critical load [5-6]. As shown in Fig. 2.7, the AC supply operates the AC motor which is coupled with DC machine (operates as generator to charge the battery) and operate as a prime mover for the AC generator. The AC generator then generates the required voltage and frequency for the load. In case of power failure, the battery bank supplies energy to the DC machine (operates as motor) and the motor is coupled with the AC generator which then drives the load. Obviously the DC battery can be replaced with a diesel engine set for unlimited backup time (only limited by the amount of fuel used. The static bypass switch is used to provide uninterrupted power to the load in case of UPS failure. Also the static bypass is used during the maintenance of the UPS. The static bypass consists mainly of two semiconductor switches connected back-to-back. A manual bypass can also be used in case of the UPS system experiences an overload or internal failure. The manual, maintenance or service bypass allows an engineer to isolate, maintain or remove the UPS without interrupting power to the load. The static and maintenance bypass switches are discussed in details later in section 2.4. Such system has the following advantages:

- More reliable than static UPS systems (failures can be predicted easier compared to static UPS systems)
- Transient overload capability is 300% to 600% of the full load for rapid fault clearing (150% for static UPS).
- Good performance for non-linear loads (because of the low output impedance).
- Very low input current THD (<3%)
- Low EMI
- Efficiency is higher than 85%.

However rotary UPS systems suffers from the following disadvantages:

- It requires more maintenance (due to the rotary parts).
- Have a much larger size and weight compared to static ones.

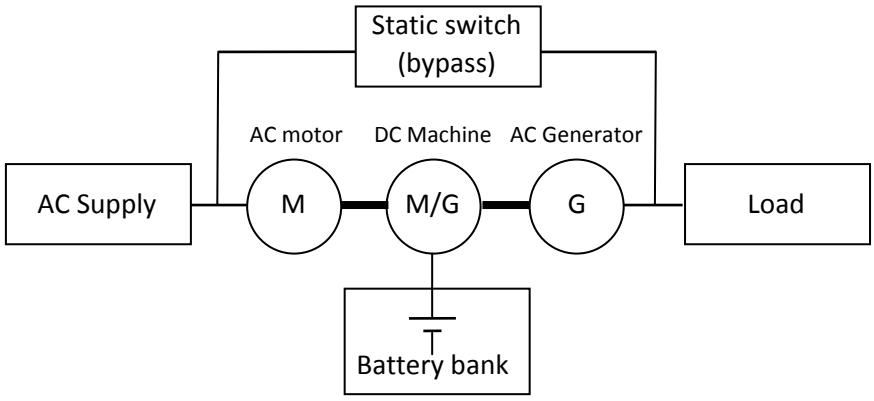


Fig. 2.8: Rotary UPS system

2.3.2 Hybrid (Static/Rotary) UPS Systems

In this system the AC motor is fed from the AC supply and drives the generator. The AC generator supplies the load. The bidirectional converter, which behaves as a rectifier, charges the battery. In case of power failure the battery supplies the AC generator via the

bidirectional converter, which operates as an inverter [7]. The AC motor drives the AC generators which feeds the load. Fig. 2.9 shows the single line diagram of such system.

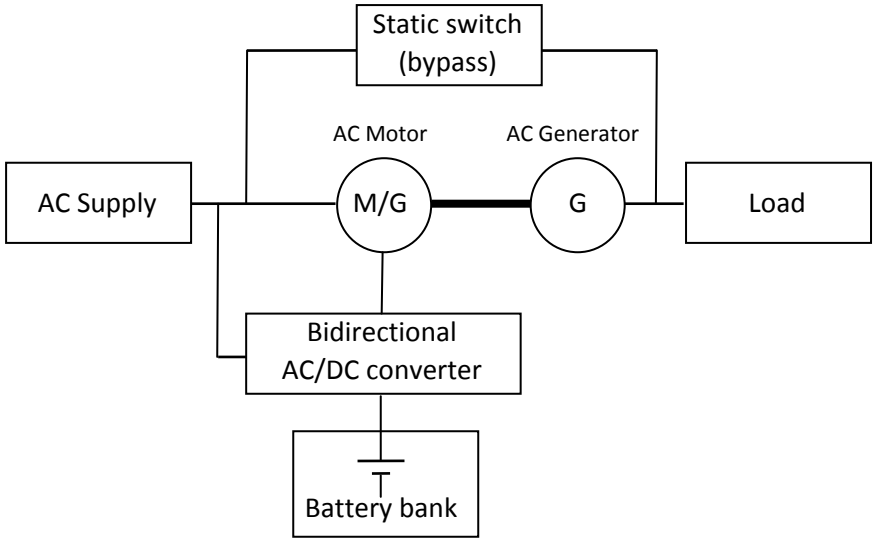


Fig. 2.9: Hybrid (static/rotary) UPS system

The hybrid UPS system has the following advantages over the static UPS:

- Low output impedance
- Low THD with non-linear loads.
- Higher reliability
- Better isolation

The low maintenance cost (because of the missing mechanical commutator) makes this system more attractive over the rotary UPS system.

2.3.3 Static UPS Systems

In static UPS system the main components are static ones (rectifier, inverter, transformer, battery charger, battery, etc.) rotary parts are not used. Such system is smaller in size and weight (for the same power rating) compared to rotary systems. It is also much less noisier

than rotary UPS systems. Static UPS are classified into different number of categories. Some are classified according to power ratings; some are classified according to the presence or absence of a short interruption time and some according to the state of the inverter within the UPS (on-line or off-line) [8-14]. Fig. 2.10 illustrates the UPS classification according to the inverter state which is adopted in this thesis. Each of these types is reviewed in more details in the following sub-sections.

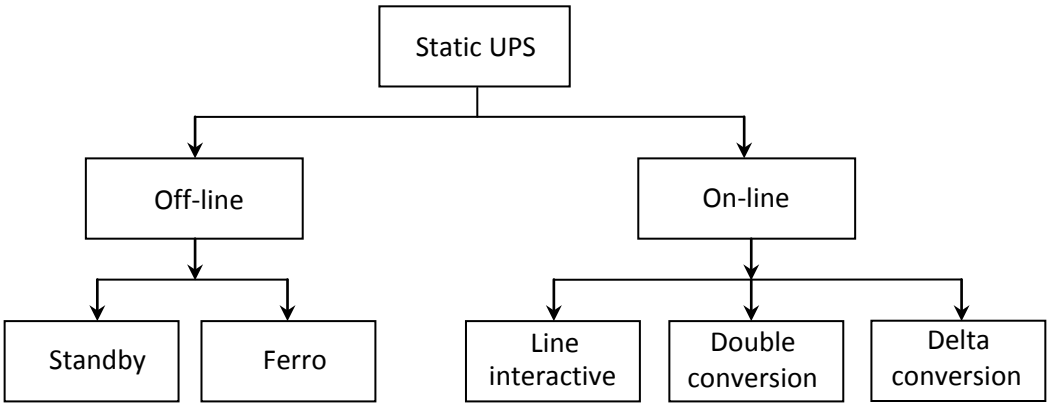


Fig. 2.10: Classification of Static UPS Systems

2.3.3.1 Off-line UPS System

In these types of UPS the mains supply is connected directly to the load without any dc link. In some applications filter is used to filter out any noise in the mains. In case of power failure the inverter which is usually off-line (hence its name) becomes active in the UPS system. Two types of 'off-line' UPS system are discussed in this chapter; the Standby and the Ferro UPS systems.

2.3.3.1.1 Standby Off-line UPS System

In normal operation the supply feeds the load via filtering circuit in order to remove any distortion from the mains. The AC/DC is trickle charging the battery set. In case of power failure or if the interruption is outside the allowable limit, then the inverter circuit inverts the DC battery voltage to AC in order to supply the load. The AC/DC converter is rated at a much lower power rating than the rectifier/charger in an on-line UPS system as will be shown later in section 2.3.3.1.3. In this application the inverter is rated at 100% of the load's demand. The duration of the switching time depends on the starting time of the inverter. The transfer time is usually about ¼ line cycle which is enough for most of the applications. The circuit topology of this system is shown in Fig. 2.11. The simple design, low cost and the small size of this UPS make it attractive for several low power applications. However the lack of real isolation between the load and the AC supply, the absence of the output voltage regulation, and the poor performance with non-linear loads, limit the application of this type of UPS to < 2kVA.

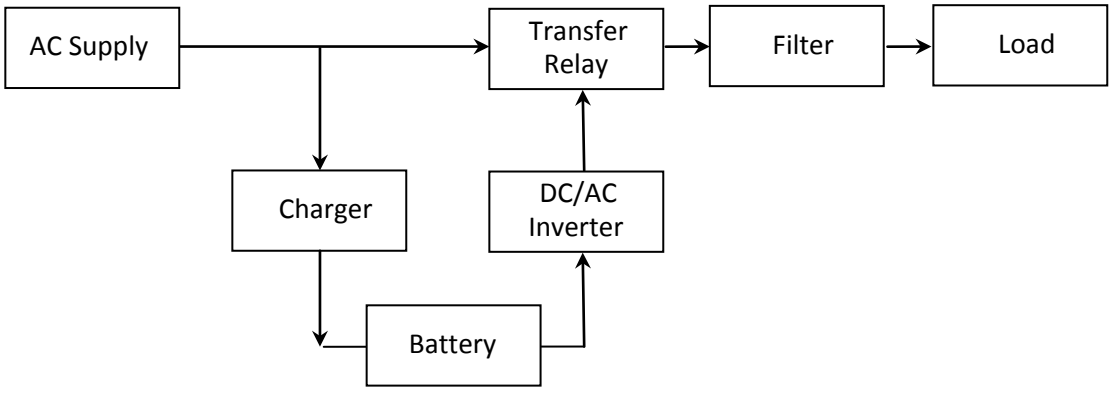


Fig. 2.11: Standby Off-line UPS System

2.3.3.1.2 Ferro Off-line UPS System

The Ferro off-line UPS system is based on using the ferroresonant transformer as the main unit in its design. The ferroresonance is a resonance situation between the nonlinear inductance of the transformer and a capacitor connected to the tertiary windings [15-17]. In this system (as shown in Fig. 2.12) the ferroresonant transformer acts as conditioner for the mains supply during the normal mode of operation. The transformer maintains a constant output voltage even with a varying input voltage and it provides good protection against line noise. The ferroresonant transformer will also maintain constant output on its secondary briefly when a total outage occurs. This UPS system has the following advantages:

- Constant output voltage given substantial variations in input voltage.
- Harmonic filtering capability between the power source and the load.
- The ability to 'ride through' brief losses in power by keeping a reserve of energy in its resonant tank circuit.
- The ferroresonant transformers are also highly tolerant of excessive loading and transient (momentary) voltage surges.

The ferroresonant UPS system also suffers from the following disadvantages:

- They waste a lot of energy (due to hysteresis losses in the saturated core), generating significant heat in the process
- They are intolerant of frequency variations, which mean they don't work very well when powered by small engine-driven generators having poor speed regulation.
- Voltages produced in the resonant winding/capacitor circuit tend to be very high, necessitating expensive capacitors and presenting the service technician with very dangerous working voltage.

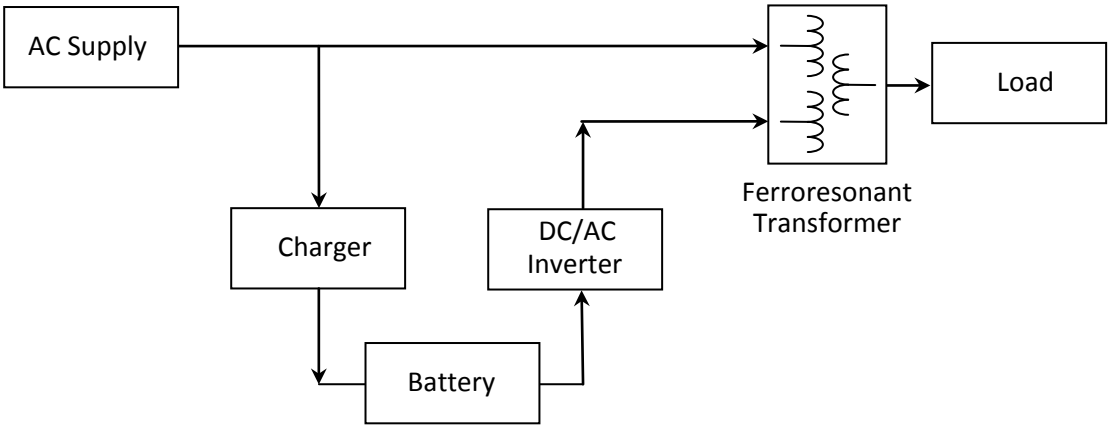


Fig. 2.12: Ferro Off-line UPS System

2.3.3.2 On-line UPS System

In this type of UPS systems the inverter is always in operation. The load should not see any interruption due to switching over in case of power failure. The load is always fed from the inverter either through the dc battery or from the output of the rectifier circuit. Such system has 100% effectiveness since there is no interruption in the load. Three topologies are derived from the On-line UPS system: Line interactive, double conversion and the delta conversion.

2.3.3.2.1 Line Interactive On-line UPS System

This is somehow similar to the off-line UPS system. The only difference is that during the normal operation the inverter is not completely 'off-line' as in the case of the off-line UPS system, but it operates as AC/DC converter in order to charge the battery. In normal

operation the load is fed directly from the supply. In case of power failure the load is fed from the converter which now operates as DC/AC inverter which is fed from the battery. This system may see very small interruption due to the transition between the normal mode and the standby mode of operations [18, 19]. Fig. 2-13 illustrates a block diagram of this UPS system.

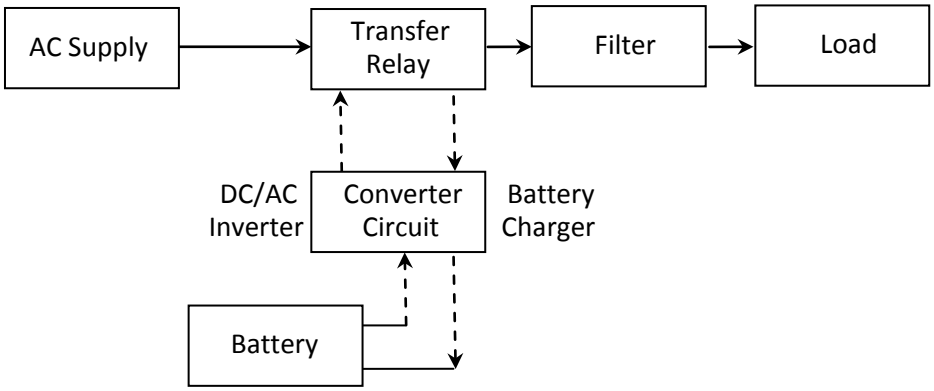


Fig. 2.13: Line Interactive On-line UPS System

2.3.3.2.2 Double Conversion On-line UPS System

During the normal mode of operation, the power to the load is continuously supplied via the rectifier/charger and inverter [20, 21]. A double conversion (AC/DC and DC/AC) takes place and it allows very good line conditioning. The AC/DC converter charges the battery set and supplies power to the load via inverter. Therefore, it has the highest power rating in this topology (higher cost).

When the AC input voltage is outside the preset tolerance, the inverter and battery maintain continuity of power to the load. The duration of this mode is the duration of the preset UPS backup time or until the AC line returns within the preset tolerance. When the AC line returns, a phase-locked loop (PLL) makes the load voltage in phase with the input voltage and after that the UPS system returns to the normal operating mode. Fig. 2.14 shows the block diagram of this type of UPS system.

The double conversion in on-line UPS system has the following advantages and disadvantages:

Advantages:

- Very wide tolerance to the input voltage variation and very precise regulation of output voltage.
- No transfer time during the transition from normal to stored energy mode.
- Capability of regulate or change output frequency.

Disadvantages:

- Low power factor (Due to the rectifier)
- High THD at the input (Due to the rectifier)
- Low efficiency (Due to double conversion)

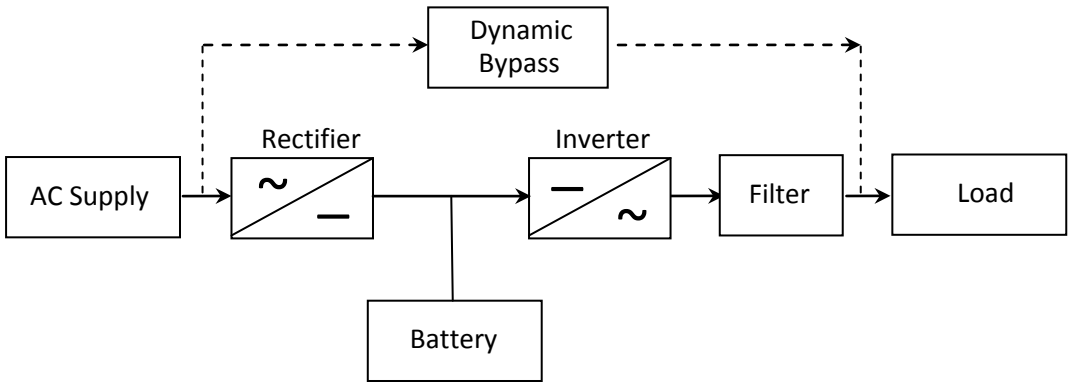


Fig. 2.14: Double Conversion On-line UPS System

2.3.3.2.3 Delta Conversion On-line UPS System

Due to the disadvantages of previous UPS systems the delta conversion topology was developed recently [22, 23]. There are two converters used in this topology, a series converter which can be used as current regulator during the normal mode of operation, and a parallel converter, which can be used as a voltage regulator during the normal mode of operation. In case of power failure the circuit operates in a similar manner as the double conversion on-line UPS system. The name 'delta' is derived from the fact that the UPS compensate the difference between the input and output of the UPS system. Fig. 2.15 shows the block diagram of delta conversion on-line UPS system.

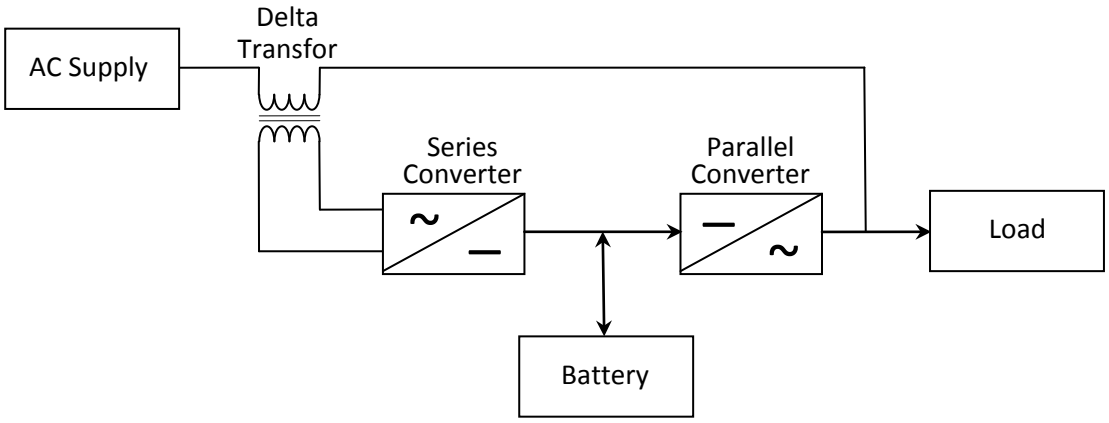


Fig. 2.15: Delta Conversion On-line UPS System

2.4 Bypass in UPS systems

Most UPS systems employ at least one kind of bypass. The bypass could be used to connect the mains directly to the load in case of malfunction of the UPS system (static bypass) or in case of UPS maintenance (manual bypass). Both bypass systems are covered in the following sections in more depth.

2.4.1 Static Bypass

Almost all on-line UPS systems are using static bypasses [24, 25]. This is mainly a backup in case the main line of the on-line UPS system (rectifier -dc link – battery - inverter) fails or in case of severe overload, the static switch connects the mains to the load automatically. Also the static switch is used to synchronise the mains with the load. The static bypass should provide uninterrupted transfer to the mains in less than 1/4 cycle.

2.4.2 Maintenance Bypass

This maintenance bypass which is also known as a manual bypass is used after the isolation of the UPS through the static switch in order to carry out any maintenance work [26, 27]. Fig. 2.16 shows the block diagram of the static and maintenance bypass switches.

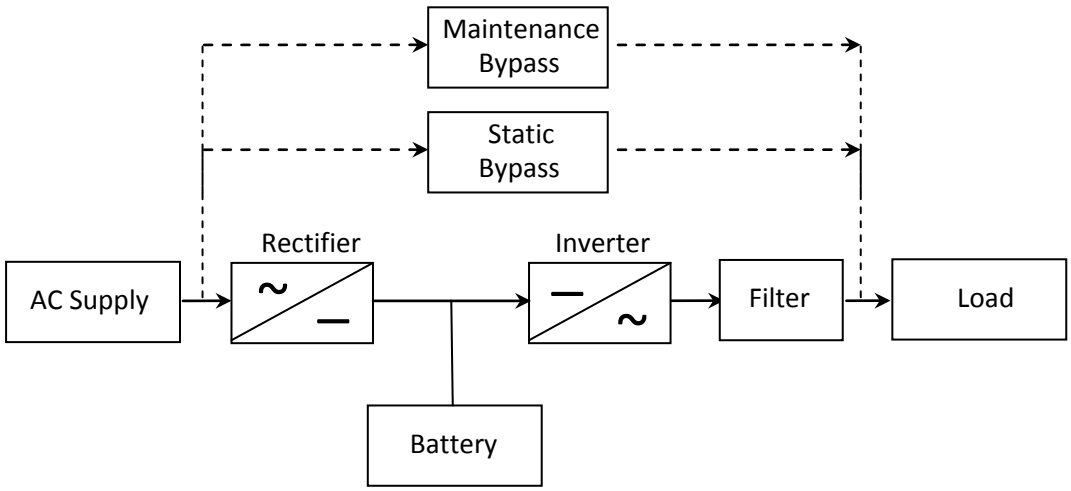


Fig. 2.16: Bypass in On-line UPS Systems

2.5 Comparison Summary of AC UPS Systems

Different UPS systems are used for different applications. For example, a rotary UPS could be the ideal one for power backup for buildings like hospitals and it can be placed in the basement where there is no restriction with place and the generated noise could be confined. On the other hand, an on-line UPS system could be used for critical loads where zero interruption is required and also where noise is an issue. Size and weight mainly depend on the stand by time. For example a UPS system with 10 minutes standby time is much smaller than a UPS with 60 minutes standby time. Table 2.1 gives a brief comparison of different types of UPS systems discussed in this chapter.

Topology / Features	Effectiveness / reliability	Efficiency	THD	Overload capability	Size / weight	By pass option
Rotary	Effective Unlimited standby time	Medium	Very low	300% - 600%	Bulky and heavy (motor generator sets)	Yes
Hybrid	V. effective Standby time depends on the battery.	Medium	Very low	300% - 600%	Bulky and heavy (motor generator sets)	Yes
Standby off-line	Low. (As interruption occurs during transition)	Very high	Low	~ 150%	Bulky and heavy (Transformers)	No
Ferro	Low. (As interruption occurs during transition)	Very high	Low	~ 150%	Bulky and heavy (Transformers)	No
Line interactive	High	High	High	~ 150%	Bulky and heavy (Transformers)	Yes
Double conversion	High	High	High	~ 150%	Bulky and heavy (Transformers)	Yes
Delta conversion	High	Very high	Low	~ 150%	Bulky and heavy (Transformers)	Yes

Table 2.1: Comparison Summary of AC UPS Systems

2.6 Summary

This chapter contains literature review on types of UPS systems. The chapter discusses the operation and the features together with the block diagrams of different types of UPS systems. It can be seen from the comparison summary shown in Table 2.1 that the size and weight is a common concern with all types of UPS systems. For example, as the size of computers are getting smaller and smaller, the UPS systems used as backup for these computers are not keeping the same pace in terms of size reduction. The proposed UPS system in this research work is focused mainly on finding a technique in order to reduce the size and weight of the UPS systems. In Chapter 3, the internal components of a typical on-line UPS system are analysed in order to identify which of these component(s) can be reduced in size/weight.

CHAPTER 3: Internal Distribution of On-line UPS System

3.1 Introduction

At the end of Chapter 2 it can be seen that the large size and the heavy weight is common feature of all UPS systems. In order to see how the reduction in size and weight of UPS systems can be achieved, a more detail diagram of an on-line UPS system is necessary. In this chapter a breakdown of a typical on-line UPS system is presented with investigation of which component(s) can be reduced in size/weight.

3.2 On-line UPS Components

In a typical single-phase UPS system the mains as well as the load voltages (load connected to the UPS) are about 240V (or 110 in USA). For safety reason the DC link should not be at high voltage, therefore two transformers are required; one to step down the AC voltage before rectification and the other to step up the voltage after the inverter. A typical block diagram for such system could be presented in Fig. 3.1.

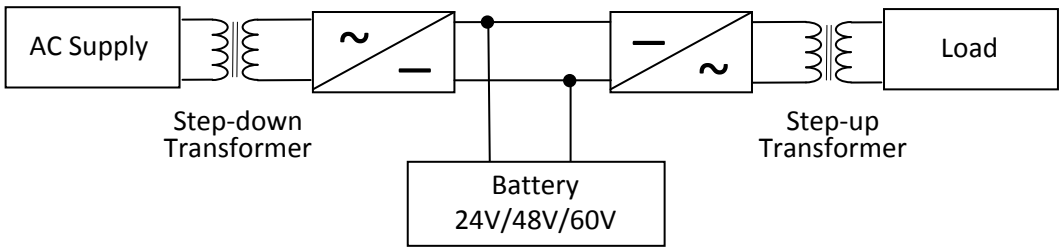


Fig. 3.1: On-line transformer-based UPS System

Since the rectifier circuit converts the 240V rms single-phase AC supply into 339V DC voltage, it is necessary to step-down the voltage before rectification so that a low voltage DC link (24V, 48V, or 60V) can be achieved at the DC link. A step-up transformer is required to

step up the AC voltage back into 240 after the inverter circuit. It is obvious that the transformer is the heaviest and largest component within the UPS system and two transformers within a single UPS will make it even heavier and bulkier. A distribution of the components within an on-line UPS system is illustrated in Fig. 3.2

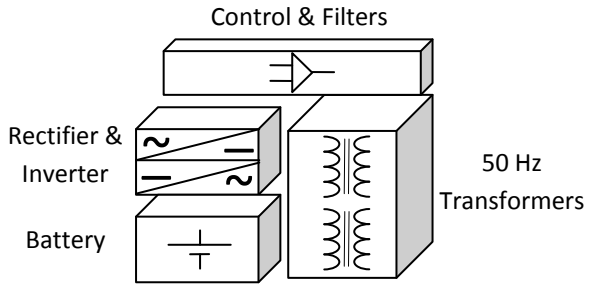


Fig. 3.2: Component distribution in on-line UPS system

It is obvious that if the size and weight of the two transformers are reduced, then the size and weight of the entire UPS system will also be reduced.

$$Let\ \emptyset = \emptyset_{max} \sin \omega t \qquad [3.1]$$

Where ϕ is the flux generated within the transformer and it takes a sinusoidal shape as the applied voltage.

The voltage developed as a result of ϕ is E where:

$$E = N \frac{d\emptyset}{dt} \qquad [3.2]$$

$$E = \omega N \emptyset_{max} \cos \omega t \qquad [3.3]$$

$$\text{Hence } E_{rms} = \frac{\omega N \emptyset_{max}}{\sqrt{2}} \qquad [3.4]$$

It can be seen from equation [3.4] that for constant E_{rms}, ϕ_{max} is proportional to $1/\omega$.

Since $\emptyset_{max} = B_{max} \times core\ cross\ sectional\ area,$

Therefore, for constant B_{max}: **Core cross sectional area of a transformer is proportional to 1/f.**

The above statement is very important because it implies that by operating the transformer at high frequency the size of the transformer core will be reduced.

For example, a 20 kHz transformer would, in theory, require a core area 400 times smaller than a 50 Hz transformer for the same power. In practice, the transformer could not be quite this small as the size of the windings and insulation cannot be reduced for the same power and voltage ratings. Also a very small transformer has less surface area to dissipate the heat. However, there is still significant reduction which can be made by operating the transformer at higher frequency.

Fig. 3.3 shows the possible reduction if 20 kHz transformers are used. The high frequency transformer is discussed in more details in section 3.3.

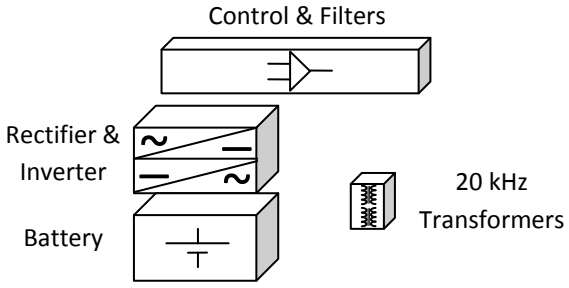


Fig. 3.3: Possible component distribution in 20 kHz on-line UPS system

It is obvious that the input frequency is 50 Hz and the output frequency should also be 50 Hz. The challenge is how to create a 20 kHz before and after each of the step-down and step-up transformers and to keep the output frequency at 50 Hz.

One way of doing that is to rectify the input AC into DC and then use an inverter to recreate the AC but at higher frequency (say 20 kHz), then use a tertiary winding transformer high-frequency transformer at turns ratio 1:1 to feed a cycloconverter which is connected to the load via a filter circuit. In case of power failure the battery feeds a "DC to 20kHz AC" inverter which feeds the same tertiary winding of the high-frequency transformer. The transformer will operate as step-up in this occasion. Fig. 3.4 shows the block diagram for such configuration.

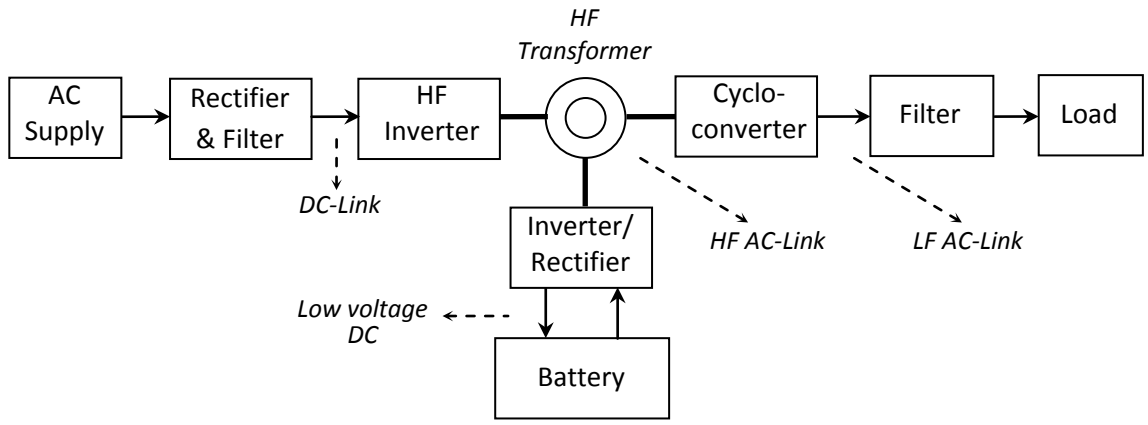


Fig. 3.4: High-frequency link UPS system (Configuration 1)

In this configuration the mains supply is converted into DC via the main rectifier circuit. The rectifier block contains a filter circuit which is mainly used to filter out the harmonics generated by the rectifier circuit and is fed back to the supply. In another word the filter is used to protect the supply from the harmonics generated from the rectifier. The HF inverter is then used to invert the DC into high frequency AC. The HF Transformer is then used to feed the cycloconverter as well as to feed the inverter/rectifier circuit (which will operate as a rectifier during this mode of operation) in order to charge the battery. The cycloconverter is used to convert the HF into 50Hz component which is then filtered and supplied to the load.

It is important to note that cycloconverters can step down an input frequency (f_i) to output frequency (f_o) under the condition that $f_o < f_i$ and f_i is an integer multiple of f_o. If a low frequency is required to be converted to a higher frequency, then a DC link is used as the one shown in Fig. 3.4.

Another configuration could also be used where only one inverter is used and the battery is charged via separate battery charger as the one shown in Fig. 3.5. In this configuration the rectifier circuit converts the AC supply into low voltage DC (using semiconductor switches as rectifying elements). The battery is charged/trickle charged from this low DC voltage. In the case of power failure the battery feeds the DC link via the rectifier circuit (which acts as a direct connection between the battery and the low voltage DC link. In both modes of operations the high frequency (HF) inverter is used to step the frequency to a higher value. The cycloconverter is then used to configure back the 50 Hz frequency required for the load. An output filter is used to remove any harmonics from the cycloconverter output.

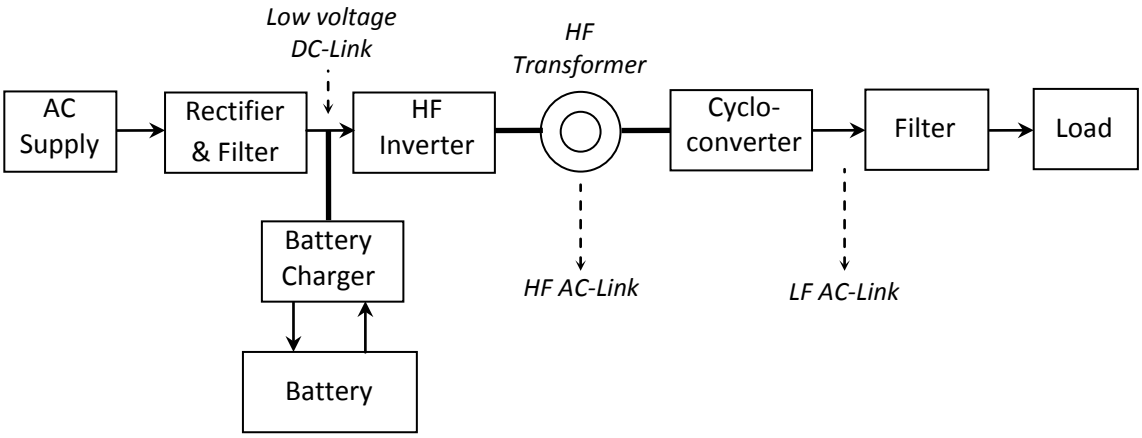


Fig. 3.5: An alternative High-frequency link UPS system (Configuration 2)

Both configurations are viable, while the first one uses transformer with three windings and two inverters, the second configuration uses transformer with two windings and one inverter. Both configurations use rectifier circuit. While the rectifier circuit in the first configuration

uses just diodes, the rectifier in the second configuration uses thyristors in order to achieve the low DC voltage.

3.3 High-Frequency Transformer

Fig. 3.6 shows the flux distribution at different frequencies [28]. It can be seen that at higher frequencies more and more core cross sectional area of the transformer becomes redundant.

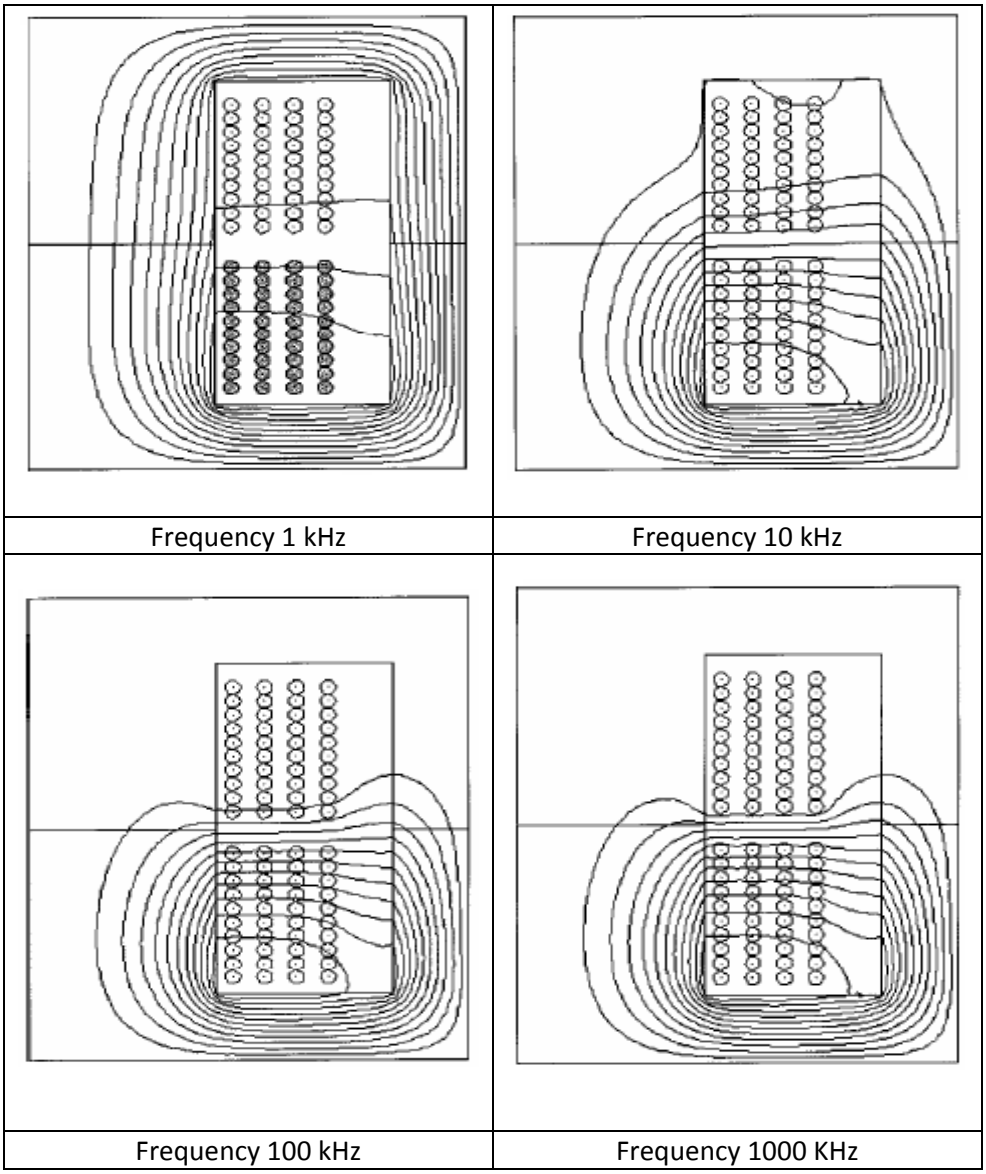


Fig. 3.6: Magnetic flux distribution at different frequencies [28]

For the purpose of clarifying the principle operation of the HF UPS system, a 500Hz, 1 kHz, 5 kHz and 10 kHz are used as the HF link. In practical design a higher frequency could be used (for example 20 kHz), the maximum value of the HF could be evaluated according to the type of the transformer used (toroidal, ferrite, iron). This is outside the scope of this research and is recommended for future work. A toroidal amorphous metglas transformer (AMT) is an ideal transformer for UPS applications. The material used in such transformer has several advantages:

- High magnetic susceptibility.
- Low coercivity (intensity of the magnetic field required to reduce the magnetization of the material to zero after the saturation point).
- High electrical resistance

Fig. 3.7 shows the toroidal transformer used in the design of the HF UPS system. Appendix A shows full details of the transformer characteristics.

Fig. 3.7: A toroidal amorphous metglas transformer (AMT)

3.4 Summary

In this chapter two HF based UPS system configurations have been introduced. In both configurations the transformer is driven at high frequency and the difference between the two configurations is mainly in the number of inverter/rectifier and in the position of the DC link. The two HF UPS configurations are designed and analysed throughout this thesis. Also in this chapter, a brief coverage of the HF transformer is introduced showing the inversely relationship between the operating frequency and the core cross section area. In Chapter 4, the full design of the HF UPS system is presented.

CHAPTER 4: DESIGN OF THE PROPOSED H.F. UPS

4.1 Introduction

Both configurations introduced in Chapter 3, use a HF link. The second configuration (shown in Fig. 3.5) is the one which is analysed fully in this chapter. It comprises a controlled rectifier circuit, a HF inverter and a cycloconverter circuit. Each of these circuits is designed and analysed in depth in this chapter with PSPICE simulation applied to all circuits. The design include harmonic analysis for each circuit.

4.2 Design and Analysis of Rectifier Circuit in HF UPS

It is required from the rectification process in the HF UPS to convert high voltage AC into low voltage DC. This is achieved by diode rectifier circuit in configuration 1. The rectifier consists of 4 diodes in a bridge configuration. The output voltage of the bridge rectifier is uncontrollable. Fig. 4.1 shows the circuit diagram of the rectifier circuit.

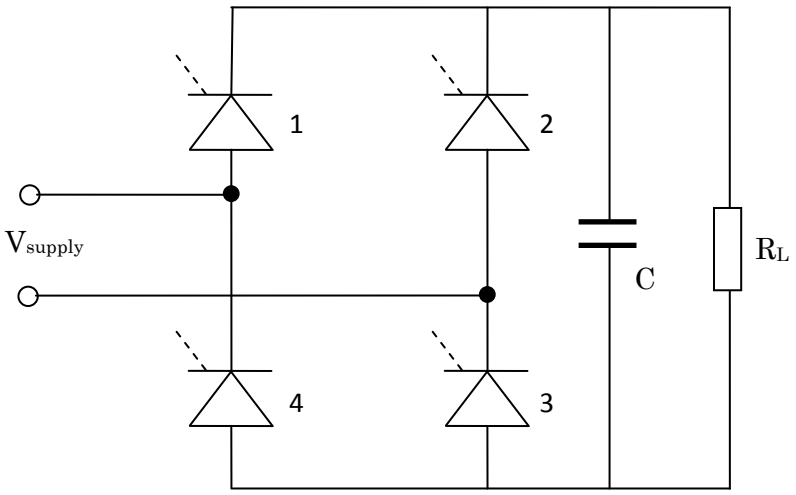


Fig. 4.1: Rectifier circuit used in UPS (Diodes in configuration 1 and Thyristors in configuration 2)

The ripple component 'r' of the output voltage depends on the load resistor 'R_L' as well as the value of the smoothing capacitor 'C' and of course the frequency of the ripple voltage. The ripple voltage can be expressed as:

$$r = \frac{1}{2\sqrt{3}} \frac{1}{fR_LC} \quad [4.1]$$

The average voltage of the output of the rectifier circuit is equal to the maximum voltage less the average ripple component and it can be expressed as:

$$V_{dc} = V_{max} - \frac{V_{max}}{2fR_LC} \quad [4.2]$$

Equation 2 shows that the output voltage of the rectifier circuit is a function of the load resistor, smoothing capacitor and the output ripple frequency (twice the supply frequency). Fig 4.2 illustrates the output and input voltage waveforms using PSPICE program.

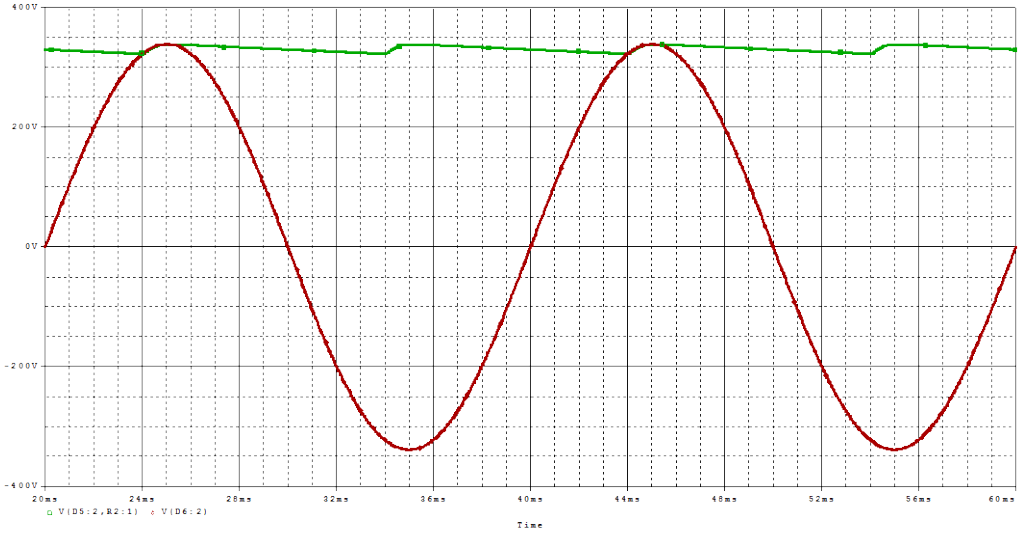


Fig. 4.2: Input and output of rectifier in UPS configuration 1

In UPS system – configuration 2, the output voltage of the rectifier circuit need to be controllable since the turn's ratio of the HF transformer is 1:1; so that the reduction in the voltage is mainly achieved through the rectifier circuit. The diodes in Fig. 4.1 are replaced with thyristors and the output voltage is controlled by controlling the thyristors triggering angle 'α'. The output voltage of the thyristors rectifier can be derived from the following equations:

$$V_{dc} = \frac{1}{\pi} \int_{\alpha}^{\pi} V_{max} \sin\theta \, d\theta \qquad [4.3]$$

$$V_{dc} = \frac{V_{max}}{\pi} [-cos\theta]_{\alpha}^{\pi} \qquad [4.4]$$

$$V_{dc} = \frac{V_{max}}{\pi} [1 + \cos\alpha] \qquad [4.5]$$

The output voltage V_{dc} is plotted against the triggering angle 'α' and is shown in Fig. 4.3. By selecting the appropriate angle the desired V_{dc} is obtained.

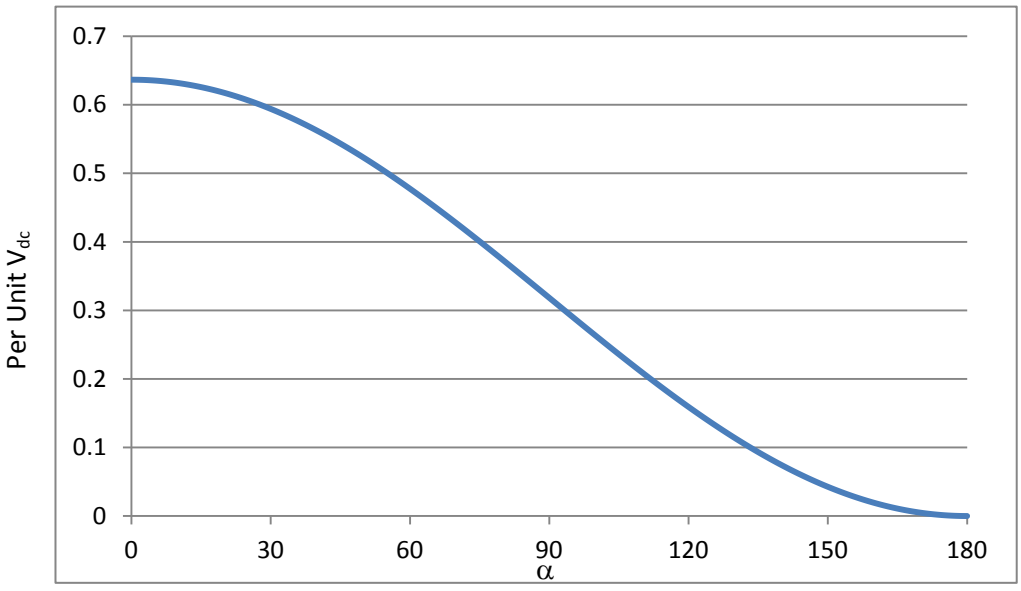


Fig. 4.3: Per unit Output voltage from the rectifier circuit in UPS configuration 2

4.3 Design and Analysis of Inverter circuit in HF UPS

The inverter circuit (shown in Fig. 4.4) consists of four semiconductor switches (MOSFETs IRF740 used in this inverter). Switches S_1 & S_3 are controlled during the positive half cycle of the output voltage and S_2 & S_4 are controlled during the negative half cycle. The manner in which the switches are controlled falls into two main categories: Uniform Pulse Width Modulation (UPWM) and Sinusoidal Pulse Width Modulation (SPWM).

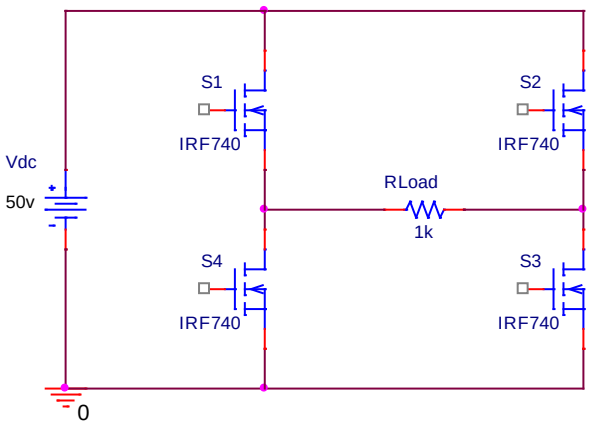


Fig. 4.4: Bridge Inverter using MOSFETs

In UPWM switches S_1 & S_3 (or S_2 & S_4) are controlled several times (M_f), where M_f is the switching or carrier frequency (f_c) / the output frequency (f_s) and is called frequency modulation. The generation of the control pulses is carried out either through hardware circuit or software programme using micro controller. This is discussed in details in Chapter 5. However in this section the control pulses are discussed regardless of the method of generation.

4.3.1 UPWM Applied to Inverter Circuit – Calculated Results

The UPWM is generated by comparing a variable DC voltage with a triangular waveform. The two signals are compared using OpAmp as a comparator and the output of the OpAmp is applied to the MOSFET driver circuits. By controlling the DC level the width of the pulses are controlled and hence the level of the output voltage is also controlled. The frequency of the triangular (or carrier) waveform (f_c) controls the switching frequency. Although it has no impact on the output voltage but it has an important effect on the Total Harmonic Distortion (THD). Fig. 4.5 illustrates how the control pulses in UPWM are generated. The ratio of the amplitude of the square waveform (A_s) to the peak value of the triangular (or carrier) waveform (A_c) is referred to as the amplitude modulation of the switch 'M_A'.

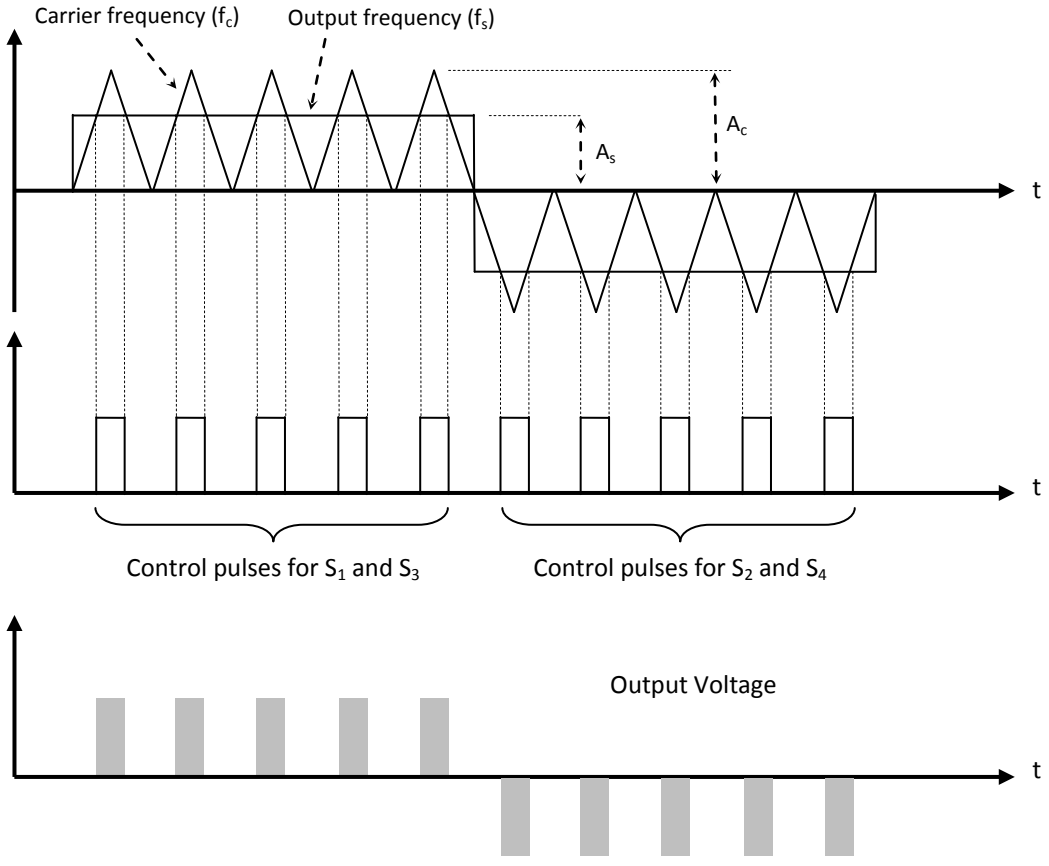


Fig. 4.5: Generation of the control pulses in UPWM Inverter

The total rms of the output voltage in the UPWM inverter circuit can be calculated from the following equation:

$$\%\frac{rms(Total)}{V_{dc}} = 100 \times \sqrt{(1-M_A} \qquad [4.6]$$

The graphs in Fig. 4.6 show the total rms of the output voltage. It is obvious from this graph that the total output voltage increases as M_A of the switches decrease. 'M_A' can be selected for the desired output voltage either through a look-up table or closed loop control and this is discussed in Chapter 5. The total output voltage is train of positive and negative pulses and equation 6 gives the total rms of this train of pulses. However, the useful power delivered by the inverter is only the fundamental power. Other harmonic voltage waveforms do not contribute to the useful power and it may cause all sort of problems (noise, heating, vibration, etc.) to the load. Therefore it is important to calculate the fundamental component of the output voltage as well as the individual harmonic components. In doing that the useful power can be precisely calculated and the harmonic power can be identified for the filter calculation purpose.

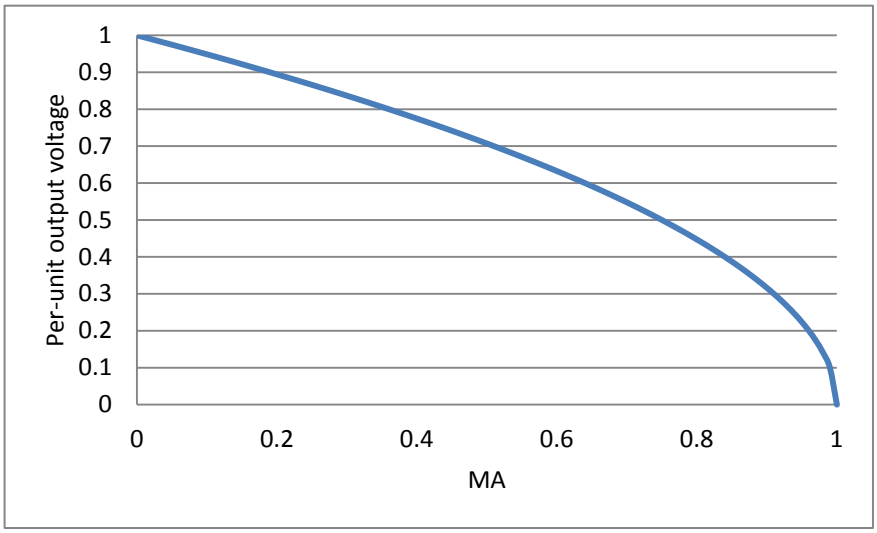


Fig. 4.6: Per-unit output voltage as function of the switches amplitude modulation.

The equation for the fundamental or any n[th] component of the output voltage can be expressed by equation 7.

$$\%\,\frac{rms(n)}{V_{dc}} = \left[\frac{2\sqrt{2}}{n\pi}\sin\left(n\frac{\pi}{M_f}(1-M_A)\right)\sum_{k=0}^{\frac{M_f}{2}-1}\sin\left(n(2k+1)\frac{\pi}{M_f}\right)\right]\times 100 \qquad [4.7]$$

It is clear from equation 4.7 that the fundamental component and each individual harmonic is influenced by both the amplitude and the frequency modulations. For example if the 3[rd] harmonic (150Hz) is to be calculated in equation 4.7 for a 50% M_A and 10 M_f; equation 4.7 becomes:

$$\%\,\frac{rms(3rd)}{V_{dc}} = \left[\frac{2\sqrt{2}}{3\pi}\sin\left(3\frac{\pi}{10}(1-0.5)\right)\sum_{k=0}^{\frac{10}{2}-1}\sin\left(n(2k+1)\frac{\pi}{10}\right)\right]\times 100 \qquad [4.8]$$

The graphs shown in Figs. 4.7 to 4.9 illustrate the variation of the % fundamental output voltage (percentage of the DC input voltage) as function of the amplitude modulation for various frequency modulations. It shows that the frequency modulation has almost no effect on the fundamental component. The fundamental in these graphs are shown for values of M_f from 3 to 20.

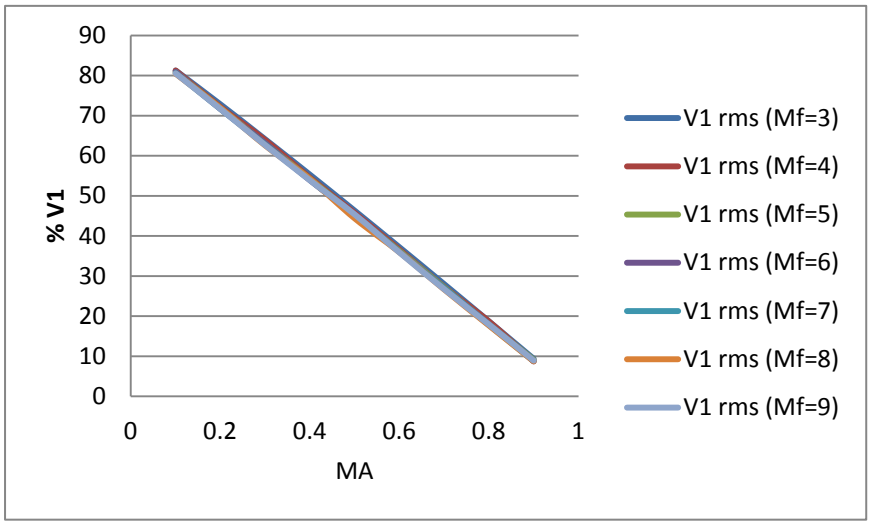


Fig. 4.7: Percentage of the fundamental voltage component for modulation indices from 3 to 9.

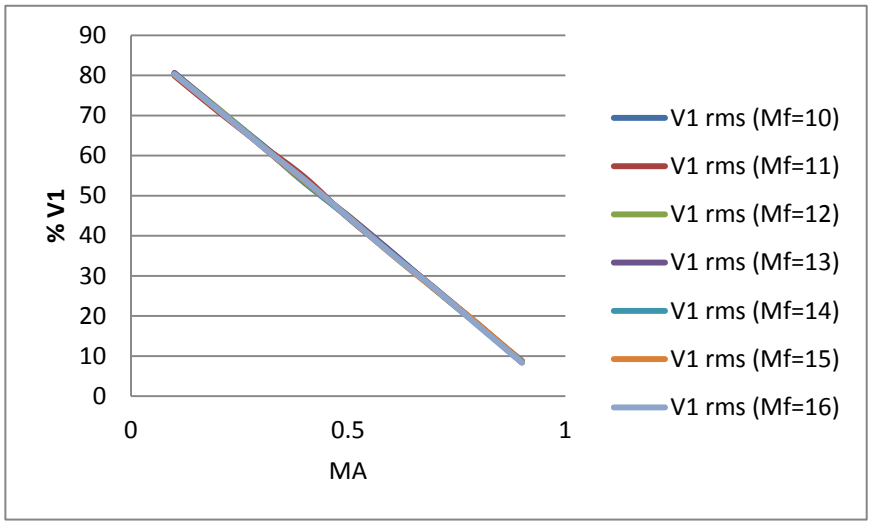


Fig. 4.8: Percentage of the fundamental voltage component for modulation indices from 10 to 16.

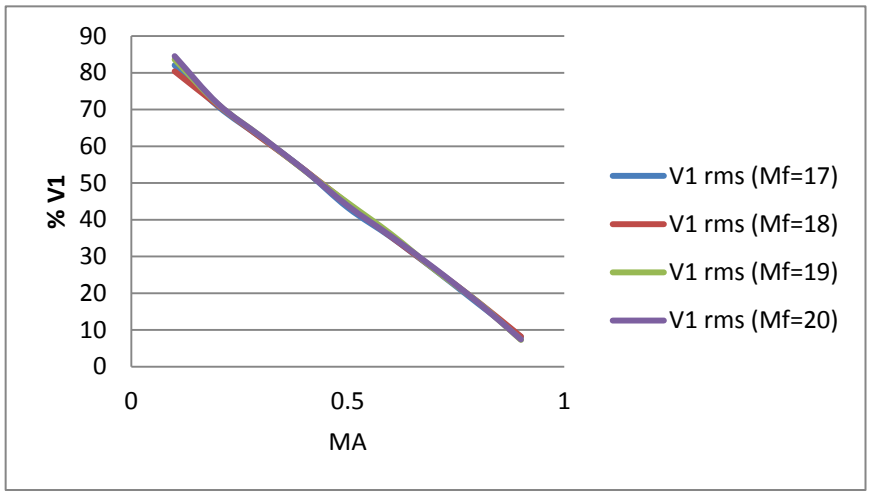


Fig. 4.9: Percentage of the fundamental voltage component for modulation indices from 17 to 20.

Instead of working each individual harmonic in the output of the inverter circuit, the total harmonic distortion is evaluated using the following equation:

$$Total\ Harmonic\ Distortion\ (T.H.D) = \frac{V_h}{V_1} \qquad [4.9]$$

where,

$$V_h = \sqrt{\left[\sum_{n=2,3,\ldots}^{\infty} V_n^2\right]} \quad or \quad V_h = \sqrt{V_{out}^2 - V_1^2} \qquad [4.10]$$

The total harmonic distortions for different frequency modulation are given in Figs. 4.10 to 4.12.

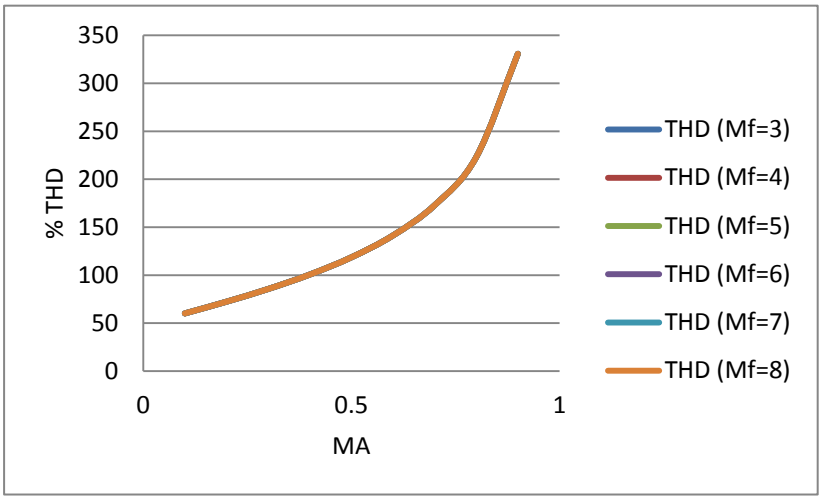


Fig. 4.10: Calculated percentage of the Total Harmonic Distortion (THD) for modulation indices from 3 to 8.

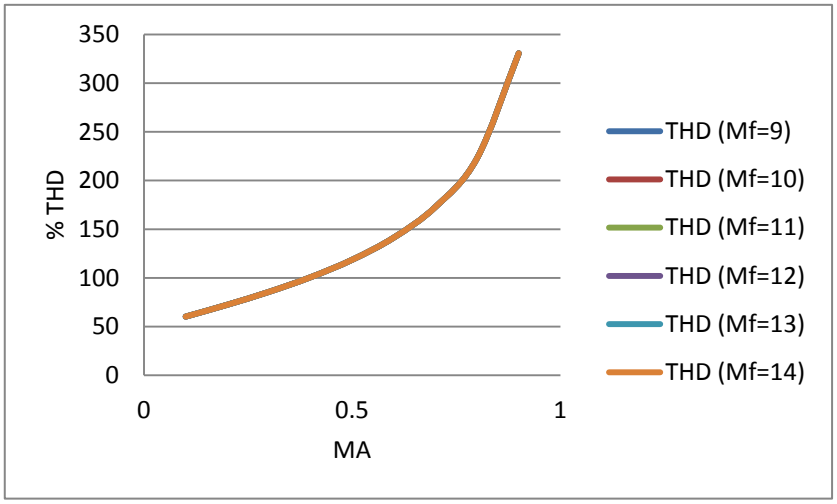


Fig. 4.11: Calculated percentage of the Total Harmonic Distortion (THD) for modulation indices from 9 to 14.

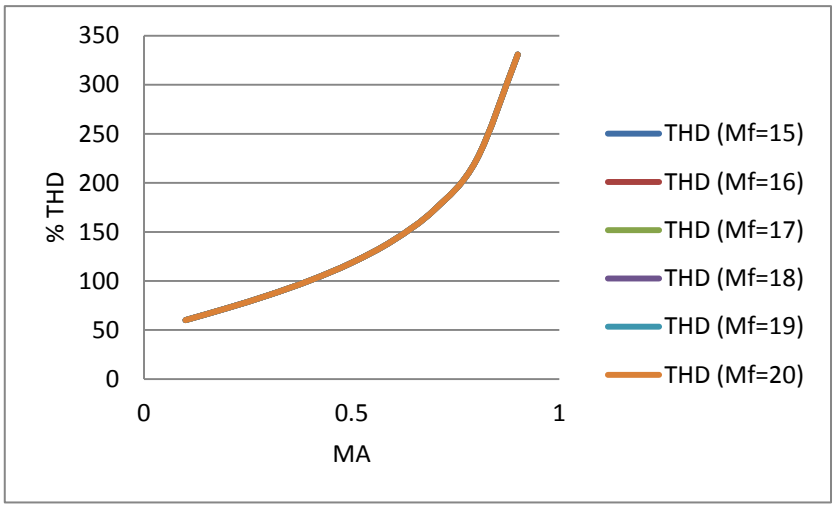


Fig. 4.12: Calculated percentage of the Total Harmonic Distortion (THD) for modulation indices from 15 to 20.

It can be seen from these figures that the THD has the same profile for different frequency modulations. Also for high amplitude modulations (small pulse width) the THD increases. The question could be: Why the frequency modulation is changed if the profile of the THD is the same? The answer to this question is that although the THD is constant (for a given value of amplitude modulation), the profile of individual harmonics are not the same for different frequency modulations.

4.3.2 UPWM Applied to Inverter Circuit – Simulated Results

The UPWM inverter circuit is simulated using MOSFETs IRF740 as switches. First the control pulses are generated by comparing square and triangular waveforms as shown in Figs. 4.13 and 4.14. The Amplitude modulation is controlled through the ratio of the DC voltage level to the amplitude of the triangular waveform. The control pulses are then applied to the MOSFET driver circuits. The amplitude modulation (M_A) shown in Fig. 4.13 is 0.4 (4V DC / 10V). The simulated results for the fundamental and the THD are shown in Figs. 4.15 to 4.17.

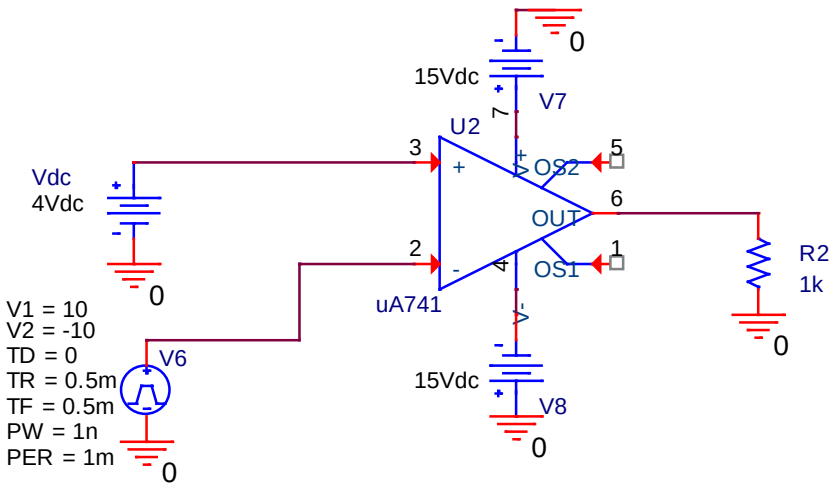


Fig. 4.13: Circuit diagram for the pulse generator

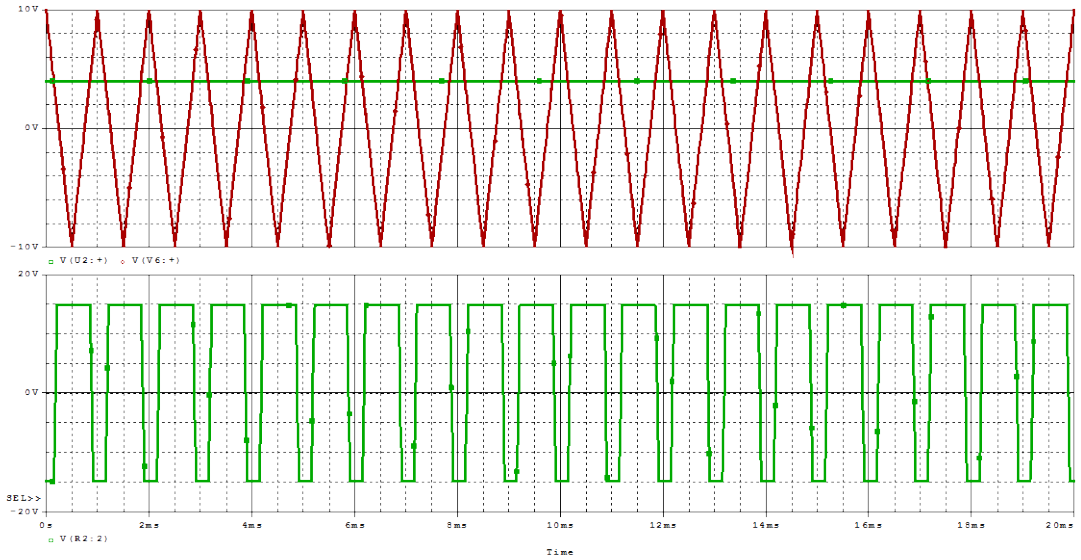


Fig. 4.14: Waveforms for the carrier, reference, and control signals

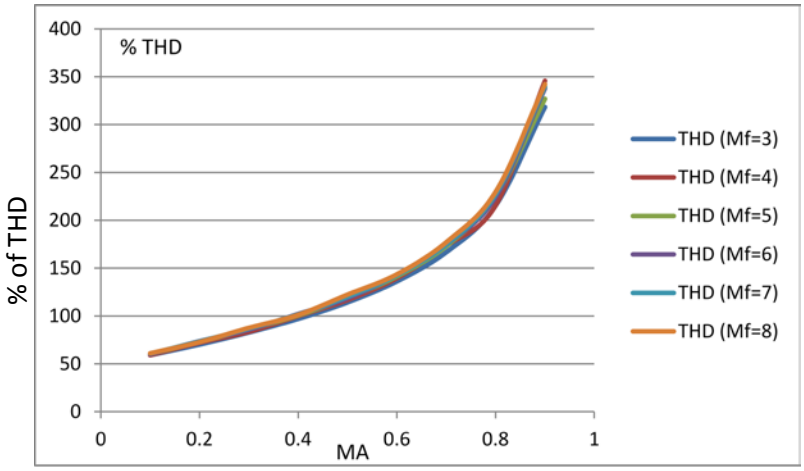


Fig. 4.15: Simulated percentage of the Total Harmonic Distortion (THD) for modulation indices from 3 to 8.

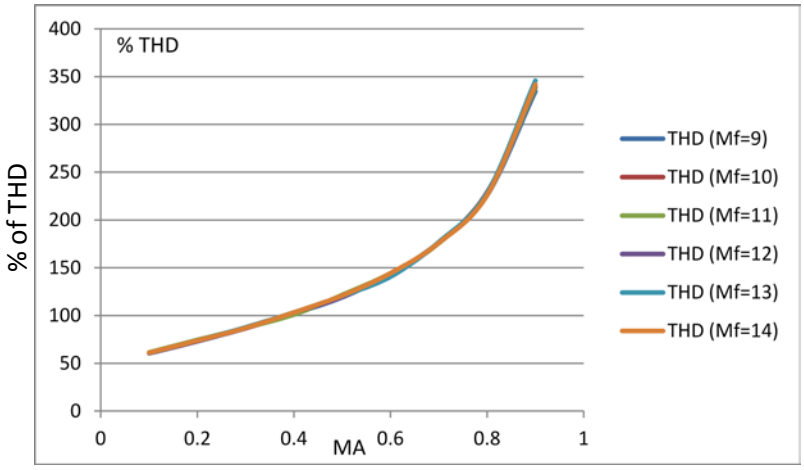
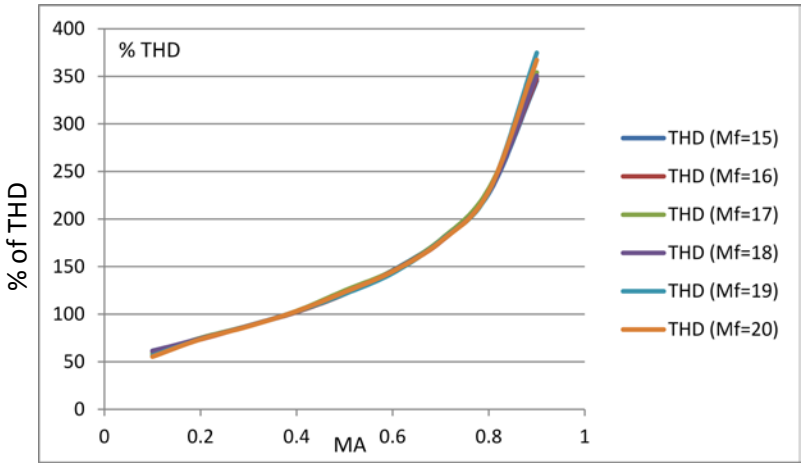


Fig. 4.16: Simulated percentage of the Total Harmonic Distortion (THD) for modulation indices from 9 to 14.

Fig. 4.17: Simulated percentage of the Total Harmonic Distortion (THD) for modulation indices from 15 to 20.



4.3.3 SPWM Applied to Inverter Circuit – Calculated Results

The SPWM is generated by comparing a sinusoidal voltage signal with a triangular waveform. The two signals are compared using OpAmp as a comparator and the output of the OpAmp is applied to the MOSFET driver circuits. By controlling the AC amplitude the width of the pulses are controlled and hence the level of the output voltage is also controlled (each pulse will have different width within the quarter of the cycle). The frequency of the triangular (or carrier) waveform (f_c) controls the switching frequency. Although it has no impact on the output voltage but is has an important effect on the Total Harmonic Distortion (THD). Fig. 4.18 illustrates how the control pulses in SPWM are generated. The ratio of the amplitude of the sinusoidal waveform (A_s) to the peak value of the triangular (or carrier) waveform (A_c) is referred to as the amplitude modulation of the switch 'M_A'. The output voltage for each individual harmonic can be expressed as:

$$\% \frac{rms(n)}{V_{dc}} = 100 \times \left(\frac{4}{n\pi\sqrt{2}} \sum_{i=1}^{M_f} (-1)^{i+1} \cos n\alpha_i \right) \qquad [4.11]$$

The percentage of total rms of the output voltage can be expressed as:

$$\%\frac{rms}{V_{dc}} = 100 \times \sqrt{\left[\frac{2}{\pi}\sum_{p=1}^{\frac{M_f}{2}}(\alpha_{2p}-\alpha_{2p-1})\right]} \qquad if\ M_f\ is\ even \qquad [4.12]$$

$$\%\frac{rms}{V_{dc}} = 100 \times \sqrt{\left[\frac{2}{\pi}\left(\sum_{p=1}^{\frac{M_f-1}{2}}(\alpha_{2p}-\alpha_{2p-1})+\frac{\pi}{2}-\alpha_{M_f}\right)\right]} \qquad if\ M_f\ is\ odd \qquad [4.13]$$

$$Total\ Harmonic\ Distortion\ (T.H.D) = \frac{V_h}{V_1} \qquad [4.15]$$

$$V_h = \sqrt{\left[\sum_{n=2,3,\ldots}^{\infty} V_n^2\right]} \quad or \quad V_h = \sqrt{V_{out}^2 - V_1^2} \qquad [4.16]$$

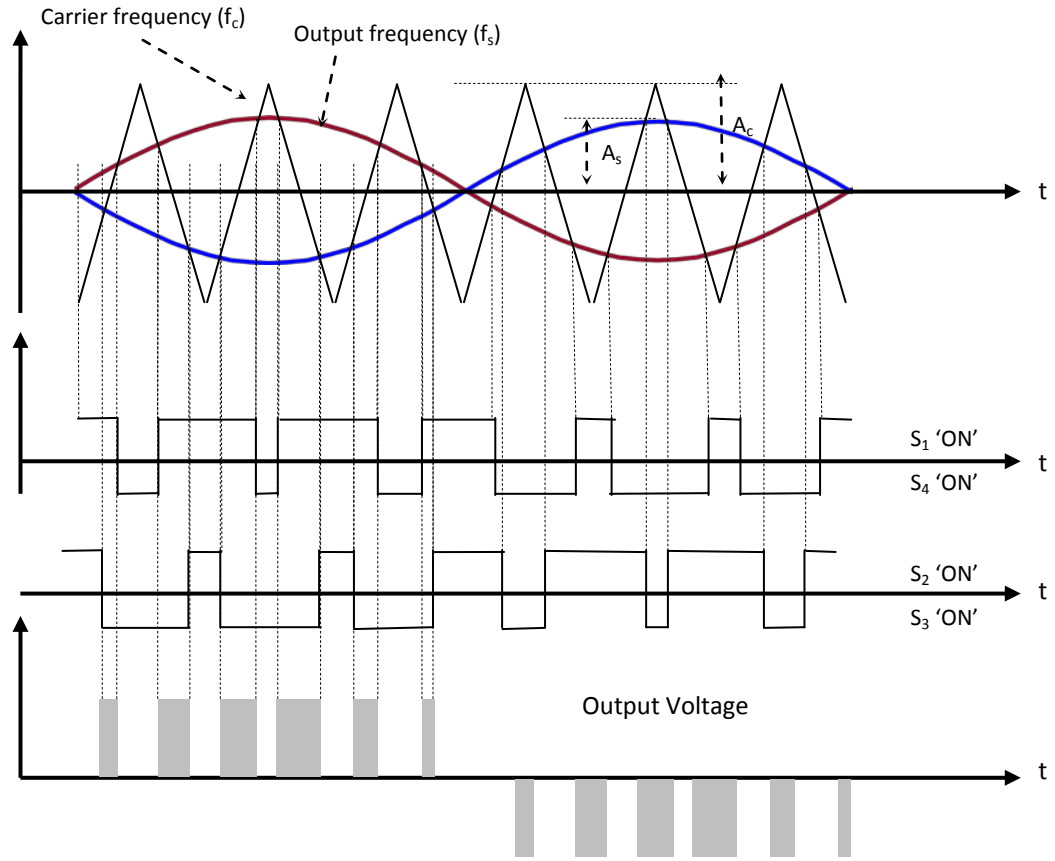


Fig. 4.18: Generation of the control pulses in SPWM Inverter

Equations 4.12 and 4.13 are used to plot the total rms for the inverter circuit. The graphs are shown in Figs. 4.19 – 4.22. For Mf 1, the waveform is different because the pulse is just a single pulse and there are no gaps between individual pulses.

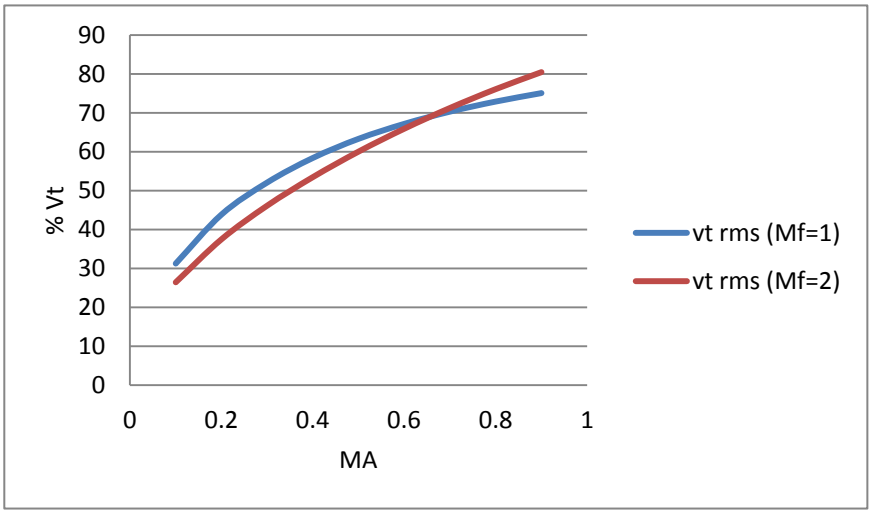


Fig. 4.19: Calculated total rms of the output voltage in SPWM for modulation indices from 1 to 2.

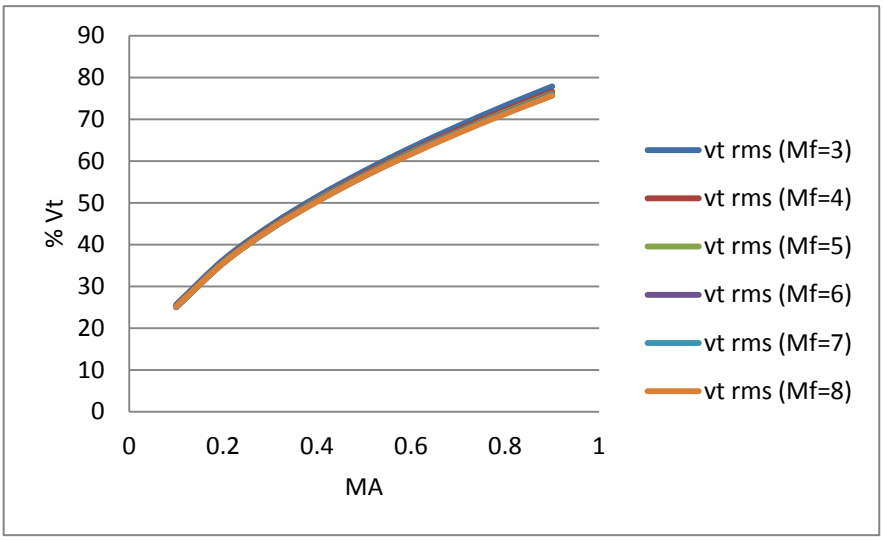


Fig. 4.20: Calculated total rms of the output voltage in SPWM for modulation indices from 3 to 8.

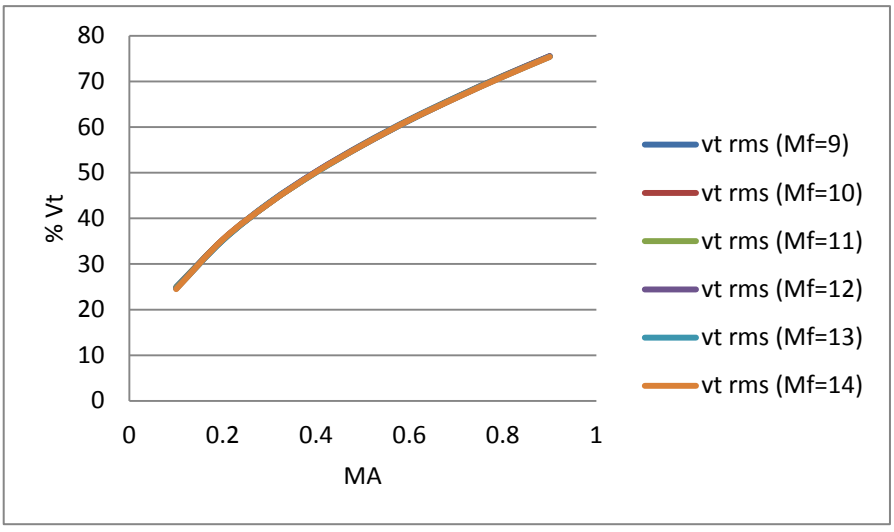


Fig. 4.21: Calculated total rms of the output voltage in SPWM for modulation indices from 9 to 14.

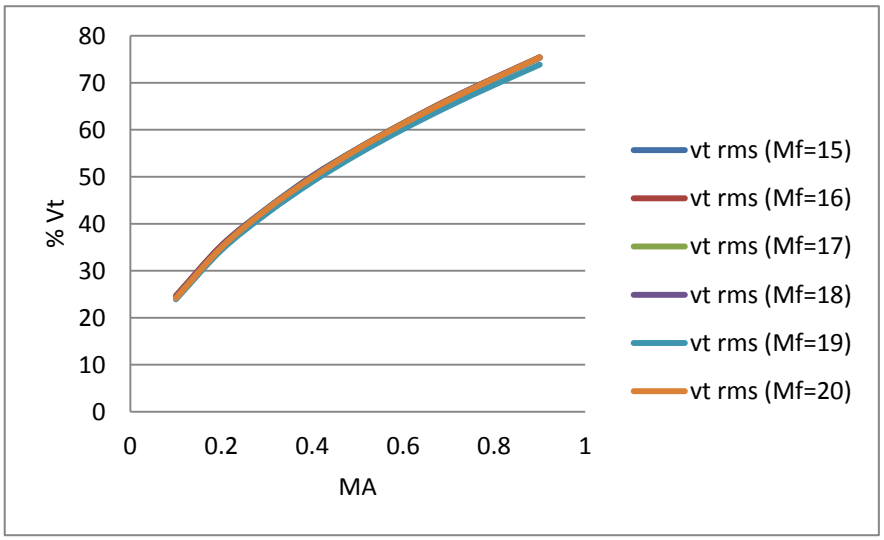


Fig. 4.22: Calculated total rms of the output voltage in SPWM for modulation indices from 15 to 20.

The rms of the fundamental component in the SPWM inverter is also plotted using equation 4.11. The values of 'α_i' in equation 4.11 are the start and end of each individual pulse. For example if there are 6 pulses in each half cycle (as shown in Fig. 4.18) there will be 12 values of 'α': α_1, α_2, α_3, . . . , α_{12}. Figs 4.23 – 4.26 illustrate V_1 rms at different frequency modulations *(M_f)*.

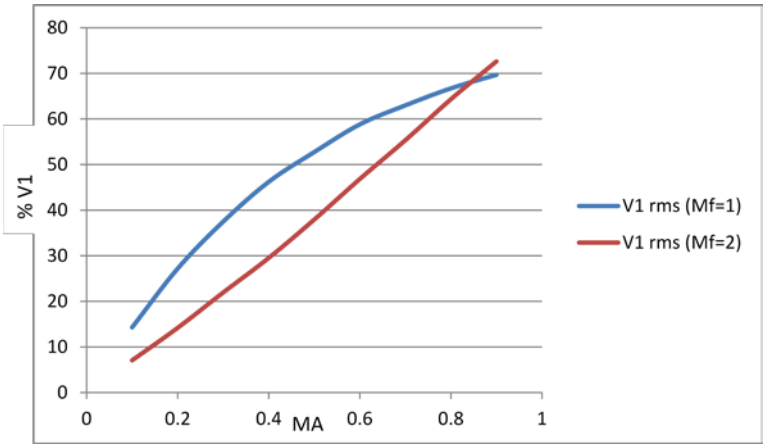


Fig. 4.23: Calculated RMS of the fundamental component of the output voltage in SPWM for modulation indices from 1 to 2.

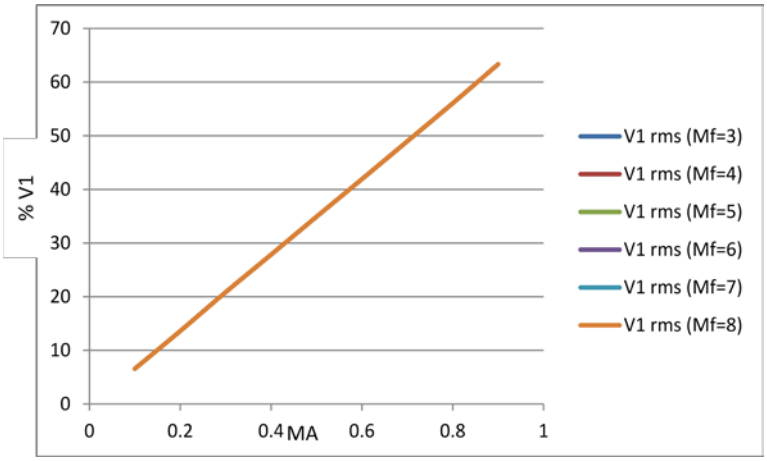


Fig. 4.24: Calculated RMS of the fundamental component of the output voltage in SPWM for modulation indices from 3 to 8.

Fig. 4.25: Calculated RMS of the fundamental component of the output voltage in SPWM for modulation indices from 9 to 14.

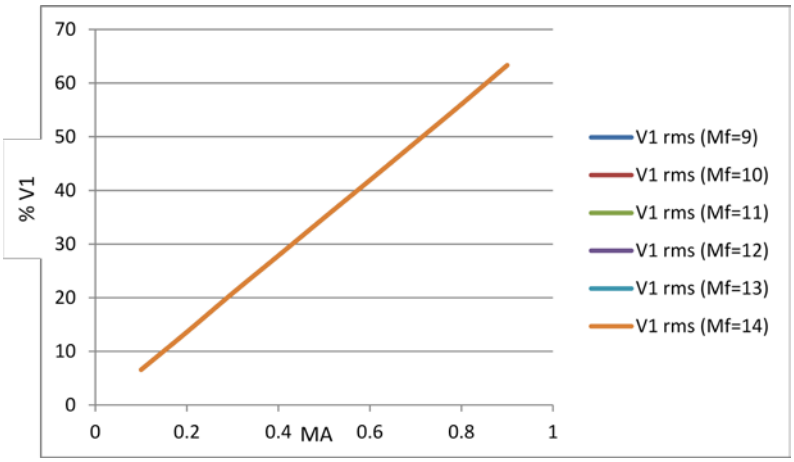
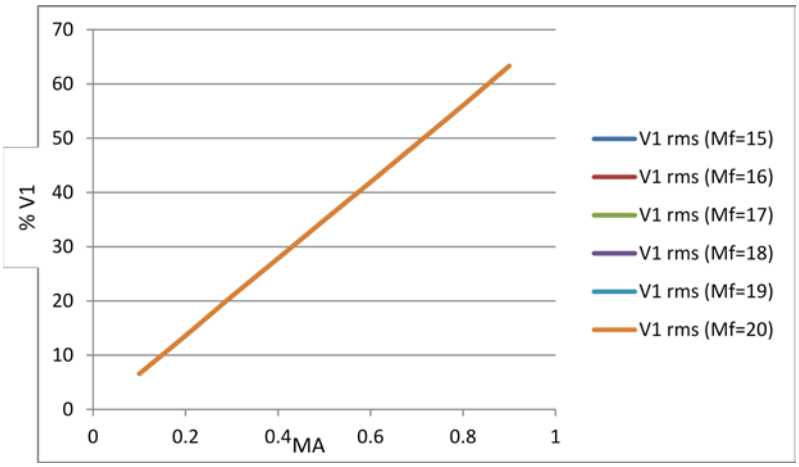


Fig. 4.26: Calculated RMS of the fundamental component of the output voltage in SPWM for modulation indices from 15 to 20.



Equations 4.15 and 4.16 are used to plot the THD of the inverter circuit. The waveforms of the THD are shown in Figs. 4.27 – 4.30 for different frequency modulations *(M_f)*. The THD for $M_f = 1$ is different from other THD curves because this is a single pulse and there is no variation between pulse widths. The reason that the THD for the other curves are similar is because the power within the harmonics can be shifted along the frequency spectra but it does not go away. Although the THD is similar for different values of M_f , the low order harmonics can be suppressed and the high order harmonics can be easily filtered with a small size filter components (in particularly filter inductor).

Fig. 4.27: Calculated THD of the output voltage in SPWM for modulation indices from 1 to 2.

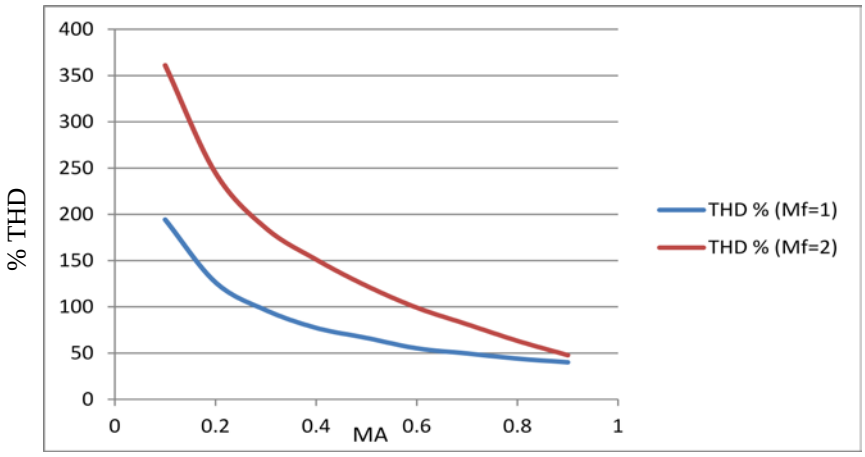


Fig. 4.28: Calculated THD of the output voltage in SPWM for modulation indices from 3 to 8.

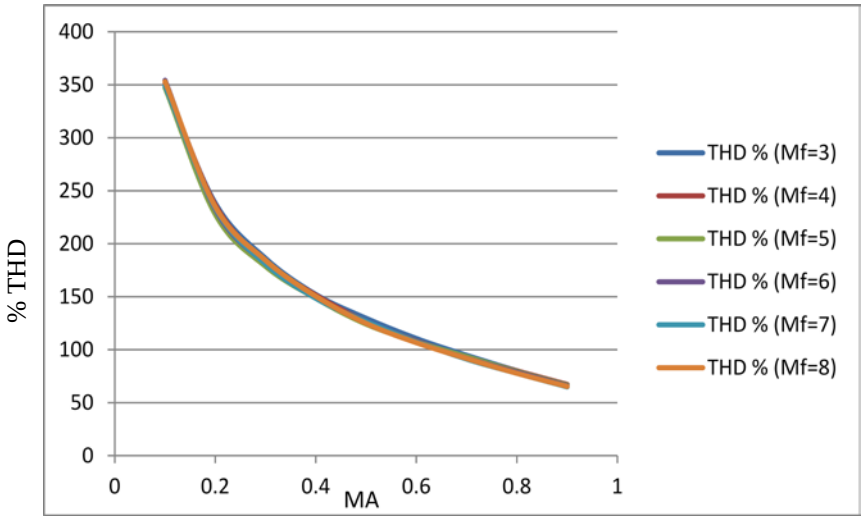


Fig. 4.29: Calculated THD of the output voltage in SPWM for modulation indices from 9 to 14.

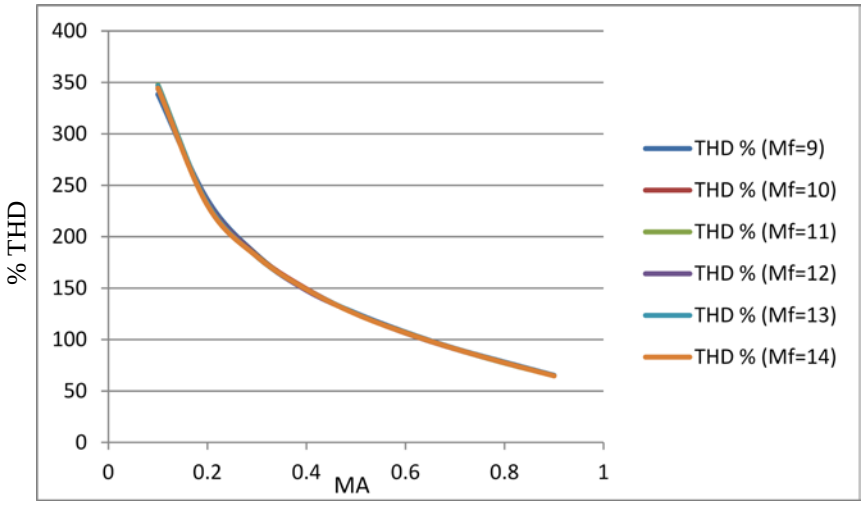
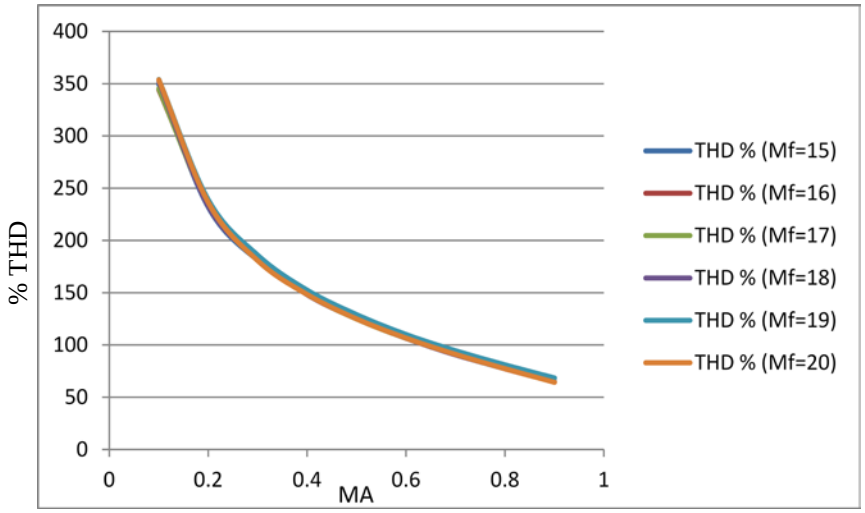


Fig. 4.30: Calculated THD of the output voltage in SPWM for modulation indices from 15 to 20.



4.3.3 SPWM Applied to Inverter Circuit – Simulated Results

The Full bridge SPWM inverter is simulated on PSPICE using MOSFET switches IRF740 and the control pulses were generated using sine and triangular signals applied to LM741 OpAmp as a comparator. The circuit diagram is shown in Fig. 4.31 and the waveforms of the control pulses and the output voltage waveform is shown in Fig. 4.32. The simulated results of the THD, fundamental output voltage and the total output voltages at different frequency modulations are identical to the calculated one and for just comparison purpose the calculated graphs in Fig. 4.3 are reproduced using PSPICE and is shown in Fig. 4.33.

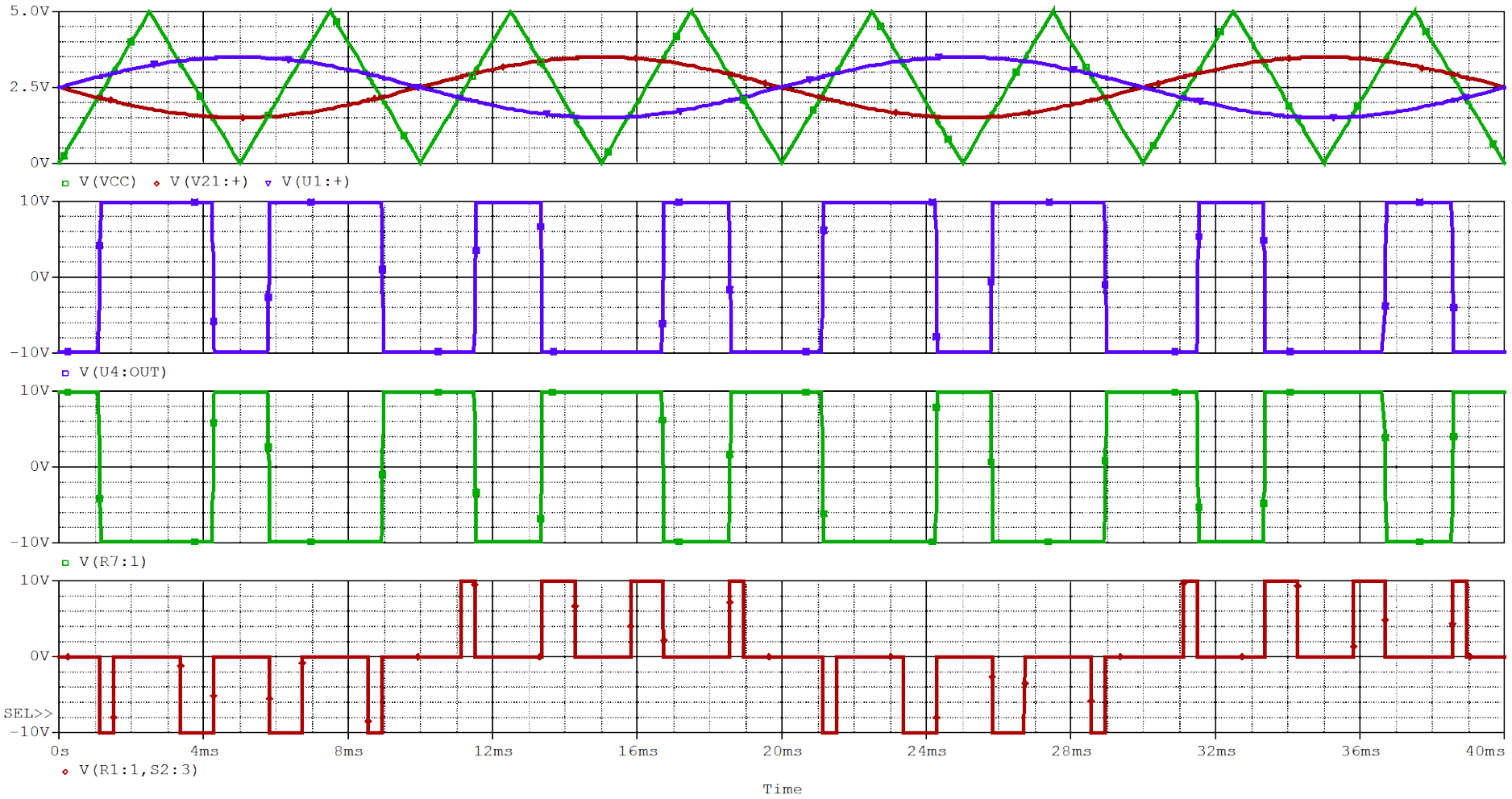


Fig. 4.31: PSPICE simulation of the full bridge inverter using SPWM

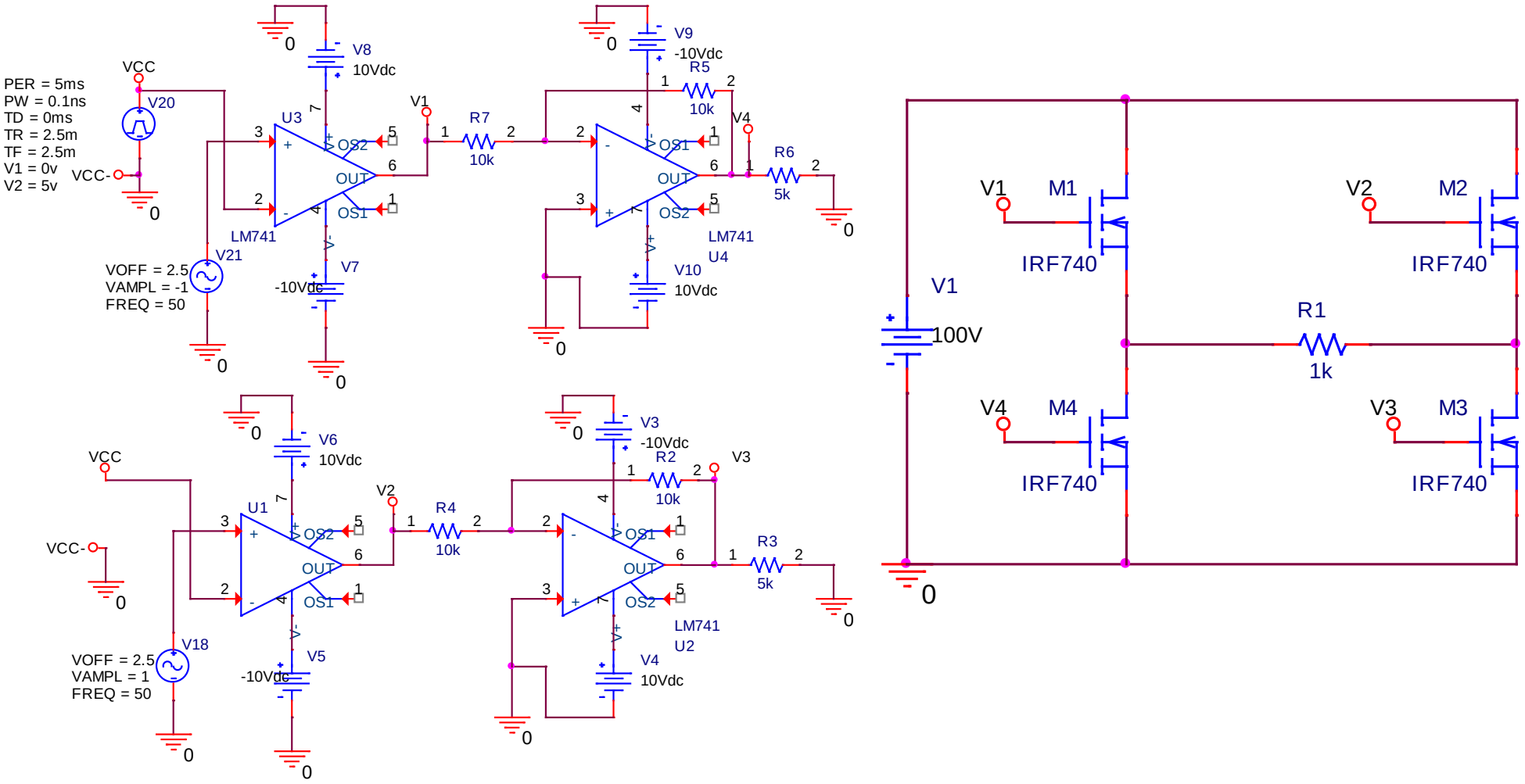
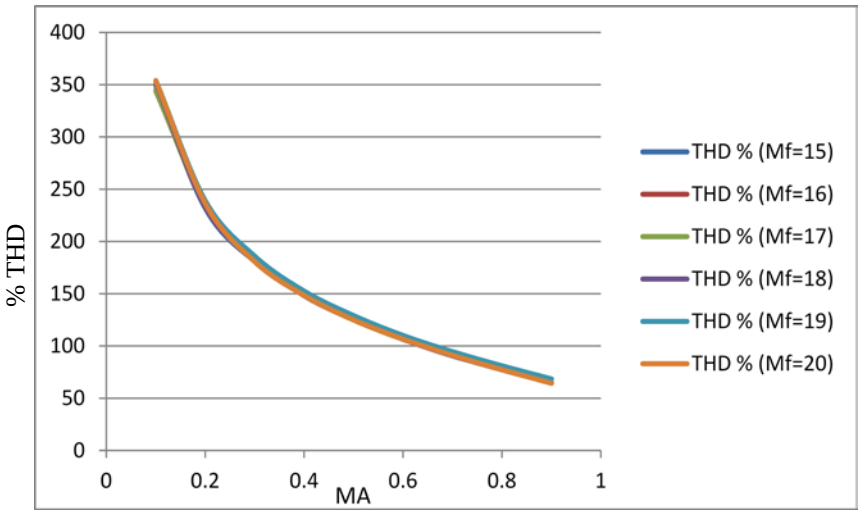


Fig. 4.32: PSPICE simulation of the full bridge inverter using SPWM

Fig. 4.33: Simulated THD of the output voltage in SPWM for modulation indices from 15 to 20.



4.3.4 HF SPWM with 50Hz Integrated Component

The input frequency of the UPS system is 50 Hz and most of the loads operate at 50 Hz (in UK). The transformer in both proposed configurations operate at high frequency (10 – 20 kHz). Therefore it is required to 'hide' the 50 Hz component within the high frequency while it is transformed by the HF transformer and then reconstruct the 50 Hz again. This is achieved with the configuration shown in Fig. 4.34. The control pulses are generated using EXCLUSIVE OR so that the voltage across the load will only be developed when the diagonal switches are controlled at the same time. The output of the inverter will be at high frequency with two 50Hz component opposite to each others included in the high frequency (3rd graph in Fig. 4.35). Then a cycloconverter is used to flip the negative 50 Hz so that the final output consists of a fundamental 50 Hz (Fig. 4.36). The output of the inverter is also simulated for 1 kHz, 5 kHz and 10 kHz as shown in Figs. 4.37 to 4.42.. Notice the absence of the 50Hz from the transformer spectrum.

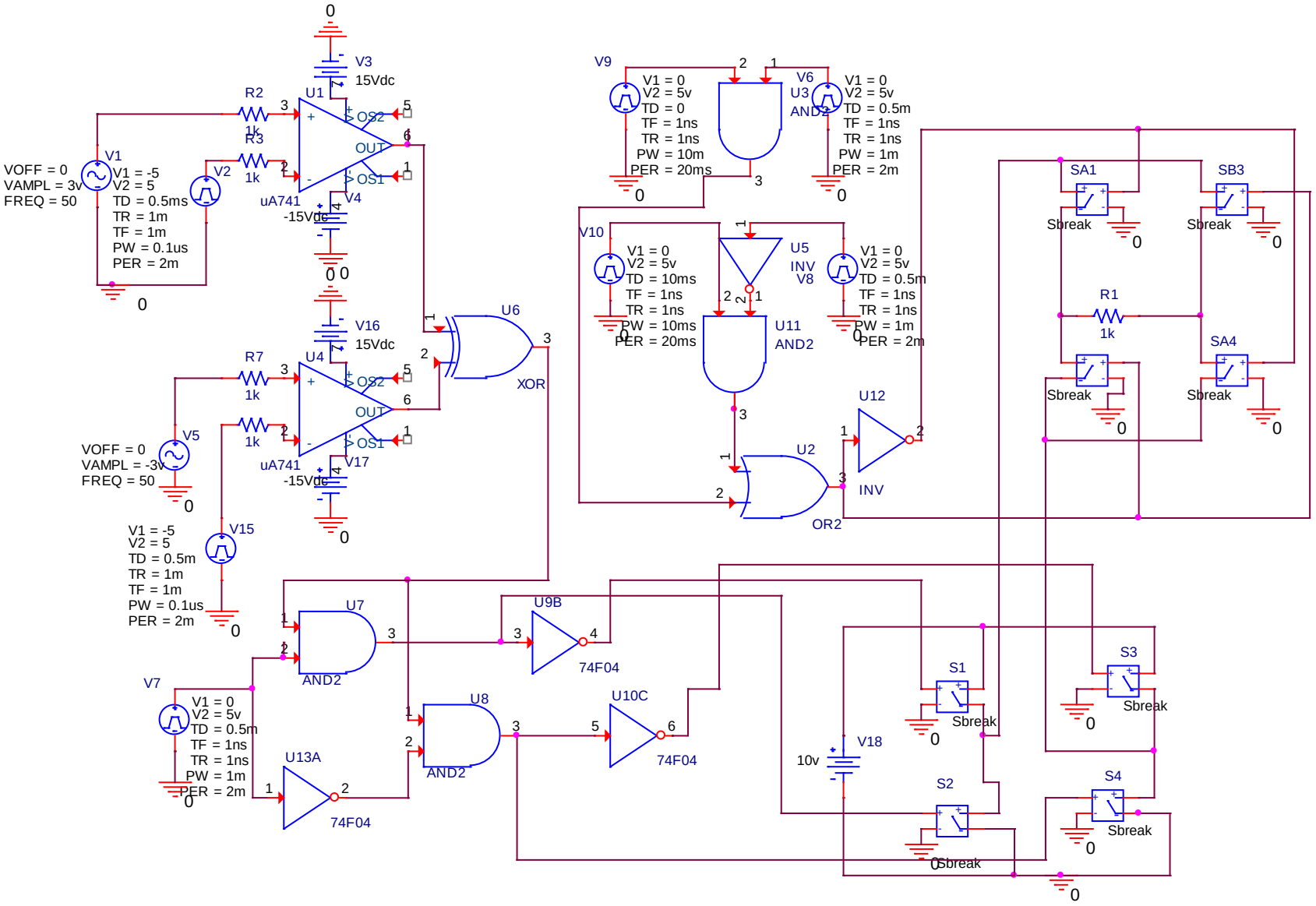


Fig. 4.34: Simulated circuit diagram of the inverter and cycloconverter with the control circuit

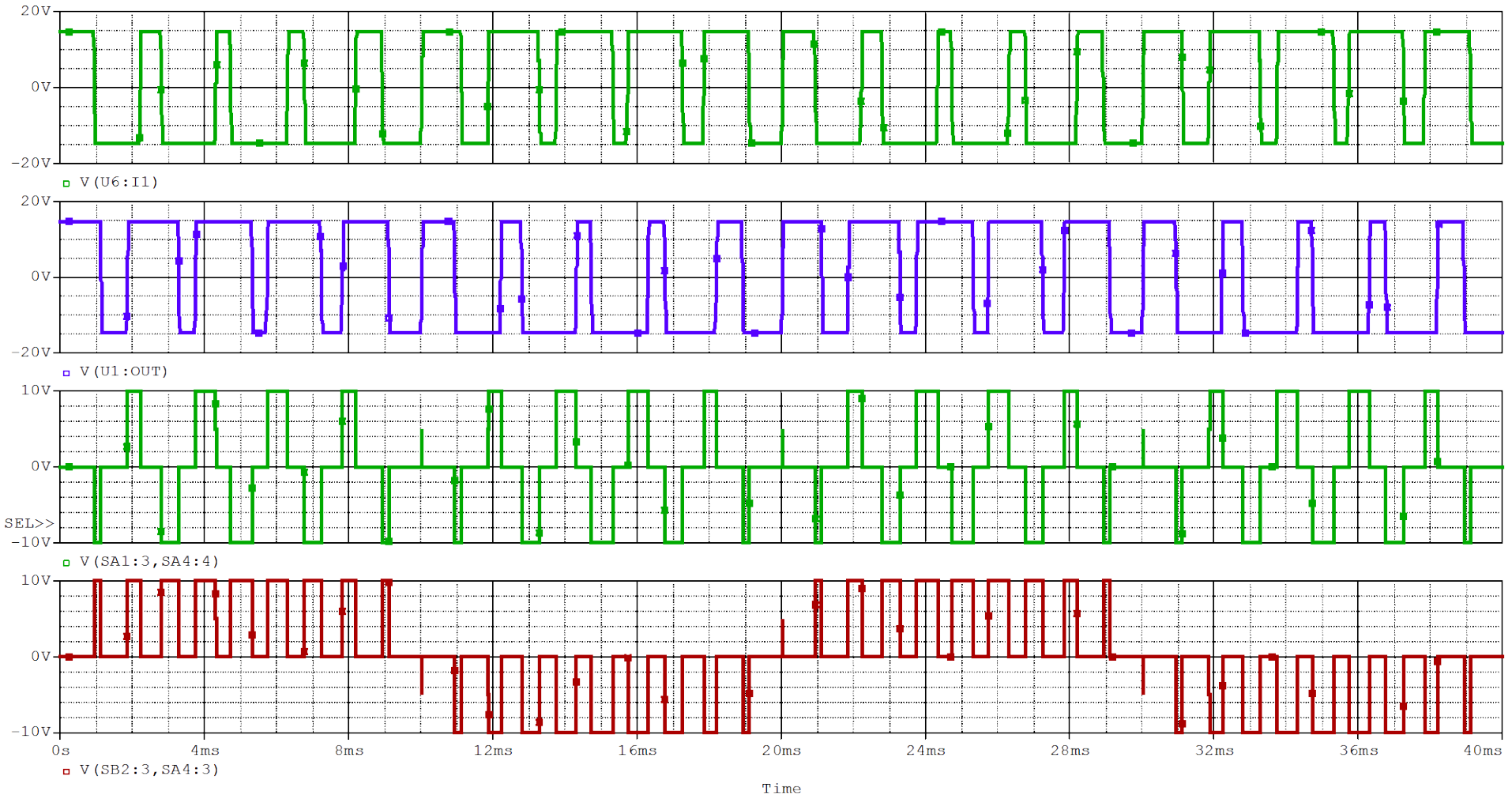


Fig. 4.35: Control pulses (top two graphs), the transformer voltage and the output voltage of the HF UPS system

Transformer frequency = 500Hz. Output frequency (50Hz)

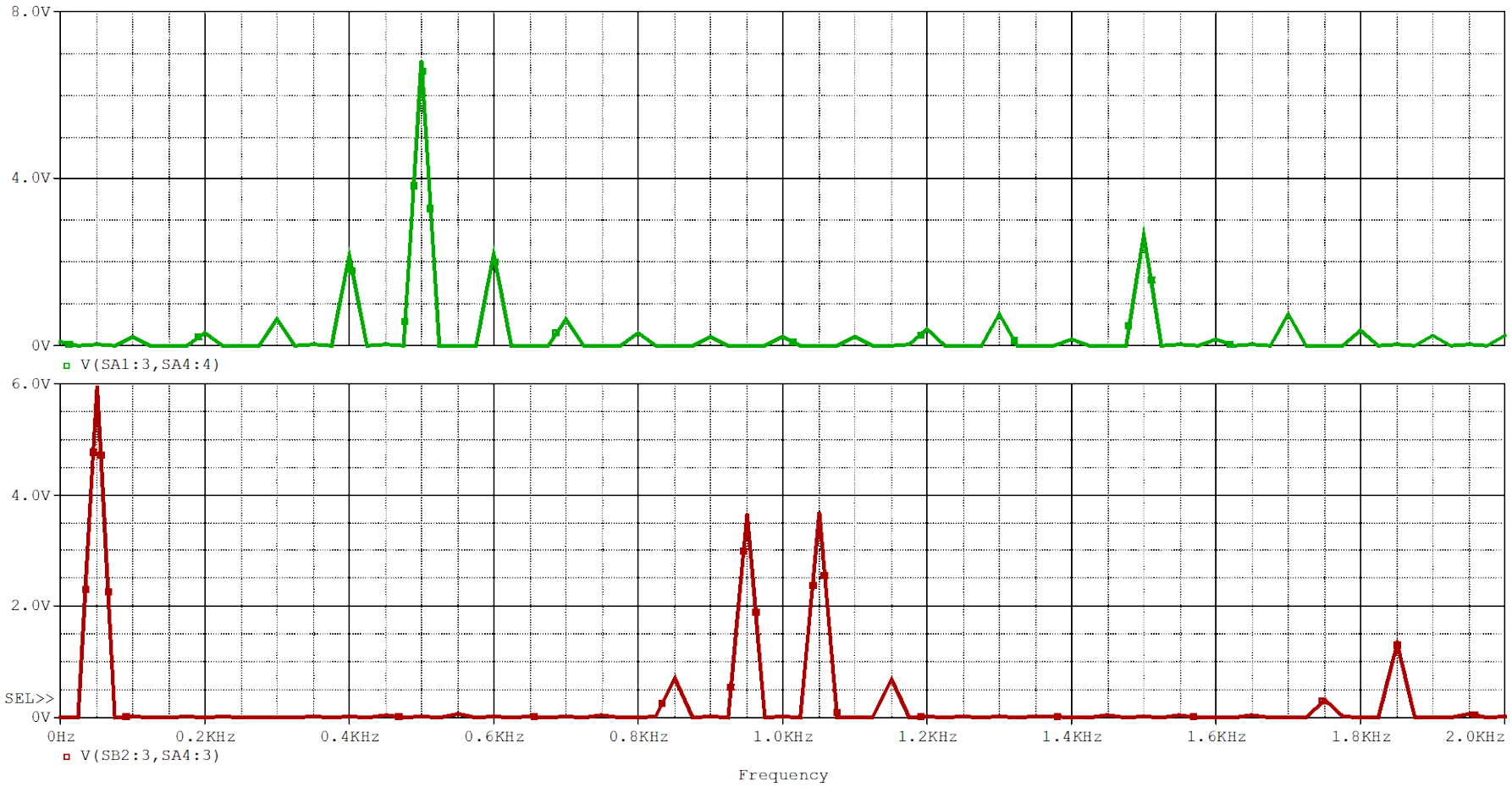


Fig. 4.36: Frequency spectra of the transformer (500Hz) and the output voltages (50Hz)

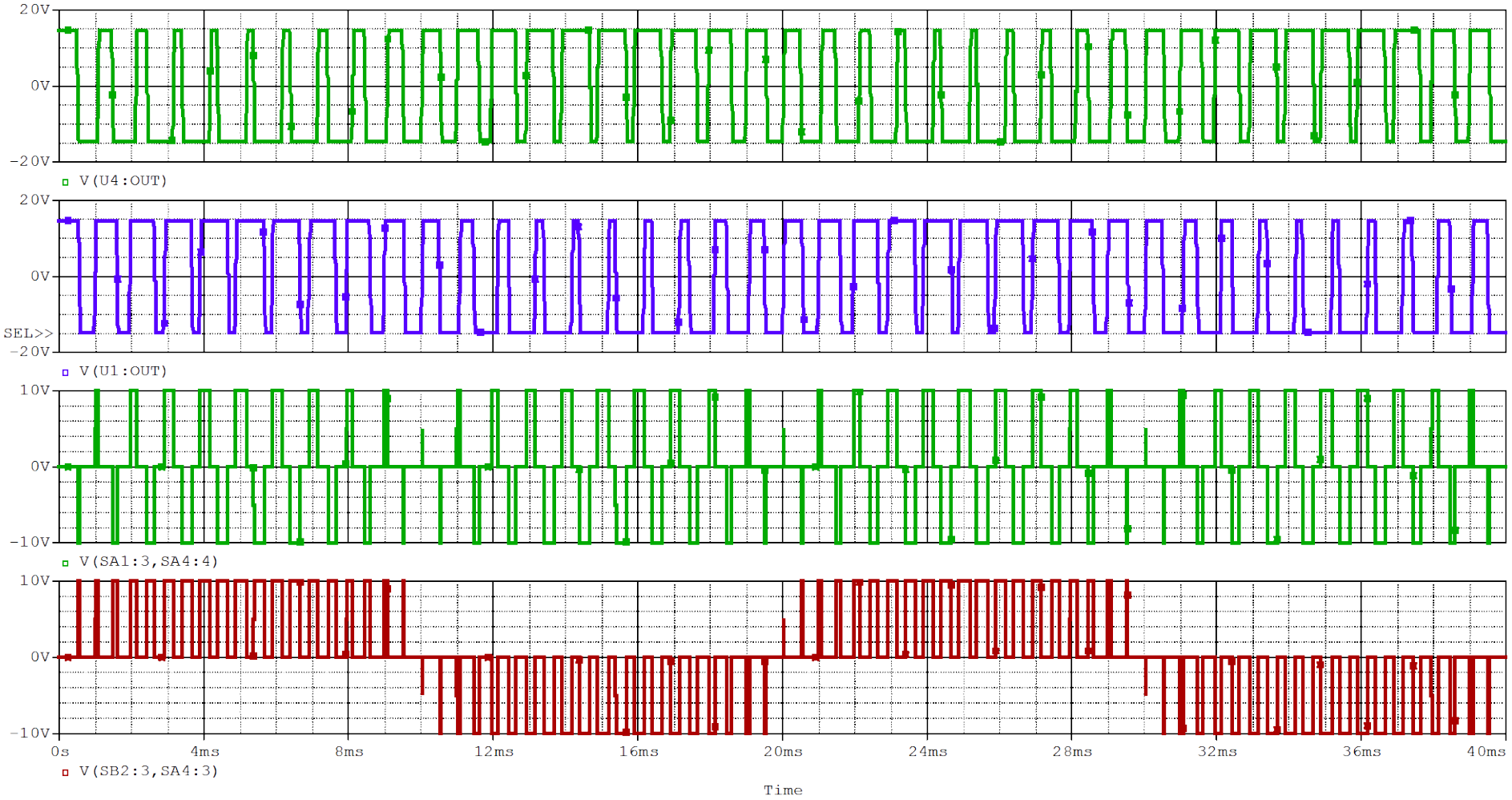


Fig. 4.37: Control pulses (top two graphs), the transformer voltage and the output voltage of the HF UPS system

Transformer frequency = 1kHz. Output frequency (50Hz)

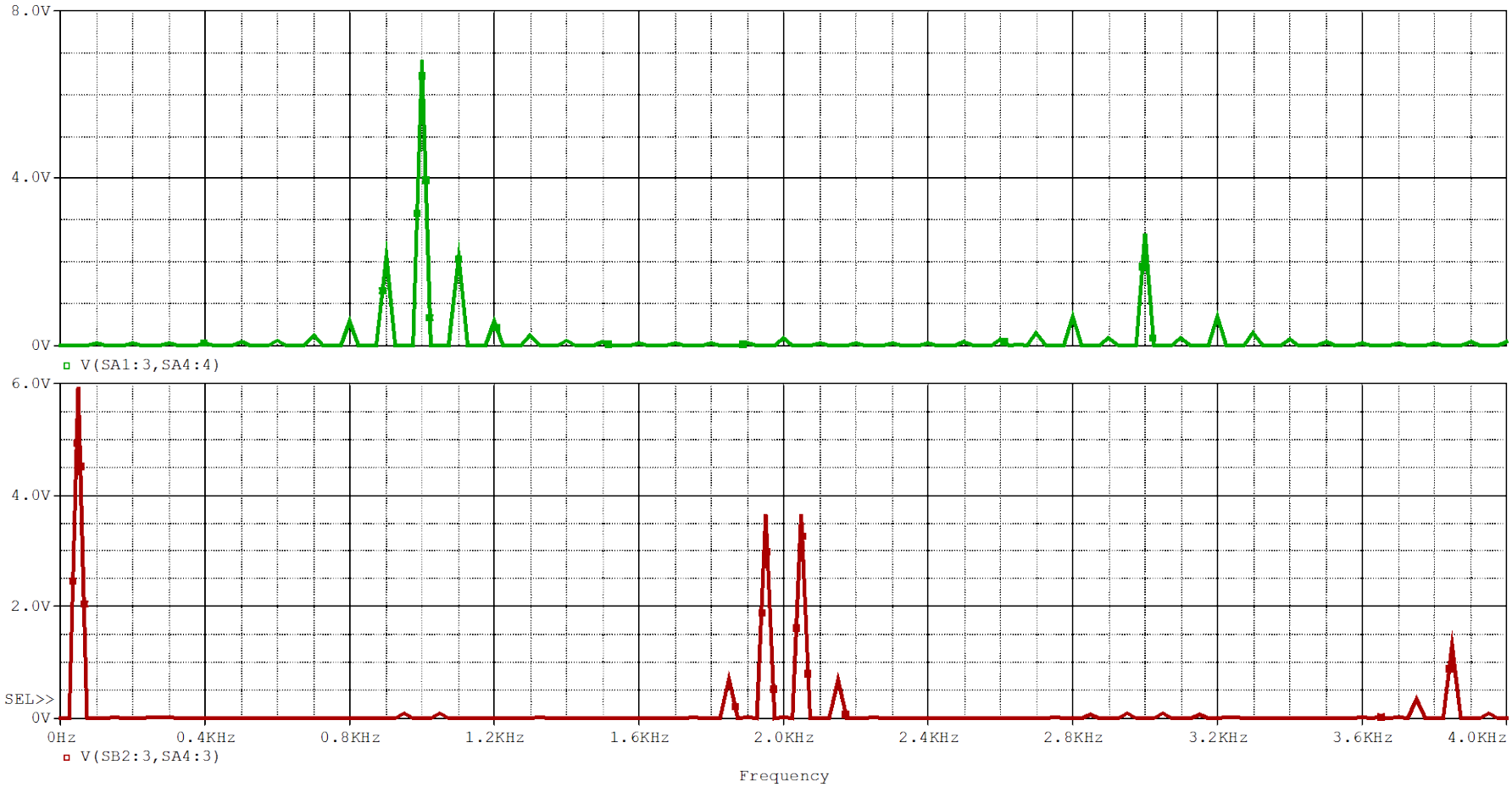


Fig. 4.38: Frequency spectra of the transformer (1kHz) and the output voltages (50Hz)

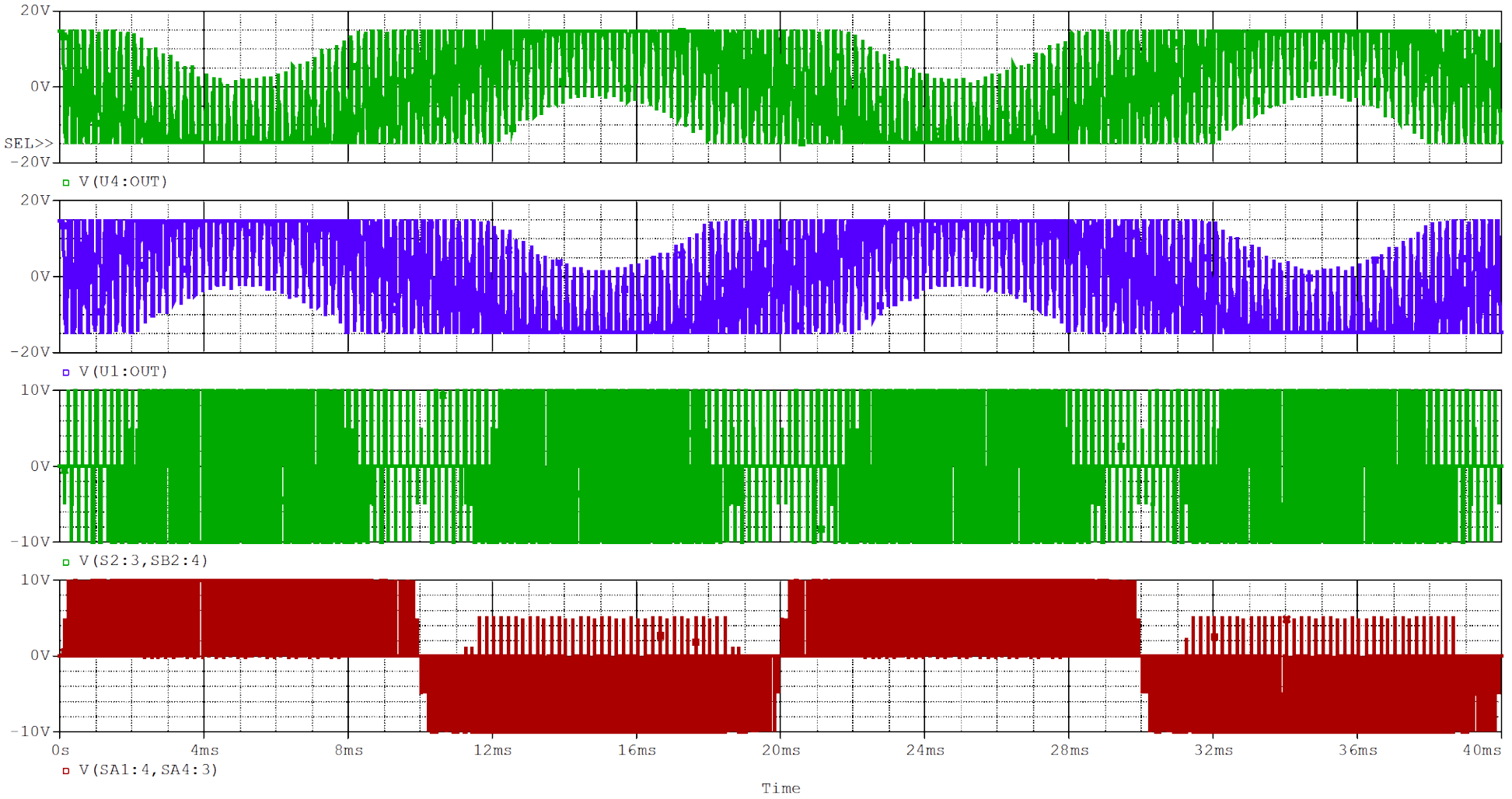


Fig. 4.39: Control pulses (top two graphs), the transformer voltage and the output voltage of the HF UPS system

Transformer frequency = 5kHz. Output frequency (50Hz)

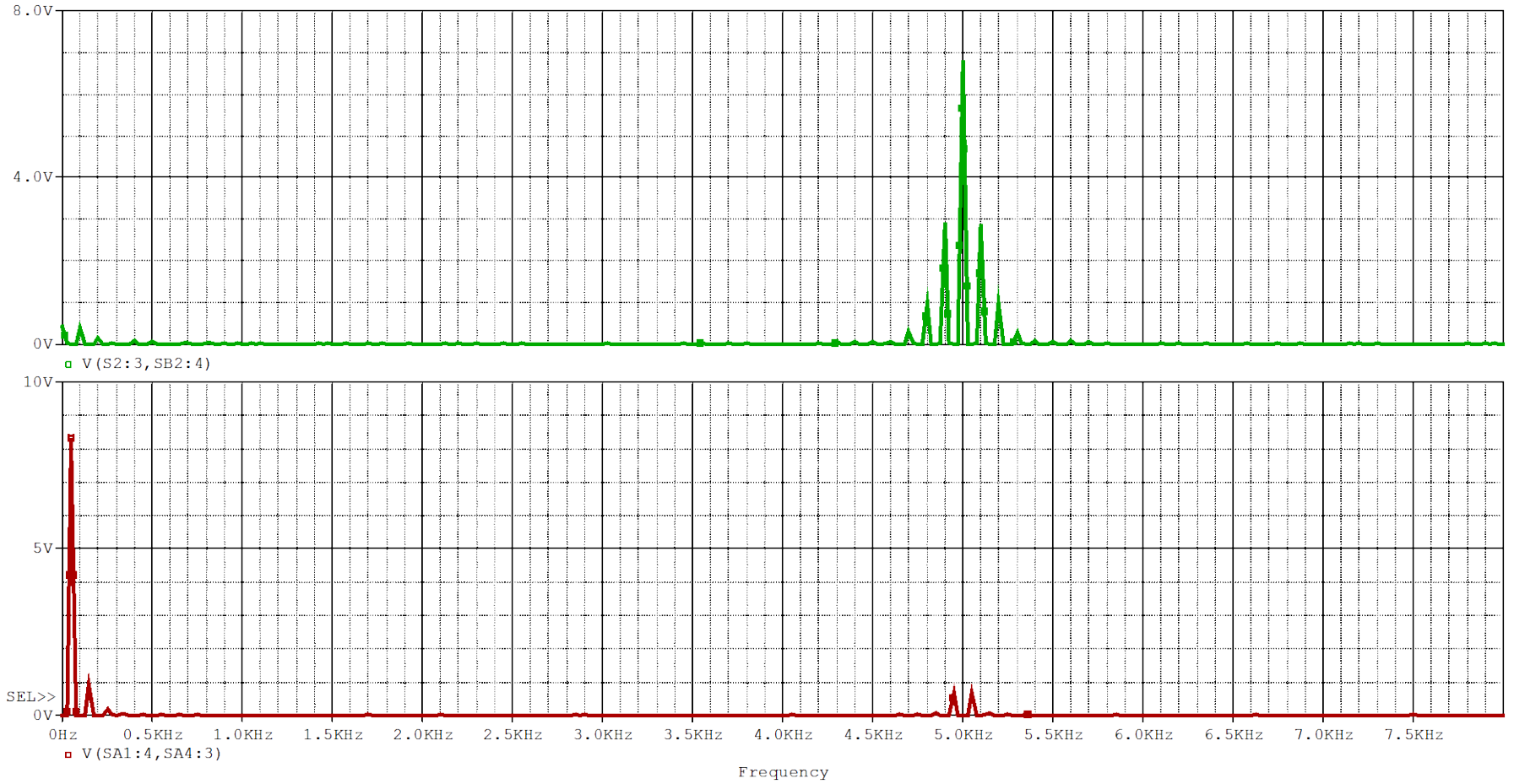


Fig. 4.40: Frequency spectra of the transformer (5kHz) and the output voltages (50Hz)

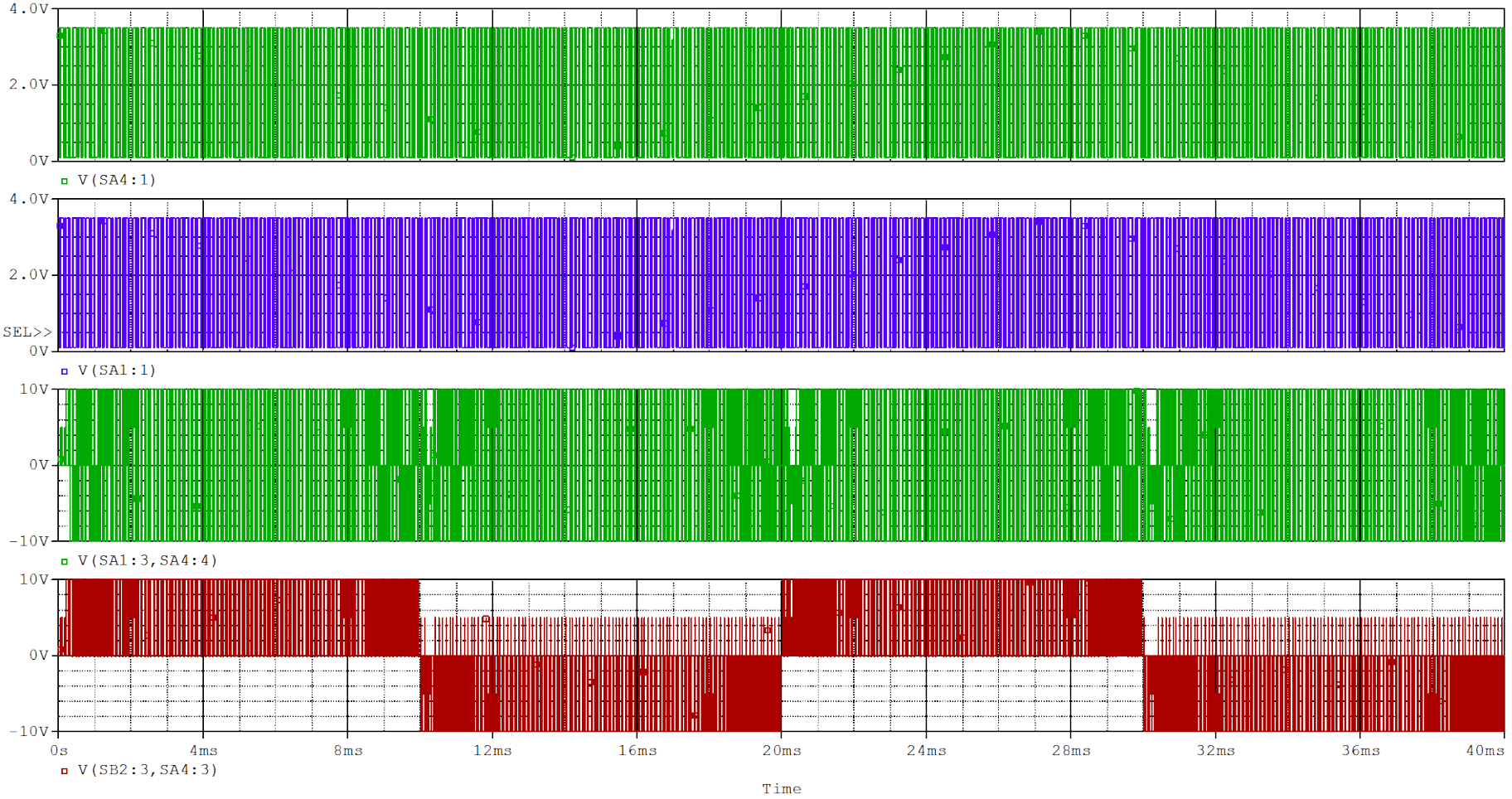


Fig. 4.41: Control pulses (top two graphs), the transformer voltage and the output voltage of the HF UPS system

Transformer frequency = 10 kHz. Output frequency (50Hz)

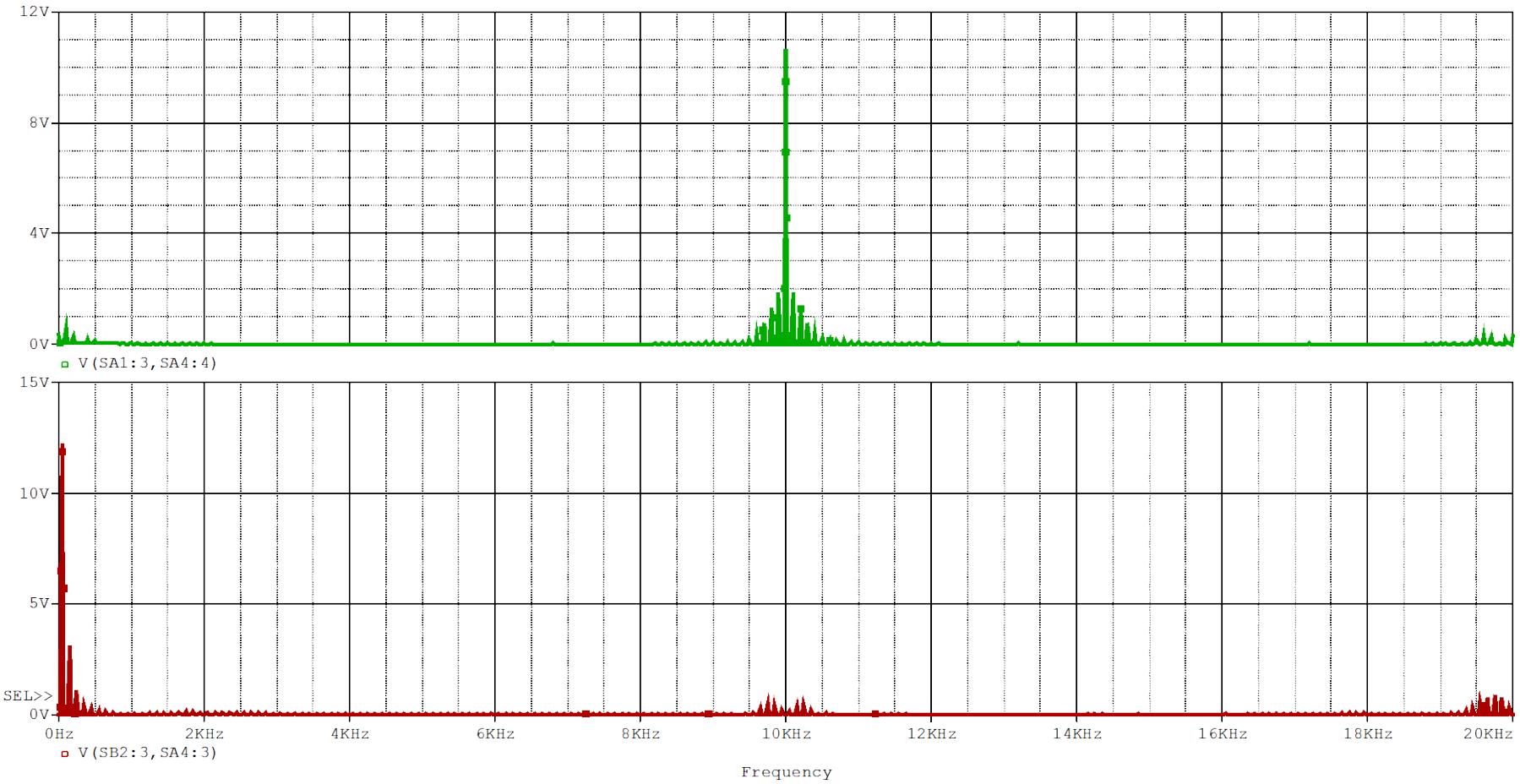


Fig. 4.42: Frequency spectra of the transformer (10kHz) and the output voltages (50Hz)

4.3.5 Summary

In this chapter two configurations of the HF inverters were introduced. The transformer operates at high frequency in both configurations. The difference between them is mainly within the rectification and the DC link. The total, fundamental and THD are evaluated for the HF inverter at different frequency modulations and it did show that the frequency modulation has no impact on the THD, however it has an impact on individual harmonics. So at high frequency modulation the filtering of the low order harmonics becomes easier. A circuit to integrate the 50Hz component within the high frequency is also simulated in this chapter. The simulation results showed that a 50 Hz component can pass through the transformer without the transformer realising it; which means that the transformer can be designed for the higher frequency and hence it will be smaller in size than a similar power 50 Hz transformer. The practical results of the proposed system are introduced in the next chapter.

CHAPTER 5: PRACTICAL IMPLEMENTATION OF THE PROPOSED H.F. UPS

5.1 Introduction

In the previous chapter the HF UPS system was simulated on PSPICE. This chapter contains the practical implementation of the system. The implementation of a microcontroller, driver circuits and the power circuits (inverter & cycloconverter) are all discussed in this chapter.

5.2 Microcontroller (Chipkit-uno32-development-board)

The UPS system could be controlled using hardware or software. In the simulation results the hardware approach was used and this is mainly due to the unavailability of the microcontroller in PSPICE. However it was educationally very useful to use the hardware approach in the simulation. As far as the results of the power circuits (inverter / cycloconverter) are concerned, it will not affect the output voltage waveform if either the hardware or software approach is used. In the practical implementation of the HF UPS system the software approach using a microcontroller Chipkit [29] is used. The reason for using this microcontroller is because of the ease of use, the low price and the compact design. The Chipkit has 23 outputs which is more than enough for UPS application. Fig. 5.1 shows the layout of the Chipkit microcontroller. A programme is written to generate the required pulses; it is then downloaded to the Chipkit memory through USB connection. The Chipkit (Uno32) development board is a clone of the Arduino Uno board. It has 128 KB Flash program memory and 16 KB RAM. The Chipkit has an 80MHz frequency and it has 32-bit processor. With reference to Fig. 5.1 the pins are determined as follow:

1) USB Connector: This is the connection to the PC. The board is also powered from this connection. as well as the power connection.
2) This connection is used for the Debugging.

3) DC power supply connection to the board (7V – 15V).

4) Regulated voltage (3.3V).

5) JP1 – Power Select Jumper.

6) Regulated voltage (5V).

7) Power Connector

8) PIC32 Microcontroller

9) Analog Signal Connectors

10) Digital Signal and Power Connectors

11) User LED

12) Master/Slave Select Jumpers.

13) SPI Signal Connector

14) Digital Signal Connectors

15) Communications Status LEDs

16) Reset Button

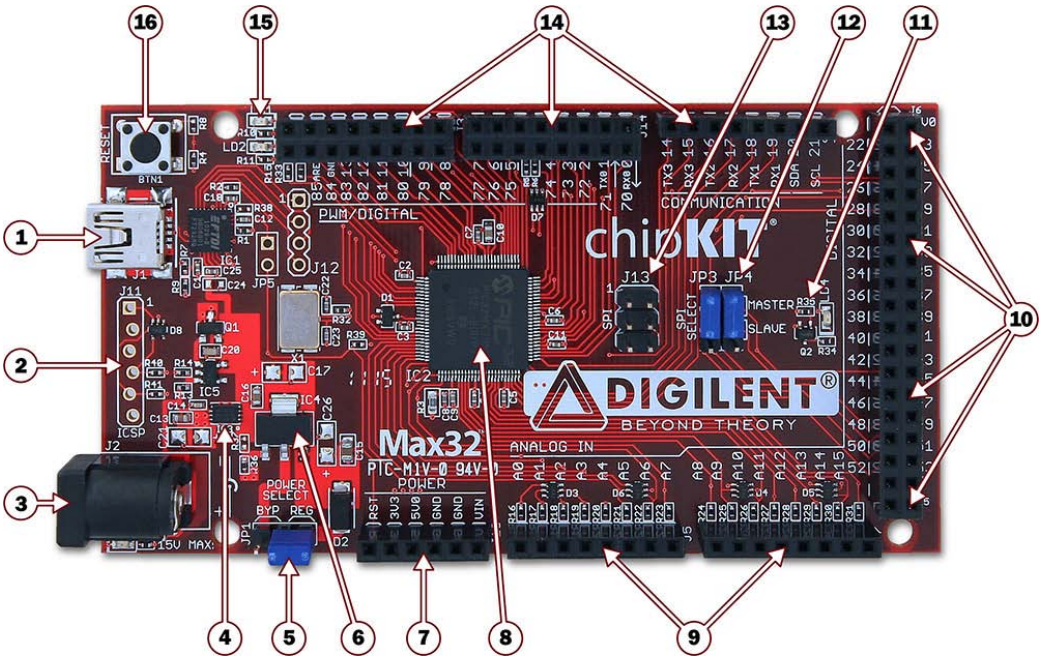


Fig. 5.1: Chipkit-uno32-development-board [29]

(http://cpc.farnell.com/digilent/chipkit-uno32/chipkit-uno32-development-board/dp/SC09963

The programme listing for generating the PWM pulses is given in Appendix B . The programme is simply made from several segments and each one is a set for a particular delay times.

One pattern from the microcontroller generated at 1 kHz is shown in Fig. 5.2.

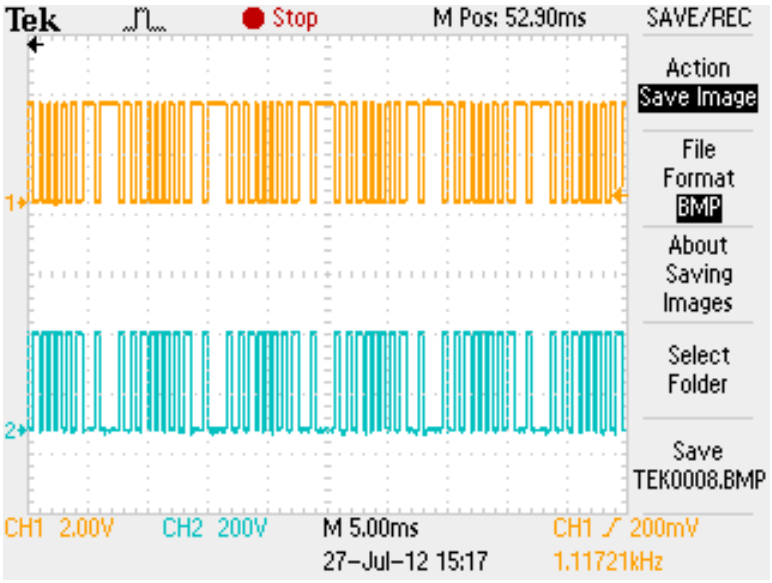


Fig. 5.2: HF-PWM pulses (1 kHz) generated from the Chipkit microcontroller

5.3 Driver and Optocouplers Circuit

In order to derive MOSFETs IRF740, driver circuits should be used. MOSFETs are voltage controlled devices, so a simple 5V pulse should be sufficient to drive them. However in inverter and cycloconverter applications the driver circuits should be isolated from each others. This is mainly because the control pulse applied to the MOSFET is connected across the gate and source. If a driver circuit (or the power supply of the driver circuit) is shared between two MOSFETS that means the two MOSFETS are short circuited through their sources. Therefore for each MOSFET switch a separate Optocouplers, a driver circuit and a power supply should be used. Fig. 5.3 shows the circuit diagram used to isolate and drive the MOSFET switches. The Optocouplers and the MOSFET drivers used are 6N137 and ICL7667 (datasheet shown in Appendix C).

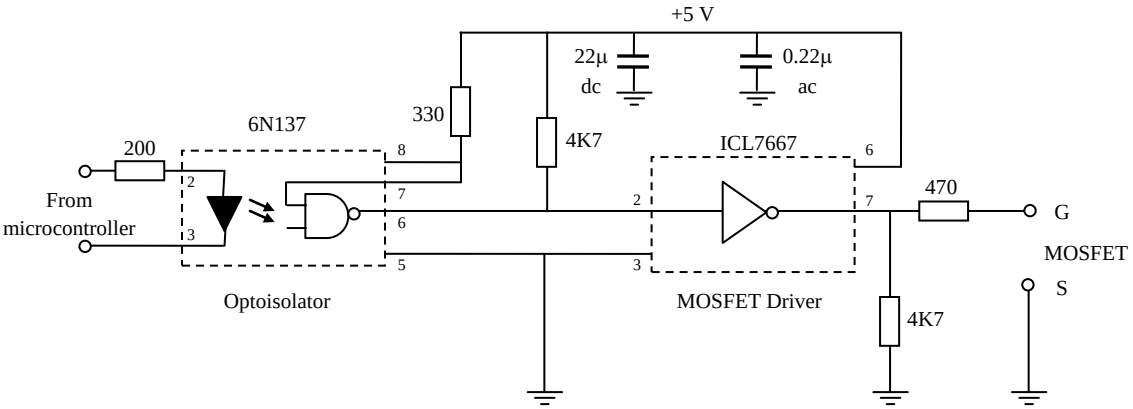


Fig. 5.3: MOSFET Optoisolator and Driver Circuit

5.4 The Practical HF UPS System

The controller is used to generate the required control pulses according to the programme written in Appendix B. These control pulses are optoisolated and are applied to the driver circuits shown in Fig. 5.3. The power circuit consists of 8 IRF740 MOSFET switches (datasheet shown in Appendix D). Four of the MOSFETs are used for the inverter and the other four are used for the cycloconverter.

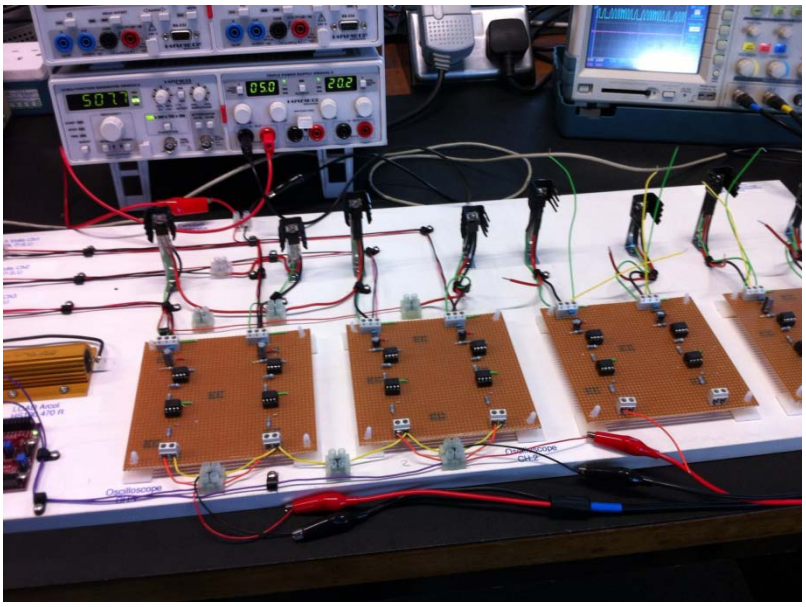


Fig. 5.4: Inverter and Cycloconverter Switches and Drivers for the HF UPS system

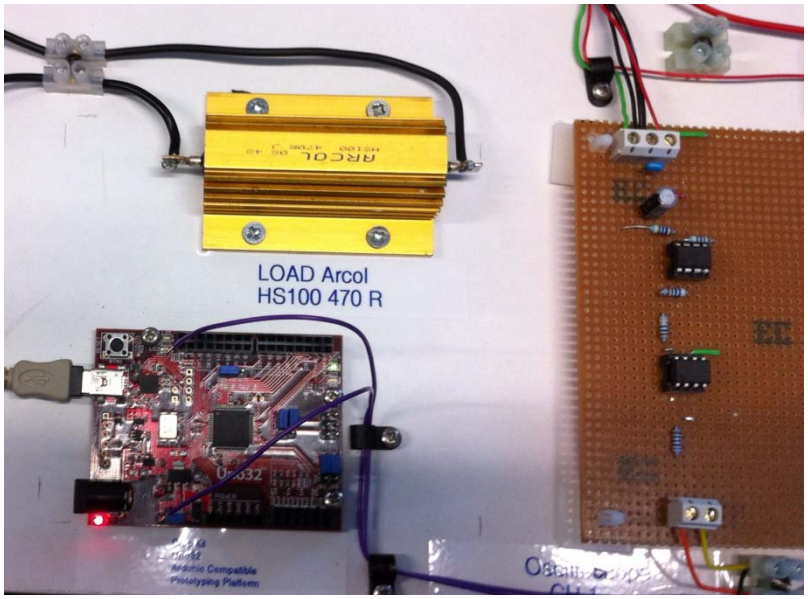


Fig. 5.5: Microcontroller and load for the HF UPS system

Figs. 5.4 and 5.5 show the hardware of the UPS system.. The eight switches shown in Fig. 5.4 and the controller & the load are shown in Fig. 5.5. Fig. 5.6 shows the control pulses generated as well as the final output voltage.

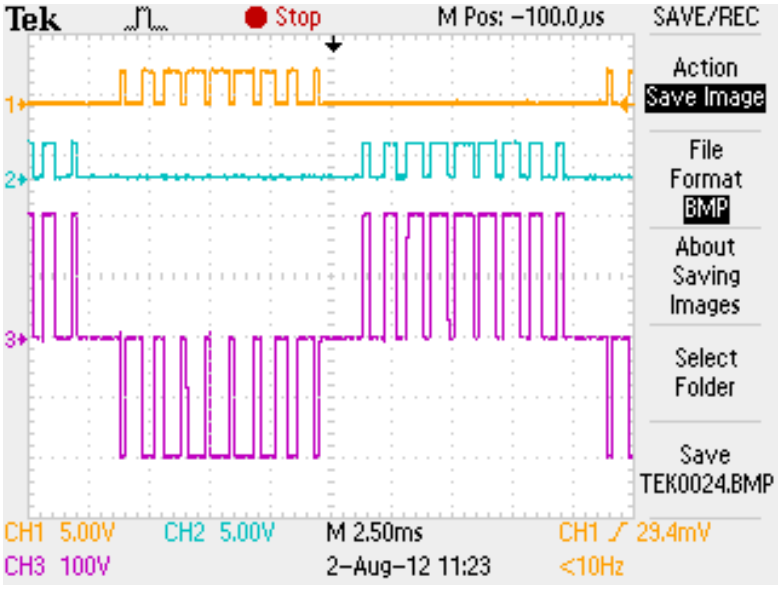


Fig. 5.6: Control pulses and the output voltage of the proposed HF UPS System

Fig. 5.7 illustrate the control pulses at different switching frequencies as well as the inverter and cycloconverter output voltages

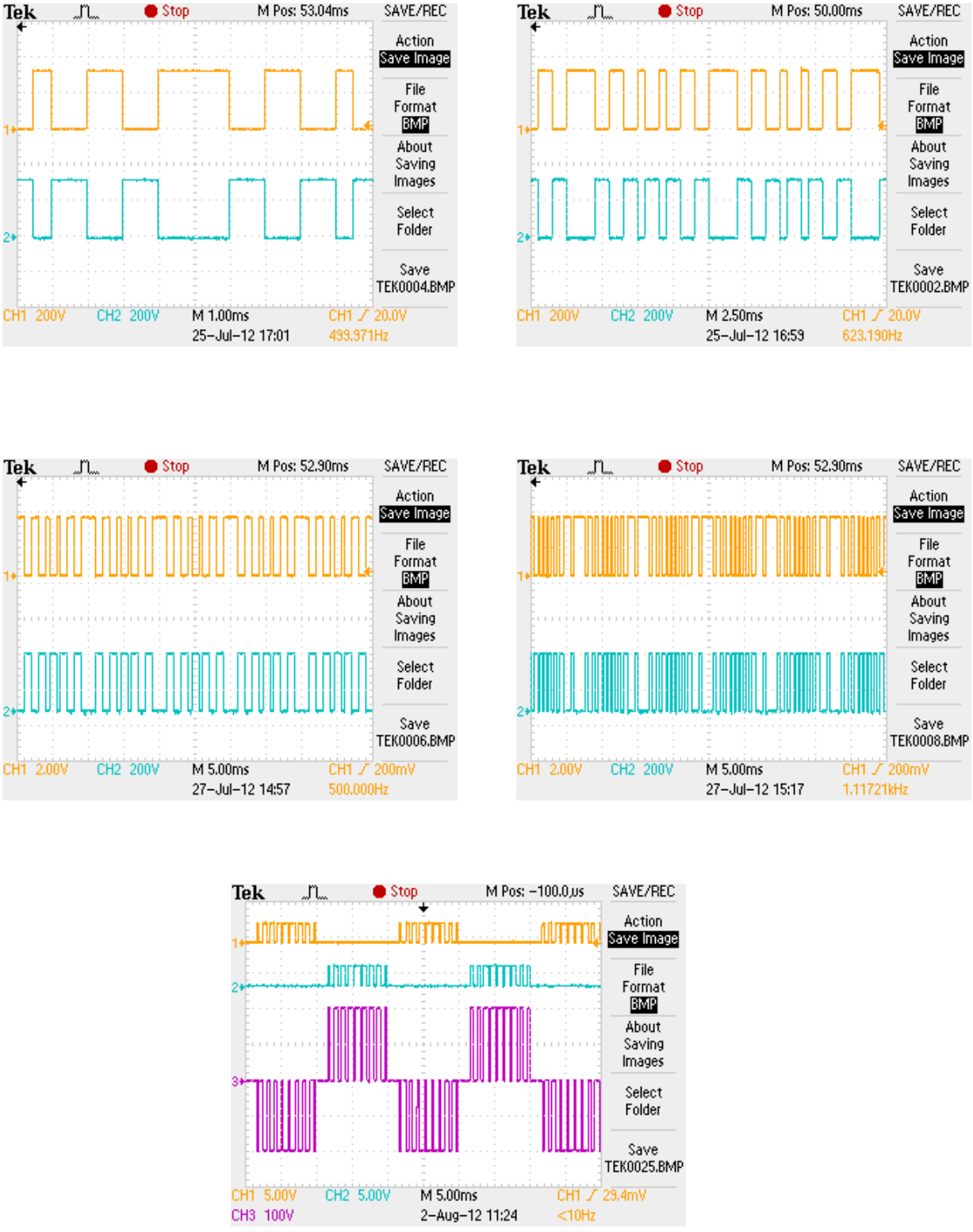


Fig. 5.7: Control pulses for different frequencies and the output voltage of the inverter and cycloconverter

5.5 Summary

In this chapter the controller of the MOSFET switches is covered. There are so many controllers which can be used in such applications, however the reason for selecting the ChipKit microcontroller is mainly due to its cheap price (£23) and the ease of use. The driver circuits and the Optocouplers are introduced in this chapter. Practical result of the final output is demonstrated.

CHAPTER 6: CONCLUSIONS AND FUTURE WORK

6.1 Conclusions

In this thesis different types of UPS system have been reviewed. It showed that the transformer is an essential element in UPS systems and this is mainly because of the need for isolation between the input and output as well as the need to keep the DC voltage level at low value for safety reasons. In order to make a compact and light UPS system (the main aim of this thesis), the step-down and step-up transformers are replaced with single high frequency transformer. In order to reduce the size of the transformer (hence the weight), the transformers are replaced with a single high frequency one. This is mainly because the cross section area of the transformer is inversely proportion to its operating frequency.

In order to achieve that, two new configurations are introduced in this thesis. The basic principle for both configuration is to step the frequency up before the transformer and then to step it down again after the transformer. By doing that the input and output frequencies are kept at 50 Hz while the transformer frequency is at higher frequency of 500 Hz, 1 kHz, 5 kHz or 10 kHz.. Simulation results for different high frequency link are given in both the analysis chapter and in Appendix E . The harmonic spectra for the transformer voltage and the final output voltage are covered and it shows that the 50Hz component does not go through the transformer.

Practical implementation of the proposed UPS system is presented in this thesis. A microcontroller is used to generate the required pulses and Optocouplers & MOSFET drivers are used to feed the appropriate drive signals to the MOSFET inverter and cycloconverter.

In general the proposed HF UPS system proved to be viable especially for compact applications where minimising the size and the weight of the UPS system is a great advantage. It is obvious that in the proposed HF UPS system there is one extra converter

used, however from the size and weight consideration this is very small addition in comparison with the transformer reduction in size and weight.

In both typical and the HF UPS systems a filter is required at the output. In the typical UPS system the filter is needed to filter out the harmonics generated from the switching pattern of the inverter circuit, according to the PWM carrier frequency. In HF UPS system also a filter is needed to filter the high frequency generated within the system. This could be higher than that of the typical UPS system and therefore easier to filter. Since filter is required in the two cases, the filter design and analysis was not considered in this thesis.

In general the project ran smoothly apart from few obstacles. For example the simulation was straightforward using the ideal switches (SBREAK), but when MOSFET switches were used convergence problems start to appear within the simulation. With the growing experience in using PSPICE such problems disappeared. The work in the Power Lab was interrupted due to the lab refurbishment, and the electronic lab was used instead. Isolated channel oscilloscope has to be used in this project and such oscilloscope has to be moved between the two labs. However, that was also a good educational experience to see the effect of isolated and non-isolated oscilloscopes in this project with so many floating grounds.

Of course the practical work was not straightforward and it took longer time than expected, to not only build the circuit, but to get it working. The amount of the simulated and practical results obtained is so large in volume and only few selected ones were used in this thesis (with some more shown in Appendix E).

One conference paper was published as a result of this research work [30] (Appendix F).

6.2 Future Work

In the simulation results the HF link used were 500 Hz, 1 kHz, 5 kHz, and 10 kHz. As it has been demonstrated that the cross sectional area of the transformer core is inversely proportional to the switching frequency. However, the switching losses are proportional to the switching frequency. That means that at higher switching frequency the transformer are getting smaller but the losses are increased. Future work could investigate the optimum frequency for getting the correct balance between the power losses and the core area as shown in the sketch in Fig. 6.1.

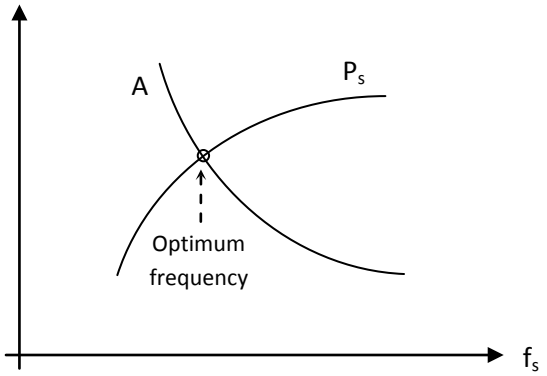


Fig. 6.1: Transformer cross-sectional area and switching losses vs the operating frequency

Also different types of transformer cores (ferrite, metglas, etc.) could be investigated in more depth in order to find out which one gives the best performance at the optimum frequency.

REFERENCES

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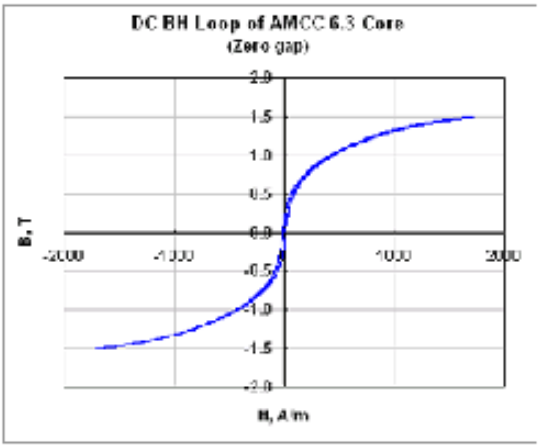
Appendix A: THE FERRORESONANT TRANSFORMER

POWERLITE® C-Cores are manufactured with iron based Metglas® amorphous Alloy 2605SA1.Their unique combination of low loss and high saturation flux density take advanced power conditioning applications to higher performance levels than previously possible with conventional ferromagnetic
Materials.



Applications

For a wide range of high frequencies and hot-spot temperatures (up to Class F), POWERLITE C-Cores are used in a growing list of advanced power conditioning applications including:

- UPS and SMPS Power Factor Correction Chokes
- UPS Harmonic Filter Inductors
- High-Power Outdoor Industrial Ballasts
- Welding Power Supplies
- High-Speed Rail Power Systems

Benefits

Manufactured in a variety of ultra-efficient core configurations, POWERLITE C-Cores provide significant cost, design and performance benefits over ordinary Si-Fe, ferrite and MPP cores such as:

- High Saturation Flux Density (1.56 T)
- Low Profile – enables weight and volume reductions of up to 50%
- Low Temperature Rise – enabling smaller compact designs
- Low Loss – resulting from micro-thin Metglas ribbon (25 µm)

Physical Properties METGLAS Alloy 2605SA1

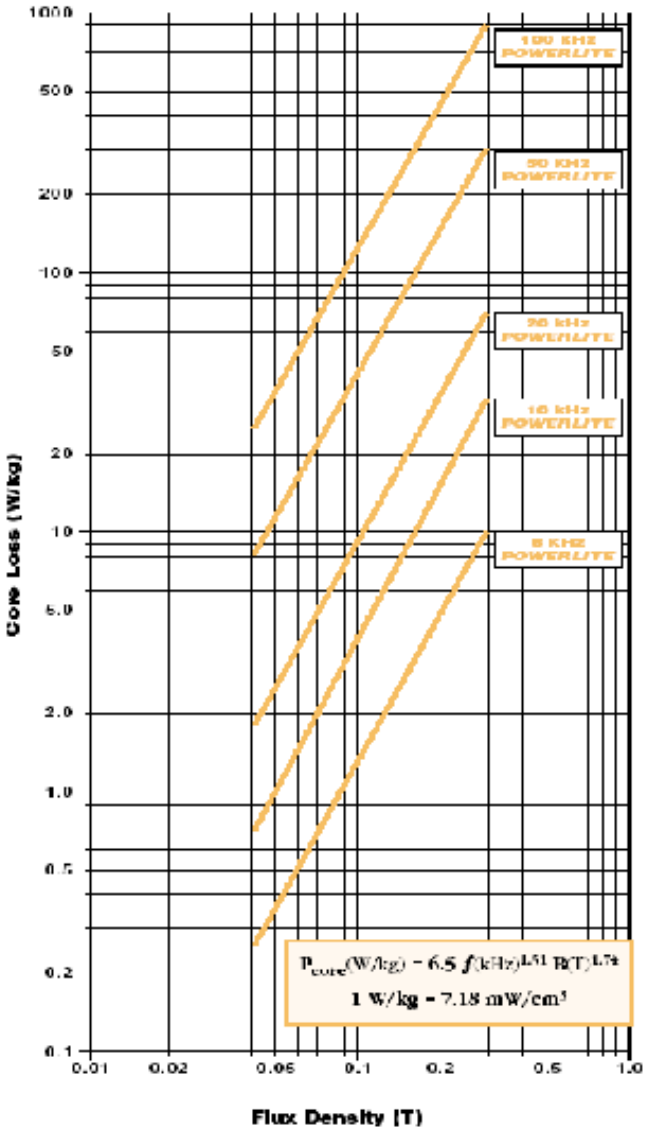
Ribbon Thickness (µm)	23
Density (g/cm^3)	7.18
Thermal Expansion (ppm/°C)	7.6
Crystallization Temperature (°C)	508
Curie Temperature (°C)	399
Continuous Service Temperature (°C)	150
Tensile Strength (MN/m2)	1k-1.7k
Elastic Modulus (GN/m2)	100-110
Vicker's Hardness (50g load)	900

Magnetic Properties METGLAS Powerlite Cores

Saturation Flux Density (T)	1.56
Permeability (depending on gap size)	VARIABLE
Saturation Magnetostriction (ppm)	27
Electrical Resistivity (µΩ.cm)	130

email: metglas@metglas.com
1-800-581-7654

Core Loss vs. Flux Density† @ 25°C



† *These curves were determined from ac data; use 1/2 the actual B to determine core loss for unidirectional applications.*

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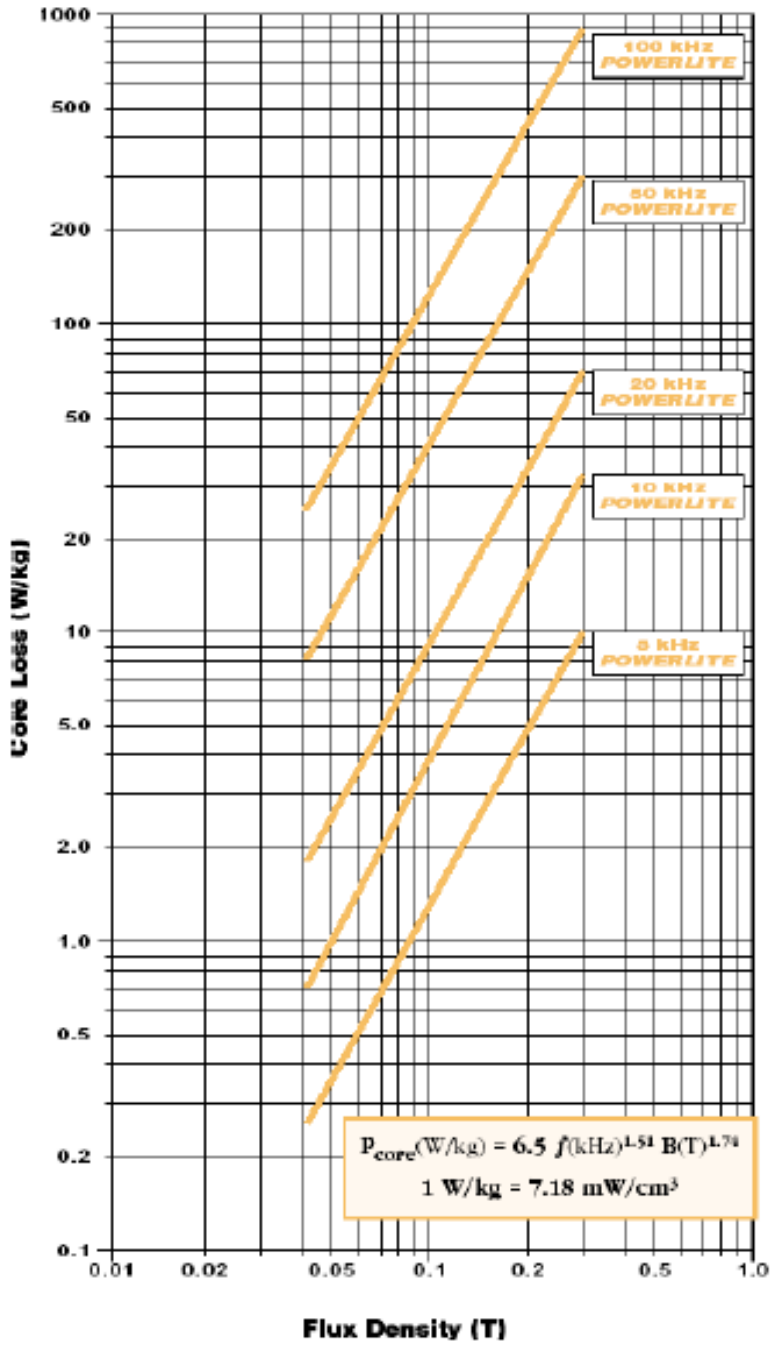
Core Loss vs. Flux Density† @ 25°C



† *These curves were determined from ac data; use 1/2 the actual ΔB to determine core loss for unidirectional applications.*

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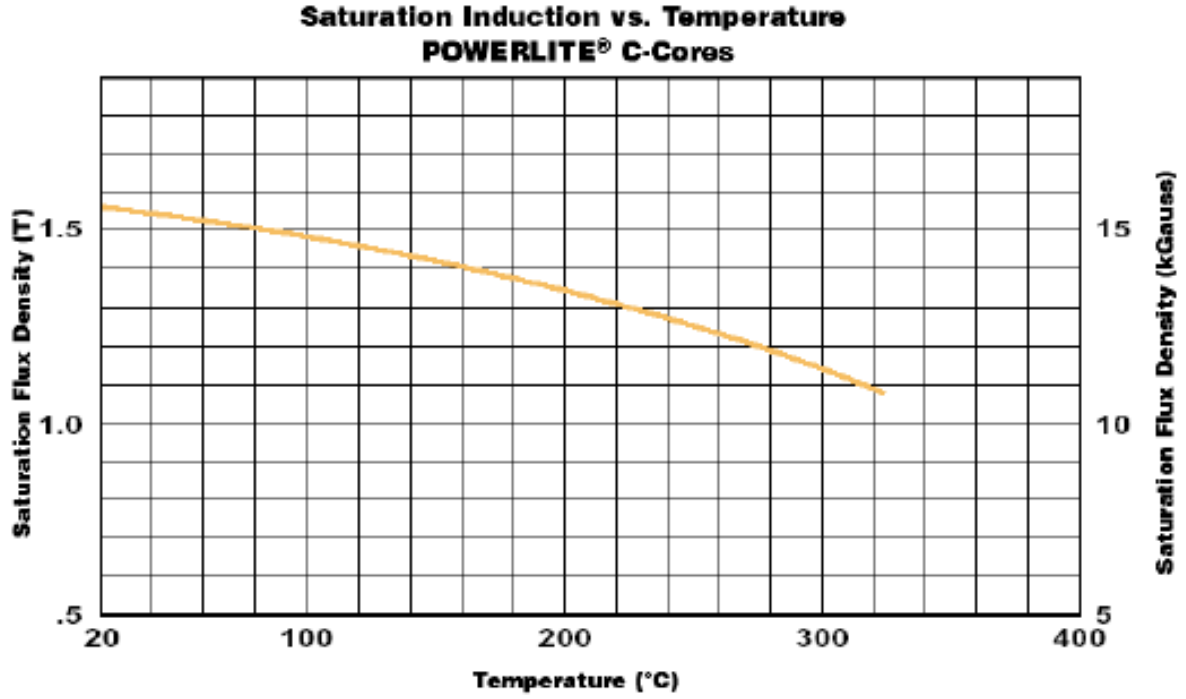

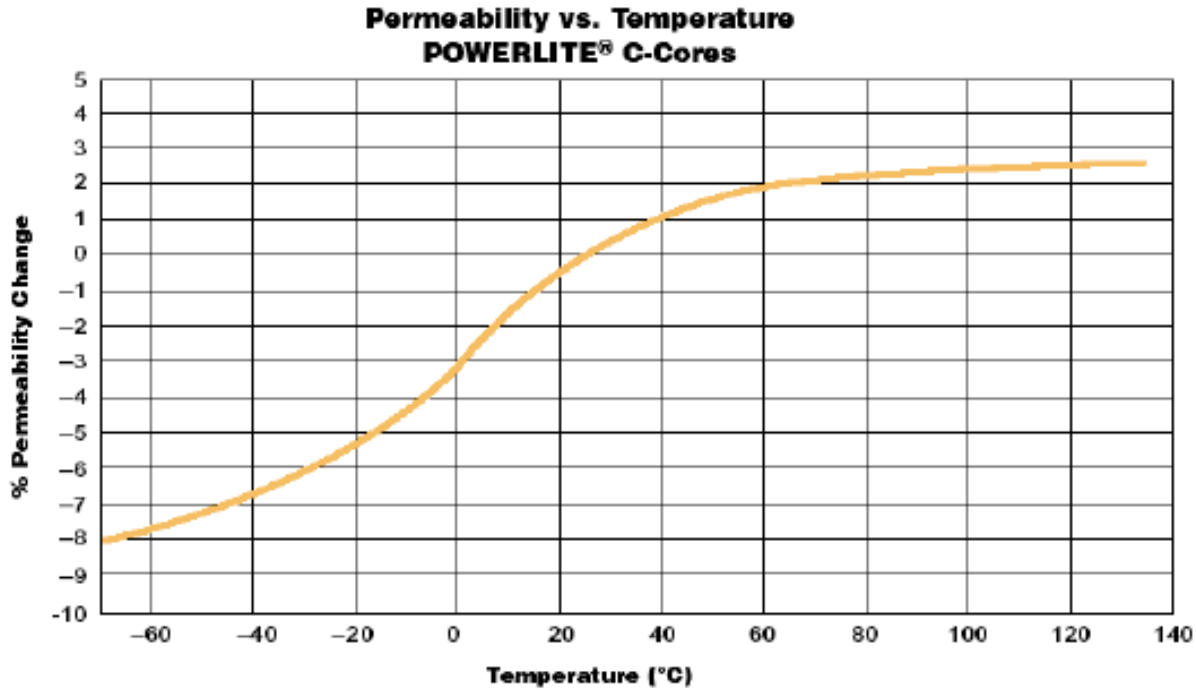

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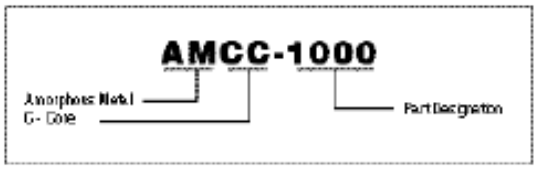
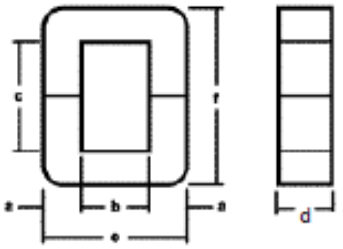
Product Code Designation





POWERLITE® C - Cores

	CORE DIMENSION										PERFROMANCE PARAMETERS				
Core No.	a (mm)	±	b (mm) ref *	c (mm) ref *	d (mm)	±	e (mm)	±	f (mm)	±	lm (cm)	Ac (cm^2)	Wa (cm^2)	Ap (cm^4)	Mass (g)
AMCC 4	9.0	0.50	10.0	32.80	15.0	0.50	28.00	1.50	50.8	1.25	12.20	1.11	3.30	3.60	99
AMCC 6.3	10.0	0.50	11.0	33.00	20.0	0.50	31.00	1.00	53.0	2.00	12.80	1.60	3.60	6.0	154
AMCC 8	11.0	0.80	13.0	30.00	20.0	0.50	35.00	1.00	52.0	2.00	13.00	1.80	3.90	7.00	172
AMCC 10	11.0	0.80	13.0	40.00	20.0	0.50	35.00	1.00	62.0	2.00	15.40	1.80	5.20	9.40	198
AMCC 16A	11.0	0.80	13.0	40.00	25.0	0.50	35.00	1.00	62.0	2.00	15.10	2.30	5.20	11.70	248
AMCC 16B	11.0	0.80	13.0	50.00	25.0	0.50	35.00	1.00	72.0	2.00	17.00	2.30	6.50	14.70	281
AMCC 20	11.0	0.80	13.0	50.00	30.0	0.50	35.00	1.00	72.0	2.00	17.50	2.70	6.50	17.60	337
AMCC 25	13.0	0.80	15.0	56.00	25.0	0.50	41.00	1.00	82.0	2.00	19.60	2.70	8.40	22.40	379
AMCC 32	13.0	0.80	15.0	56.00	30.0	0.50	41.00	1.00	82.0	2.00	20.00	3.20	8.40	26.90	454
AMCC 40	13.0	0.80	15.0	56.00	35.0	0.50	41.00	1.00	82.0	2.00	19.90	3.70	8.40	31.30	530
AMCC 50	16.0	1.00	20.0	70.00	25.0	0.50	52.00	1.00	102.0	3.00	24.90	3.30	14.00	45.90	586
AMCC 63	16.0	1.00	20.0	70.00	30.0	0.50	52.00	1.00	102.0	3.00	25.30	3.90	14.00	55.10	703
AMCC 80	16.0	1.00	20.0	70.00	40.0	1.00	52.00	1.00	102.0	3.00	25.40	5.20	14.00	73.50	938
AMCC 100	16.0	1.00	20.0	70.00	45.0	1.00	52.00	1.00	102.0	3.00	25.00	5.90	14.00	82.7	1,055
AMCC 168S	20.4	0.50	30.0	154.20	20.0	0.50	70.50	1.25	195.0	3.00	45.40	3.35	45.80	153.2	1,101
AMCC 125	19.0	1.00	25.0	83.00	35.0	1.00	63.00	1.00	121.0	3.00	30.20	5.50	20.80	113.1	1,166
AMCC 160	19.0	1.00	25.0	83.00	40.0	1.00	63.00	1.00	121.0	3.00	28.50	6.20	20.80	129.3	1,333
AMCC 200	19.0	1.00	25.0	83.00	50.0	1.00	63.00	1.00	121.0	3.00	29.80	7.80	20.80	161.6	1,666
AMCC 367S	25.8	1.00	67.0	97.80	25.0	0.70	117.60	1.50	149.4	1.50	43.78	5.29	63.81	340.1	1,668
AMCC 250	19.0	1.00	25.0	90.00	60.0	1.00	63.00	1.00	128.0	3.00	31.40	9.30	22.50	210.3	2,095
AMCC 320	22.0	1.00	35.0	85.00	50.0	1.00	79.00	1.00	129.0	4.00	32.50	9.00	29.80	268.3	2,167
AMCC 400	22.0	1.00	35.0	85.00	65.0	1.00	79.00	1.00	129.0	4.00	33.60	11.70	29.80	348.8	2,817
AMCC 500	25.0	1.00	40.0	85.00	55.0	1.00	90.00	1.00	135.0	4.00	35.60	11.30	34.00	383.4	2,890
AMCC 630	25.0	1.00	40.0	85.00	70.0	1.00	90.00	1.00	135.0	4.00	35.60	14.30	34.00	487.9	3,678
AMCC 800A	25.0	1.00	40.0	85.00	85.0	1.50	90.00	1.00	135.0	4.00	35.60	17.40	34.00	592.5	4,466
AMCC 800B	30.0	1.00	40.0	95.00	85.0	1.50	100.00	1.00	155.0	4.00	39.30	21.00	38.00	794.6	5,972
AMCC 1000	33.0	1.00	40.0	105.00	85.0	1.50	106.00	1.00	171.0	5.00	42.70	23.00	42.00	966.0	7,109

** Products generally do not fully comply with material characteristics – deviations may occur due to shape and size.*

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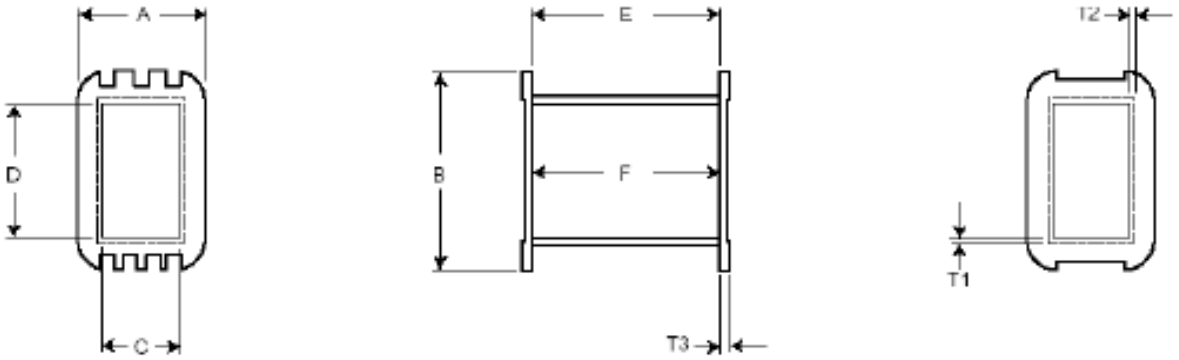
POWERLITE® C-Cores – Bobbins



BOBBIN NUMBER	A (mm)	B (mm)	C (mm)	D (mm)	E (mm)	F (mm)	T1 (mm)	T2 (mm)	T3 (mm)
AMCC-6.3BOB	21	31.5	11.5	21.5	30	32	1.0	1.0	2.0
AMCC-8BOB	24.5	34	13	21.5	27.5	29.5	1.0	1.0	2.0
AMCC-10BOB	25	34	12	20.5	38	40	1.0	1.0	2.0
AMCC-16ABOB	25	39	12	25.5	38	40	1.0	1.2	2.0
AMCC-16BBOB	25	39	12	25.5	48	50	1.0	1.2	2.0
AMCC-20BOB	25	44	12	30.5	48	50	1.0	1.2	2.0
AMCC-25BOB	27.5	42.5	15.5	26.5	52.5	55	1.0	1.2	2.2
AMCC-32BOB	28	49	14	30.5	53	56	1.2	1.5	2.2
AMCC-40BOB	27.5	55	15.5	38.5	52	54.5	1.0	1.2	2.2
AMCC-50BOB	36	48	17	25.5	67	70	1.5	1.8	2.4
AMCC-63BOB	35	56	18	31.5	66	68	1.2	1.8	2.4
AMCC-80BOB	36	63	17	41	67	70	1.2	1.8	2.4
AMCC-100BOB	35.5	70	18	47	66.5	69.5	1.2	1.8	2.4

POWERLITE® C-Core Bobbins - Material Properties

MATERIAL: Arnite
FLAMMABILITY RATING: UL94V0
TEMPERATURE RATING: Vical Softening Point = 200°C

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Appendix B: MICROCONTROLLER PROGRAM USED FOR GENERATING THE HF SIGNALS

This appendix contains the code used for generating the HF control pulses. The width of the pulses are generated from the simulated results (Figs. 4.36, 4.38, 4.40, 4.42)

```
//PWM Output for Inverter
//Output Pins 12 & 13 are used
//We can use ports from 1 to 13, also we
can use 28 to 41.  There are so many grounds
void setup() {
 pinMode(13, OUTPUT);
 pinMode(12, OUTPUT);
}
void loop() {
 digitalWrite(13, LOW);
 digitalWrite(12, HIGH);

 delayMicroseconds(250);
//the above is for 2.5ms delay

 digitalWrite(13, HIGH);
 digitalWrite(12, LOW);

 delayMicroseconds(100);

 digitalWrite(13, LOW);
 digitalWrite(12, HIGH);

 delayMicroseconds(500);

 digitalWrite(13, HIGH);
 digitalWrite(12, LOW);
 delayMicroseconds(250);

 digitalWrite(13, LOW);
 digitalWrite(12, HIGH);

 delayMicroseconds(500);

 digitalWrite(13, HIGH);
 digitalWrite(12, LOW);

 delayMicroseconds(400);

 digitalWrite(13, LOW);
 digitalWrite(12, HIGH);

 delayMicroseconds(500);

 digitalWrite(13, HIGH);
 digitalWrite(12, LOW);

 delay(1);

 digitalWrite(13, LOW);
 digitalWrite(12, HIGH);

 delayMicroseconds(500);
```

```
digitalWrite(13, HIGH);
 digitalWrite(12, LOW);

  delay(2);

 digitalWrite(13, LOW);
 digitalWrite(12, HIGH);

 delayMicroseconds(500);

 digitalWrite(13, HIGH);
 digitalWrite(12, LOW);

 delay(1);

 digitalWrite(13, LOW);
 digitalWrite(12, HIGH);

 delayMicroseconds(500);

 digitalWrite(13, HIGH);
 digitalWrite(12, LOW);

 delayMicroseconds(400);

 digitalWrite(13, LOW);
  digitalWrite(12, HIGH);

 delayMicroseconds(500);

 digitalWrite(13, HIGH);
 digitalWrite(12, LOW);

 delayMicroseconds(250);

 digitalWrite(13, LOW);
 digitalWrite(12, HIGH);

 delayMicroseconds(500);

 digitalWrite(13, HIGH);
 digitalWrite(12, LOW);

 delayMicroseconds(100);

 digitalWrite(13, LOW);
 digitalWrite(12, HIGH);

 delayMicroseconds(250);

 digitalWrite(13, HIGH);
 digitalWrite(12, LOW);
 }
```

Appendix C: THE OPTOCOUPLERS AND THE MOSFET DRIVERS DATASHEETS

FAIRCHILD SEMICONDUCTOR®

January 2011

Single-Channel: 6N137, HCPL2601, HCPL2611
Dual-Channel: HCPL2630, HCPL2631
High Speed 10MBit/s Logic Gate Optocouplers

Features

- Very high speed – 10 MBit/s
- Superior CMR – 10 kV/µs
- Double working voltage-480V
- Fan-out of 8 over -40°C to +85°C
- Logic gate output
- Strobable output
- Wired OR-open collector
- U.L. recognized (File # E90700)

Applications

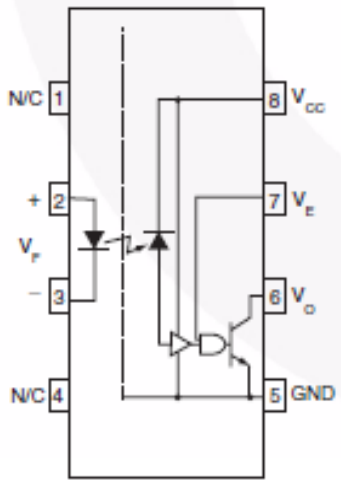
- Ground loop elimination
- LSTTL to TTL, LSTTL or 5-volt CMOS
- Line receiver, data transmission
- Data multiplexing
- Switching power supplies
- Pulse transformer replacement
- Computer-peripheral interface

Description

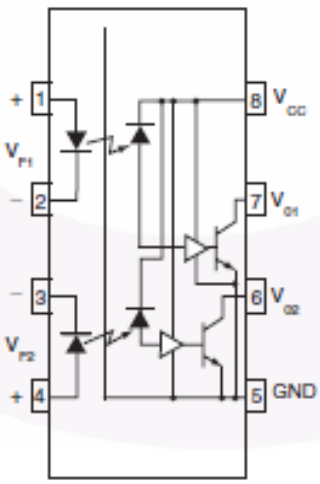
The 6N137, HCPL2601, HCPL2611 single-channel and HCPL2630, HCPL2631 dual-channel optocouplers consist of a 850 nm AlGaAS LED, optically coupled to a very high speed integrated photo-detector logic gate with a strobable output. This output features an open collector, thereby permitting wired OR outputs. The coupled parameters are guaranteed over the temperature range of -40°C to +85°C. A maximum input signal of 5mA will provide a minimum output sink current of 13mA (fan out of 8).

An internal noise shield provides superior common mode rejection of typically 10kV/µs. The HCPL2601 and HCPL2631 has a minimum CMR of 5kV/µs. The HCPL2611 has a minimum CMR of 10kV/µs.

Schematics



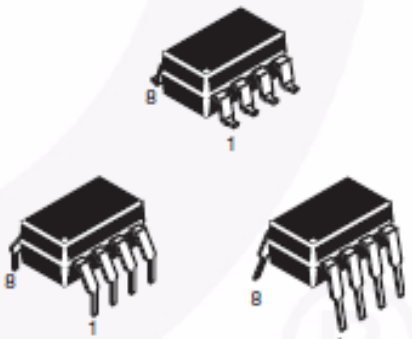
6N137
HCPL2601
HCPL2611



HCPL2630
HCPL2631

A 0.1µF bypass capacitor must be connected between pins 8 and 5[1].

Package Outlines



Truth Table (Positive Logic)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H
H	NC	L
L	NC	H

Absolute Maximum Ratings (T_A = 25°C unless otherwise specified)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Value	Units
T_{STG}	Storage Temperature		-55 to +125	°C
T_{OPR}	Operating Temperature		-40 to +85	°C
T_{SOL}	Lead Solder Temperature (for wave soldering only)*		260 for 10 sec	°C
EMITTER				
I_F	DC/Average Forward	Single Channel	50	mA
	Input Current	Dual Channel (Each Channel)	30	
V_E	Enable Input Voltage Not to Exceed V_{CC} by more than 500mV	Single Channel	5.5	V
V_R	Reverse Input Voltage	Each Channel	5.0	V
P_I	Power Dissipation	Single Channel	100	mW
		Dual Channel (Each Channel)	45	
DETECTOR				
V_{CC} (1 minute max)	Supply Voltage		7.0	V
I_O	Output Current	Single Channel	50	mA
		Dual Channel (Each Channel)	50	
V_O	Output Voltage	Each Channel	7.0	V
P_O	Collector Output	Single Channel	85	mW
	Power Dissipation	Dual Channel (Each Channel)	60	

*For peak soldering reflow, please refer to the Reflow Profile on page 11.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
I_{FL}	Input Current, Low Level	0	250	µA
I_{FH}	Input Current, High Level	*6.3	15	mA
V_{CC}	Supply Voltage, Output	4.5	5.5	V
V_{EL}	Enable Voltage, Low Level	0	0.8	V
V_{EH}	Enable Voltage, High Level	2.0	V_{CC}	V
T_A	Low Level Supply Current	-40	+85	°C
N	Fan Out (TTL load)		8	

*6.3mA is a guard banded value which allows for at least 20% CTR degradation. Initial input current threshold value is 5.0mA or less.

Electrical Characteristics (T_A = 0 to 70°C unless otherwise specified)

Individual Component Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.*	Max.	Unit
EMITTER							
V_F	Input Forward Voltage	I_F = 10mA				1.8	V
			T_A = 25°C		1.4	1.75	
B_{VR}	Input Reverse Breakdown Voltage	I_R = 10µA		5.0			V
C_{IN}	Input Capacitance	V_F = 0, f = 1MHz			60		pF
$\Delta V_F / \Delta T_A$	Input Diode Temperature Coefficient	I_F = 10mA			-1.4		mV/°C
DETECTOR							
I_{CCH}	High Level Supply Current	V_{CC} = 5.5V, I_F = 0mA, V_E = 0.5V	Single Channel		7	10	mA
			Dual Channel		10	15	
I_{CCL}	Low Level Supply Current	Single Channel	V_{CC} = 5.5V, I_F = 10mA		9	13	mA
		Dual Channel	V_E = 0.5V		14	21	
I_{EL}	Low Level Enable Current	V_{CC} = 5.5V, V_E = 0.5V			-0.8	-1.6	mA
I_{EH}	High Level Enable Current	V_{CC} = 5.5V, V_E = 2.0V			-0.6	-1.6	mA
V_{EH}	High Level Enable Voltage	V_{CC} = 5.5V, I_F = 10mA		2.0			V
V_{EL}	Low Level Enable Voltage	V_{CC} = 5.5V, I_F = 10mA[3]				0.8	V

Switching Characteristics (T_A = -40°C to +85°C, V_{CC} = 5V, I_F = 7.5mA unless otherwise specified)

Symbol	AC Characteristics	Test Conditions		Min.	Typ.*	Max.	Unit
T_{PLH}	Propagation Delay Time to Output HIGH Level	R_L = 350Ω, C_L = 15pF[4] (Fig. 12)	T_A = 25°C	20	45	75	ns
						100	
T_{PHL}	Propagation Delay Time to Output LOW Level	T_A = 25°C[5]		25	45	75	ns
		R_L = 350Ω, C_L = 15pF (Fig. 12)				100	
$\lvert T_{PHL} - T_{PLH} \rvert$	Pulse Width Distortion	(R_L = 350Ω, C_L = 15pF (Fig. 12)			3	35	ns
t_r	Output Rise Time (10–90%)	R_L = 350Ω, C_L = 15pF[6] (Fig. 12)			50		ns
t_f	Output Rise Time (90–10%)	R_L = 350Ω, C_L = 15pF[7] (Fig. 12)			12		ns
t_{ELH}	Enable Propagation Delay Time to Output HIGH Level	I_F = 7.5mA, V_{EH} = 3.5V, R_L = 350Ω, C_L = 15pF[8] (Fig. 13)			20		ns
t_{EHL}	Enable Propagation Delay Time to Output LOW Level	I_F = 7.5mA, V_{EH} = 3.5V, R_L = 350Ω, C_L = 15pF[9] (Fig. 13)			20		ns
$\lvert CM_H \rvert$	Common Mode Transient Immunity (at Output HIGH Level)	T_A = 25°C, $\lvert V_{CM} \rvert$ = 50V (Peak), I_F = 0mA, V_{OH} (Min.) = 2.0V, R_L = 350Ω[10] (Fig. 14)	6N137, HCPL2630		10,000		V/µs
			HCPL2601, HCPL2631	5000	10,000		
		$\lvert V_{CM} \rvert$ = 400V	HCPL2611	10,000	15,000		V/µs
$\lvert CM_L \rvert$	Common Mode Transient Immunity (at Output LOW Level)	R_L = 350Ω, I_F = 7.5mA, V_{OL} (Max.) = 0.8V, T_A = 25°C[11] (Fig. 14)	6N137, HCPL2630		10,000		
			HCPL2601, HCPL2631	5000	10,000		
		$\lvert V_{CM} \rvert$ = 400V	HCPL2611	10,000	15,000		

Electrical Characteristics (Continued)

Transfer Characteristics (T_A = -40 to +85°C unless otherwise specified)

Symbol	DC Characteristics	Test Conditions	Min.	Typ.*	Max.	Unit
I_{OH}	HIGH Level Output Current	V_{CC} = 5.5V, V_O = 5.5V, I_F = 250µA, V_E = 2.0V(2)			100	µA
V_{OL}	LOW Level Output Current	V_{CC} = 5.5V, I_F = 5mA, V_E = 2.0V, I_{CL} = 13mA(2)		.35	0.6	V
I_{FT}	Input Threshold Current	V_{CC} = 5.5V, V_O = 0.6V, V_E = 2.0V, I_{OL} = 13mA		3	5	mA

Isolation Characteristics (T_A = -40°C to +85°C unless otherwise specified.)

Symbol	Characteristics	Test Conditions	Min.	Typ.*	Max.	Unit
I_{I-O}	Input-Output Insulation Leakage Current	Relative humidity = 45%, T_A = 25°C, t = 5s, V_{I-O} = 3000 VDC(12)			1.0*	µA
V_{ISO}	Withstand Insulation Test Voltage	RH < 50%, T_A = 25°C, I_{I-O} ≤ 2µA, t = 1 min.(12)	2500			V_{RMS}
R_{I-O}	Resistance (Input to Output)	V_{I-O} = 500V(12)		10^{12}		Ω
C_{I-O}	Capacitance (Input to Output)	f = 1MHz(12)		0.6		pF

*All Typicals at V_{CC} = 5V, T_A = 25°C

Notes:

1. The V_{CC} supply to each optoisolator must be bypassed by a 0.1µF capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package V_{CC} and GND pins of each device.
2. Each channel.
3. Enable Input – No pull up resistor required as the device has an internal pull up resistor.
4. t_{PLH} – Propagation delay is measured from the 3.75mA level on the HIGH to LOW transition of the input current pulse to the 1.5 V level on the LOW to HIGH transition of the output voltage pulse.
5. t_{PHL} – Propagation delay is measured from the 3.75mA level on the LOW to HIGH transition of the input current pulse to the 1.5 V level on the HIGH to LOW transition of the output voltage pulse.
6. t_r – Rise time is measured from the 90% to the 10% levels on the LOW to HIGH transition of the output pulse.
7. t_f – Fall time is measured from the 10% to the 90% levels on the HIGH to LOW transition of the output pulse.
8. t_{ELH} – Enable input propagation delay is measured from the 1.5V level on the HIGH to LOW transition of the input voltage pulse to the 1.5V level on the LOW to HIGH transition of the output voltage pulse.
9. t_{EHL} – Enable input propagation delay is measured from the 1.5V level on the LOW to HIGH transition of the input voltage pulse to the 1.5V level on the HIGH to LOW transition of the output voltage pulse.
10. CM_H – The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the HIGH state (i.e., V_{OUT} > 2.0V). Measured in volts per microsecond (V/µs).
11. CM_L – The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the LOW output state (i.e., V_{OUT} < 0.8V). Measured in volts per microsecond (V/µs).
12. Device considered a two-terminal device: Pins 1, 2, 3 and 4 shorted together, and Pins 5, 6, 7 and 8 shorted together.

Dual Power MOSFET Driver

The ICL7667 is a dual monolithic high-speed driver designed to convert TTL level signals into high current outputs at voltages up to 15V. Its high speed and current output enable it to drive large capacitive loads with high slew rates and low propagation delays. With an output voltage swing only millivolts less than the supply voltage and a maximum supply voltage of 15V, the ICL7667 is well suited for driving power MOSFETs in high frequency switched-mode power converters. The ICL7667's high current outputs minimize power losses in the power MOSFETs by rapidly charging and discharging the gate capacitance. The ICL7667's inputs are TTL compatible and can be directly driven by common pulse-width modulation control ICs.

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ICL7667CBA*	7667 CBA	0 to 70	8 Ld SOIC (N)	M8.15
ICL7667CBAZA	7667 CBAZ	0 to 70	8 Ld SOIC (N) (Pb-Free)	M8.15
ICL7667CPA*	7667 CPA	0 to 70	8 Ld PDIP	E8.3
ICL7667CPAZ	7667 CPAZ	0 to 70	8 Ld PDIP* (Pb-Free)	E8.3

*Add "-T" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

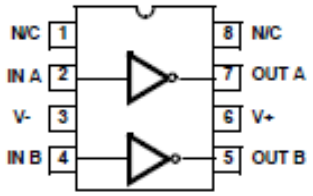
- Fast Rise and Fall Times
  - 30ns with 1000pF Load
- Wide 15V Supply Voltage Range
  - V+ = +4.5V to +15V
  - V- = -15V to Ground (0V)
- Low Power Consumption
  - 4mW with Inputs Low
  - 20mW with Inputs High
- TTL/CMOS Input Compatible Power Driver
  - R_{OUT} = 7Ω Typ
- Direct Interface with Common PWM Control ICs
- Pin Equivalent to DS0026/DS0056; TSC426
- Pb-Free Available (RoHS Compliant)

Applications

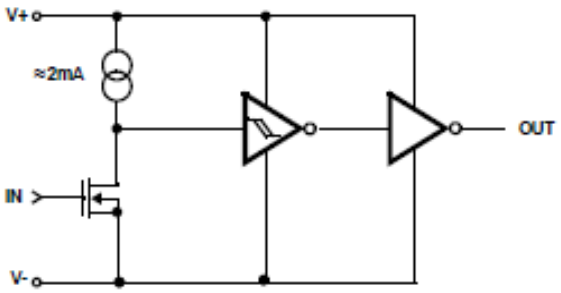
- Switching Power Supplies
- DC/DC Converters
- Motor Controllers

Pinout

ICL7667
(8 LD PDIP, SOIC)
TOP VIEW



Functional Diagram (Each Driver)



Absolute Maximum Ratings

Supply Voltage V+ to V- . . . . . ±18V
Input Voltage . . . . . V- -0.3V to V+ +0.3V
Package Dissipation, T_A +25°C 500mW

Operating Conditions

ICL7667C . . . . . 0° to +70°C
Supply Voltages: V+ = +4.5V to +15V; V- = Ground to -15V
Logic Inputs: Logic Low = V- < Vin < 0.8V ; Logic High = 2.0V< Vin < V+

Thermal Information

Thermal Resistance (Typical, Note 1, 2)	θ_{JA} (°C/W)	θ_{JC}(°C/W)
8 Ld PDIP Package	150	N/A
8 Ld SOIC Package	170	N/A

Maximum Storage Temperature Range . . . . . -65° to +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)
Pb-Free Reflow Profile. . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp
Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Parameters with MIN and/or MAX limits are 100% tested at +25°C, V+ = 0V unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	SYMBOL	TEST CONDITIONS	ICL7667C, M T_A = +25°C			ICL7667M 0°C ≤ T_A ≤ +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
DC SPECIFICATIONS									
Logic 1 Input Voltage	V_{IH}	V+ = 4.5V	2.0	-	-	2.0	-	-	V
Logic 1 Input Voltage	V_{IH}	V+V+ = 15V	2.0	-	-	2.0	-	-	V
Logic 0 Input Voltage	V_{IL}	V+ = 4.5V	-	-	0.8	-	-	0.5	V
Logic 0 Input Voltage	V_{IL}	V+ = 15V	-	-	0.8	-	-	0.5	V
Input Current	I_{IL}	V+ = 15V, V_{IN} = 0V and 15V	-0.1	-	0.1	-0.1	-	0.1	µA
Output Voltage High	V_{OH}	V+ = 4.5V and 15V	V+ -0.05	V+	-	V+ -0.1	V+	-	V
Output Voltage Low	V_{OL}	V+ = 4.5V and 15V	-	0	0.05	-	-	0.1	V
Output Resistance	R_{OUT}	V_{IN} = V_{IL}, I_{OUT} = -10mA, V+ = 15V	-	7	10	-	-	12	Ω
Output Resistance	R_{OUT}	V_{IN} = V_{IH}, I_{OUT} = 10mA, V+ = 15V	-	8	12	-	-	13	Ω
Power Supply Current	I_{CC}	V+ = 15V, V_{IN} = 3V both inputs	-	5	7	-	-	8	mA
Power Supply Current	I_{CC}	V+ = 15V, V_{IN} = 0V both inputs	-	150	400	-	-	400	µA
SWITCHING SPECIFICATIONS									
Delay Time	T_{D2}	(Figure 3)	-	35	50	-	-	60	ns
Rise Time	T_R	(Figure 3)	-	20	30	-	-	40	ns
Fall Time	T_F	(Figure 3)	-	20	30	-	-	40	ns
Delay Time	T_{D1}	(Figure 3)	-	20	30	-	-	40	ns

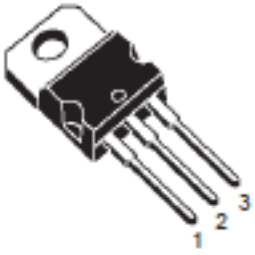
Appendix D: DATASHEETS FOR MOSFET IRF740

IRF740

N - CHANNEL 400V - 0.48 Ω - 10 A - TO-220 PowerMESH™ MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
IRF740	400 V	< 0.55 Ω	10 A

- TYPICAL $R_{DS(on)}$ = 0.48 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED



TO-220

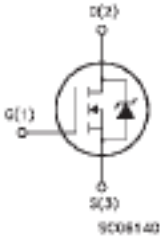
DESCRIPTION

This power MOSFET is designed using the company's consolidated strip layout-based MESH OVERLAY™ process. This technology matches and improves the performances compared with standard parts from various sources.

APPLICATIONS

- HIGH CURRENT SWITCHING
- UNINTERRUPTIBLE POWER SUPPLY (UPS)
- DC/DC COVERTERS FOR TELECOM, INDUSTRIAL, AND LIGHTING EQUIPMENT.

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	400	V
V_{DGR}	Drain- gate Voltage (R_{GS} = 20 kΩ)	400	V
V_{GS}	Gate-source Voltage	± 20	V
I_D	Drain Current (continuous) at T_c = 25 °C	10	A
I_D	Drain Current (continuous) at T_c = 100 °C	6.3	A
I_{DM}(•)	Drain Current (pulsed)	40	A
P_{tot}	Total Dissipation at T_c = 25 °C	125	W
	Derating Factor	1.0	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	4.0	V/ns
T_{stg}	Storage Temperature	-65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

(•) Pulse width limited by safe operating area (1) I_{SD} ≤10 A, di/dt ≤120 A/µs, V_{DD} ≤ $V_{(BR)DSS}$, Tj ≤ T_{JMAX}
First Digit of the Datecode Being Z or K Identifies Silicon Characterized in this Datasheet

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	1.0	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	62.5	oC/W
$R_{thc\text{-}sink}$	Thermal Resistance Case-sink	Typ	0.5	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose		300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	10	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	520	mJ

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA V_{GS} = 0	400			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating T_c = 125 °C			1 50	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20 V			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V I_D = 5.3 A		0.48	0.55	Ω
$I_{D(on)}$	On State Drain Current	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$ V_{GS} = 10 V	10			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$ I_D = 6 A	5.8			S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		1400 220 27		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Time Rise Time	V_{DD} = 200 V I_D = 5 A R_G = 4.7 Ω V_{GS} = 10 V (see test circuit, figure 3)		17 10		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 320 V I_D = 10.7 A V_{GS} = 10V		35 11 12	43	nC nC nC

SWITCHING OFF

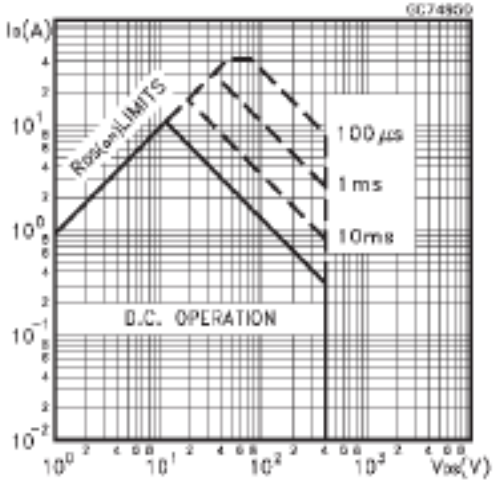
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	V_{DD} = 320 V I_D = 10 A R_G = 4.7 Ω V_{GS} = 10 V (see test circuit, figure 5)		10 10 17		ns ns ns

SOURCE DRAIN DIODE

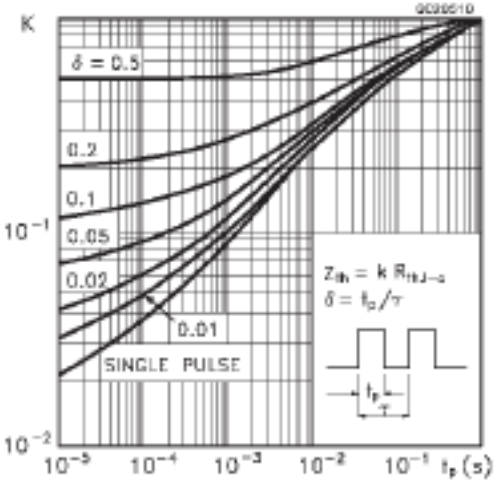
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (•)	Source-drain Current Source-drain Current (pulsed)				10 40	A A
V_{SD} (•)	Forward On Voltage	I_{SD} = 10 A V_{GS} = 0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} =10 A di/dt = 100 A/µs V_{DD} = 100 V T_j = 150 °C (see test circuit, figure 5)		370 3.2 17		ns µC A

(•) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %
(•) Pulse width limited by safe operating area

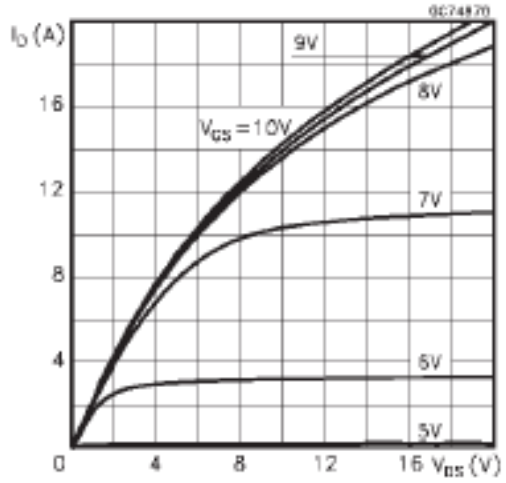
Safe Operating Area



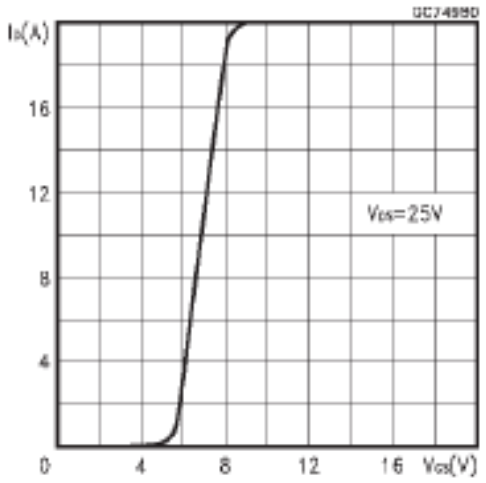
Thermal Impedance



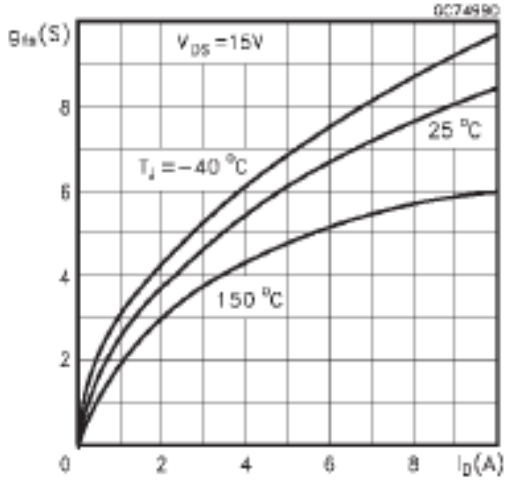
Output Characteristics



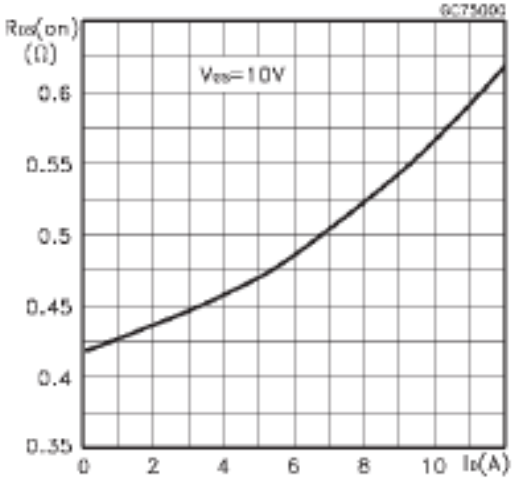
Transfer Characteristics



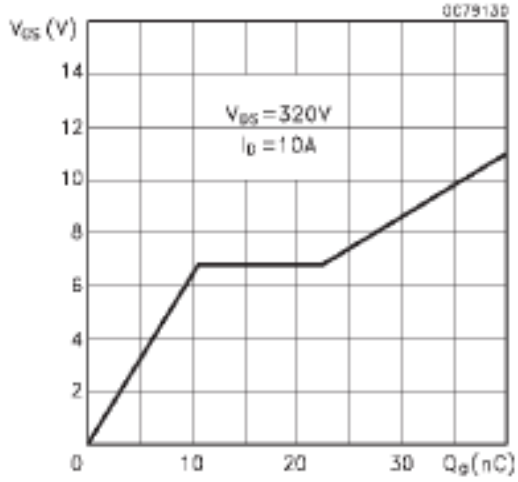
Transconductance



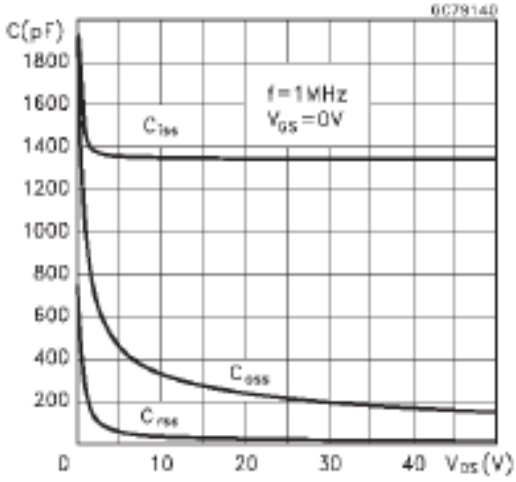
Static Drain-source On Resistance



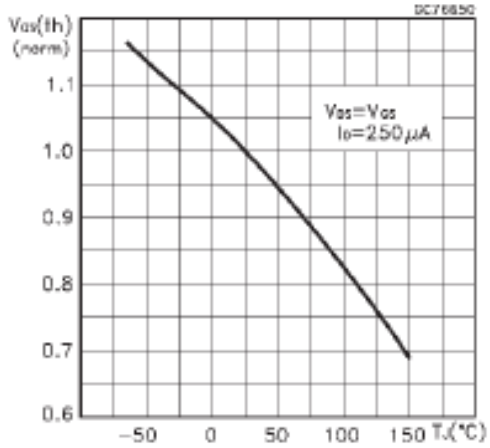
Gate Charge vs Gate-source Voltage



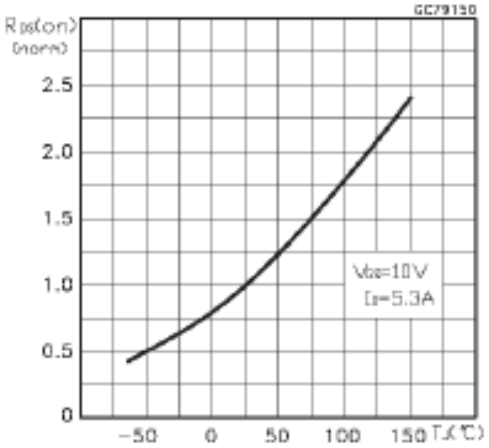
Capacitance Variations



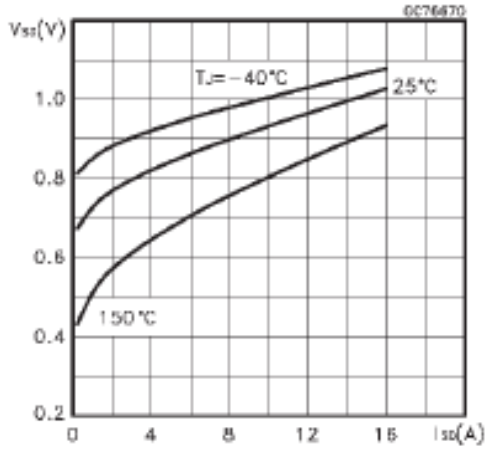
Normalized Gate Threshold Voltage vs Temperature



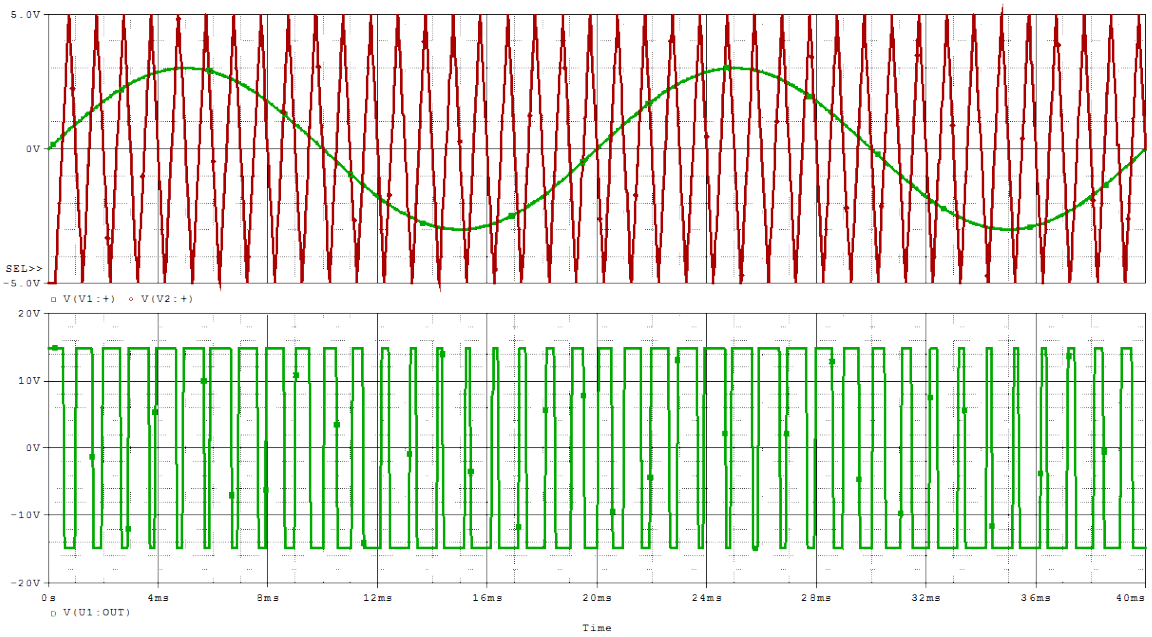
Normalized On Resistance vs Temperature



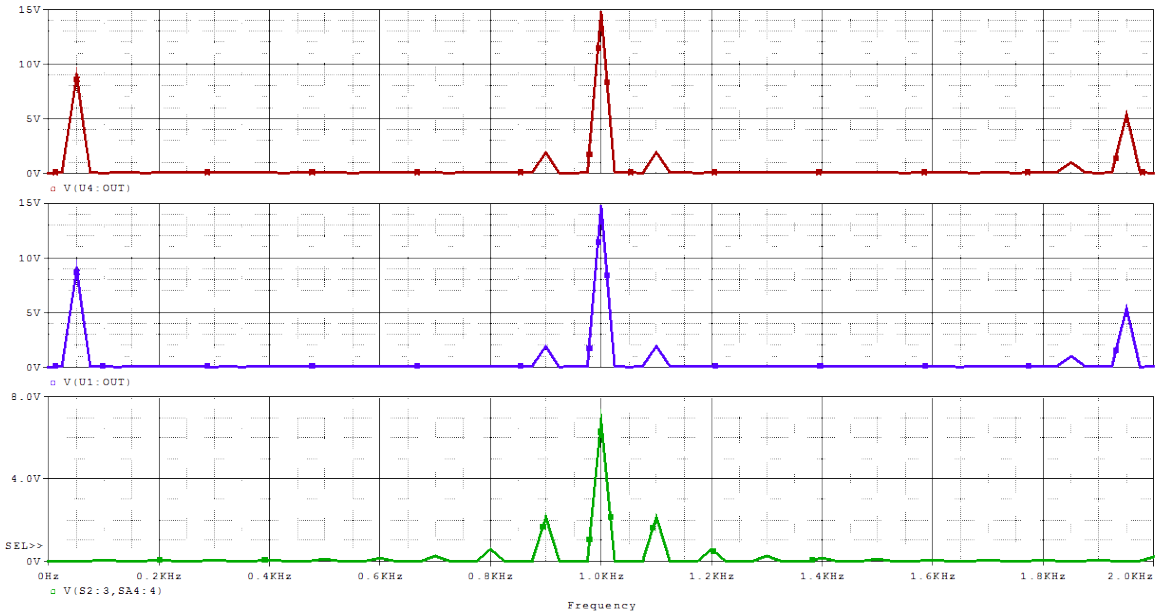
Source-drain Diode Forward Characteristics



Appendix E: EXTRA SIMULATION RESULTS



Generation of 1kHz PWM



Spectra of the witching and the transformer frequencie

Appendix F: PUBLISHED PAPER

High Frequency Inverter circuit for UPS Systems

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Abstract- **In this paper an On-Line UPS system is proposed. The traditional inverter in the double conversion On-Line UPS system is replaced with a high frequency inverter so that the size and hence the performance of the UPS is improved. The input as well as the output frequencies of the proposed UPS is still 50Hz, however the internal operating frequency of the UPS inverter is higher than 50Hz. The challenge in this proposed circuit is to keep the 50Hz go through the transformer windings without altering the transformer high-frequency design. The results presented in this paper are shown at 500Hz and this is mainly to demonstrate the idea. However, a much higher frequency can be used.**

Index Terms—**Inverter, High-frequency, UPS system, Transformers.**

I. Introduction

Uninterruptible Power Supply (UPS) systems are widely used nowadays for protecting critical loads. There are several UPS topologies available on the market which can come mainly under two types: off-line (including line interactive and standby ferro) and on-line (including double conversion and delta conversion) [1]. The off-line UPS system has the advantages of smaller size and less cost compared to the on-line system. However, the on-line is more effective particularly for very critical types of loads. The selection of a UPS system depends on economics, reliability, size and also effectiveness (particularly with non-linear loads such as computers).

In an off-line UPS (Fig. 1), the critical load is normally powered from the mains supply, and a small mains-driven charger keeps the UPS's batteries topped-up. The filter reduces spikes and RFI in the supply before it is supplied to the load and, under these conditions, the inverter does nothing. When the quality of the mains supply falls below a certain level, the inverter starts-up virtually instantaneously and takes over the task of supplying the critical load from the battery. This configuration is common in small loads (up to 1kVA).

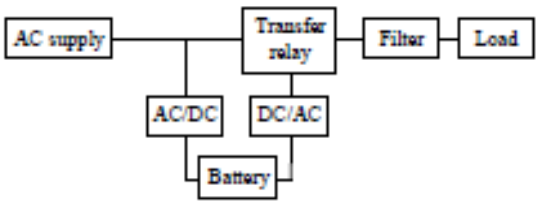

Fig. 1. Block diagram of a typical off-line UPS system

To meet the requirements of some very sensitive systems, the load cannot be supplied directly from the mains. The load must always be supplied from a source which is completely isolated from the mains supply which will ensure that both voltage and frequency variations are eliminated. An on-line UPS system is usually used in such application as shown in Fig. 2. The UPS output parameters are independent of the input and, under all conditions of mains supply, its output voltage and frequency will always be controlled within very closely defined limits.

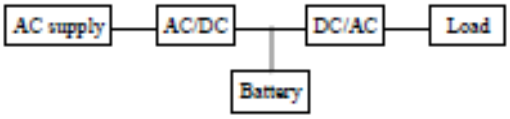

Fig. 2. Block diagram of a typical on-line UPS system

In office applications when on-line UPS system is used, it is desirable to have a low dc voltage level (12, 24, 48 V). To achieve that two transformers have to be used in order to setup up and step down the voltage levels as shown in Fig. 3.

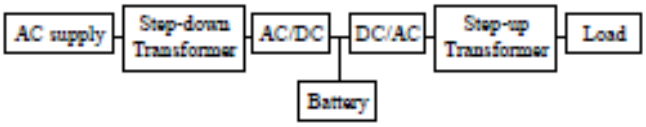

Fig. 3. Block diagram of a low voltage DC link on-line UPS system

As shown in this figure, the step down transformer is used to bring the supply voltage from 240 rms to 12/24/or 48 volts. The rectifier is then used to charge the battery as well as supplying the power to the load via the dc/ac inverter. Obviously another transformer is required to step up the output voltage of the inverter to the load. These transformers are operated at 50Hz fundamental frequency. About a third of the volume of the UPS is occupied by these transformers. The physical size, hence weight and overall cost of the UPS systems could be significantly reduced by operating these transformers at higher frequency than 50Hz. Advances in semiconductor technology make the operation of power converters at higher switching frequencies possible, thus the energy transmission can be accomplished with high frequency (HF) power conversion.

Authors believe that there is a gap in the market for effective, yet compact UPS systems. Advancements in electronics have reduced the costs of inverters considerably and have increased the reliability. However reduction in size is still long way to go particularly with low voltage DC link on-line UPS systems [2]. This is mainly because the growth of small powerful computers does not match with present UPS systems where the size of the transformers could be as large as half the size of the entire UPS system. Also the weight of the two transformers could exceed half the weight of the UPS system as shown in the size distribution in Fig. 4.

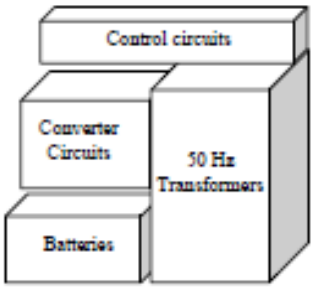

Fig. 4. Size distribution in a typical On-Line UPS system

The physical size, hence the weight and overall cost of UPS systems could be significantly reduced by operating these transformers at much higher frequency than 50 Hz. Analysis and simulation results of this proposed UPS system is presented in the following sections.

II. Analysis

In a typical transformer the flux generated in the core can be presented as:

$$\varphi = \phi_{max} \sin \omega t \quad (1)$$

$$E = N\frac{d\varphi}{dt} \quad (2)$$

$$E_{rms} = \frac{\omega N \phi_{max}}{\sqrt{2}} \quad (3)$$

For constant E_{rms}, ϕ_{max} is $\propto 1/\omega$

Where $\omega = 2\pi f$

Now, $\phi_{max} = B_{max} \times$ (Core cross sectional area of the transformer).

Therefore, for constant B_{max}:

Core cross sectional area of the transformer is $\propto 1/f$

For example, a 10 kHz transformer would, in theory, require a core area 200 times smaller than a 50 Hz transformer for the same power. In practice, the transformer could not be quite this small as the size of the windings and insulation cannot be reduced for the same power and voltage ratings. Also a very small transformer has less surface area to dissipate the heat.

The task is to design an on-line UPS system which operates internally at high frequency (in order to reduce the transformers size) and also to keep both output and input frequencies at 50 Hz.

III. Proposed Topology

In order to achieve the high frequency internal operation of the UPS system and keeping the input and output frequencies at 50Hz, the block diagram shown in Fig. 5 is proposed.

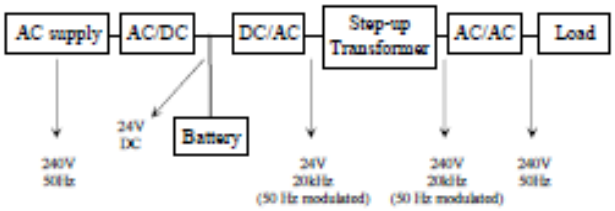

Fig. 5. Block diagram of the proposed HF UPS system

The 24V DC is achieved through the rectifier circuit where the AC is rectified and chopped to the desired low DC voltage. The DC/AC inverter is used to increase the frequency to 20 kHz – modulated at 50Hz. The 50Hz modulated component will not affect the transformer design as will be shown in the next paragraph. In ideal situation the transformer should operate at very high frequency in order to reduce the core cross section area. However, the winding size is not reduced or affected by the high frequency operation. Therefore a critical size of the transformer core is required to hold the transformer windings. A 20 kHz was the critical frequency at which the size of the transformer could not be reduced further. Fig. 6 shows a picture of the transformer used in such system.

Fig. 6. HF Transformer used in the proposed UPS system

The transformer core used is VITROPERM 500F. It has a number of advantages over ferrite cores which includes [3]:

- Smaller size (for the same power rating)
- More suitable for high currents and/or high voltages
- High efficiency, low power loss
- Suitable for high and low ambient temperatures and high operating temperatures.
- No operating noise.
- Best suited for winding of thick wires.

Fig. 7 shows the PSPICE simulated waveforms of the transformer and load voltages. The transformer switching frequency in this figure has been selected at 500 Hz for demonstration purpose in order to see the pattern in a clear way. It can be seen that although the transformer voltage is 500Hz, there are two 50Hz components going through the transformer in opposite way so that they cancel each other and only the 500Hz is the frequency seen by the transformer (not the 50Hz) as shown in the frequency spectra in Fig. 8.

CONCLUSIONS

In this paper, an on-line UPS circuit topology is proposed. The inverter circuit used in this UPS operates at higher frequency so that the size of the transformer can be reduced. This configuration could be attractive to small size office UPS units where the battery voltage needs to be kept at a safe low value (12 or 24V). The simulation results reveals that the transformer does not see the 50Hz component and this is mainly because the high frequency is modulated at two 50Hz anti-phase frequencies.

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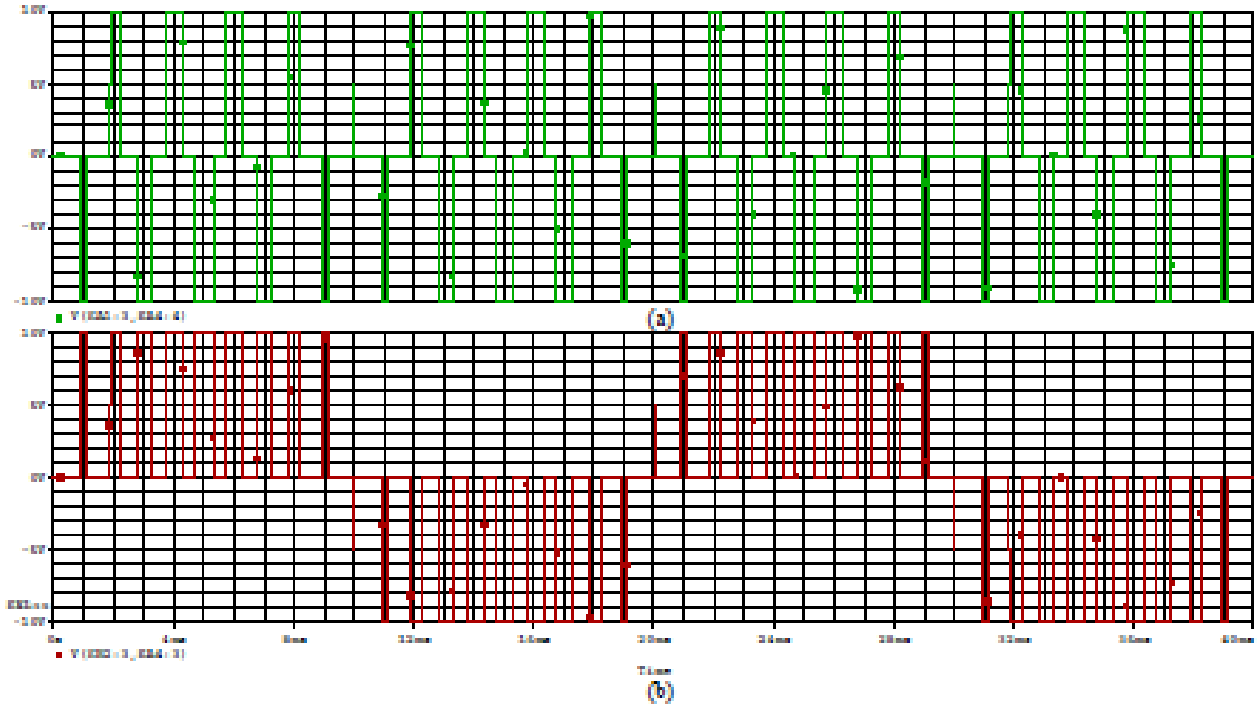
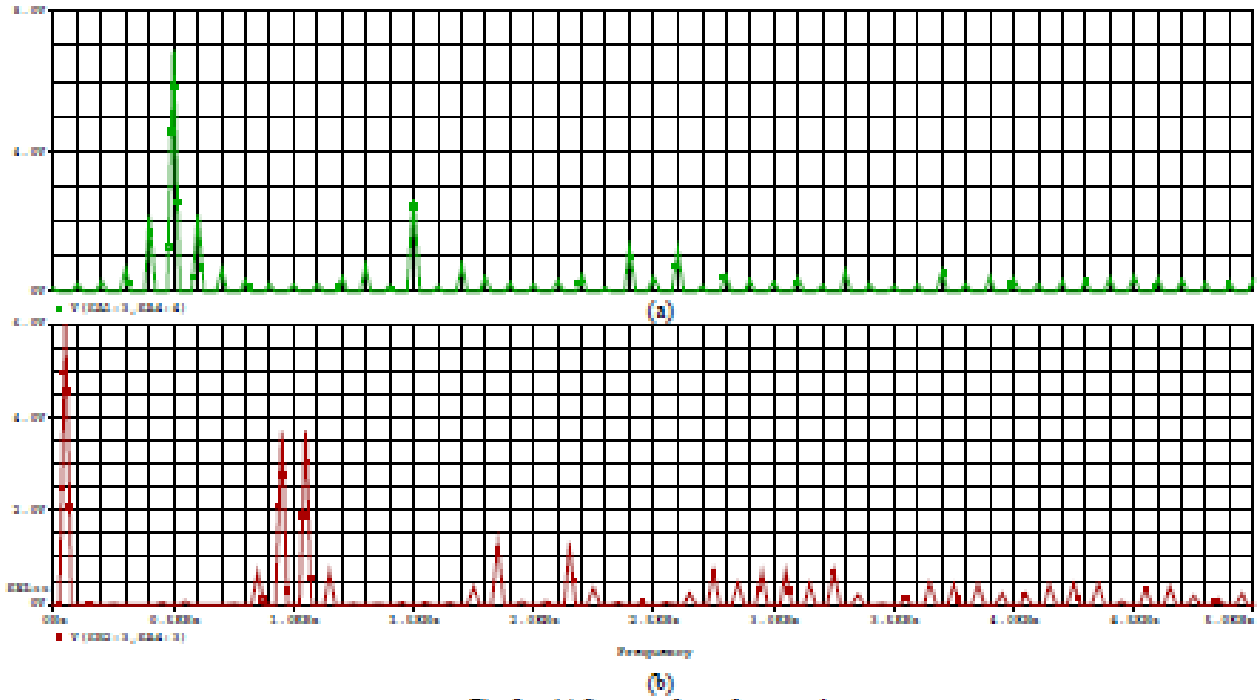


(a)

(b)

Fig. 7. (a) Transformer voltage
(b) Load voltage



(a)

(b)

Fig. 8. (a) Spectra of transformer voltage
(b) Spectra of the load voltage