THEORY AND MEASUREMENTS OF THYRISTORS WITH PARTICULAR REFERENCE TO LATERAL EFFECTS.

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To My Dearest Wife and My Parents.

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ABSTRACT

The characteristics and theories of four-layer pnpn semiconductor devices have been considered with particular reference to the two transistor analogy of thyristor in order to obtain an expression for the current-voltage characteristics of the device.

The small-signal, low-frequency current gains of the npn and pnp transistor sections of high and low power thyristors were measured by a three terminal method originally employed by W.Fülop. The technique is shown to be applicable to measurements on high power thyristors.

The current gains of two transistor component were also measured as a function of temperature at a series of anode currents. From this it can be shown that, the temperature dependance of two-terminal latching current can be qualitatively estimated from the plot of current gain measured at a series of temperature for constant anode current. Analysis of instability of devices with temperature showed that, the saturation current of isolated centre junction plays a dominant role. Gold doping predictably leads to low current gain of the pnp transistor section.

Current gain measurements of thyristors with and without shorting dot showed an almost similar variation with frequency. For both type of devices α_{npn0} was almost

equal and even closer at high temperature (100°C).

The theory of the influence of shorting dots on current flow in thyristors outlined in a report by W. Fulop, was developed. The value of I_L, hole lateral current in the p-base is found and its dependence upon p-base width and shorting dot area investigated.

The voltage distribution in the two central base regions just after the device has switched on but before the plasma has had time to spread is investigated. It was found that junctions J_1 and J_2 become reverse biased and share the bias reverse voltage. Calculations shows that for very large V_{OFF}, the voltages in these two junctions are equal.

In order to have a better understanding of thyristor behaviour, the set of one-dimensional non-linear partial differential equations describing the Poisson's equation and the two current continuity equations are solved numerically under steady-state conditions. The potential distribution and the hole and electron current density distribution within the device plotted one-dimensionally are given.

INTRODUCTION

1.1 Historical Notes.

In recent years, a number of semiconductor devices have been the subject of large-scale popular attention. A new type of engineer was required-one who could bridge the gap between electronics and conventional power engineering. It was the ease with which electronic control could be achieved with the thyristor that made manufacturers change more and more to designs using this device.

The silicon controlled rectifiers was developed from W. Shockley's idea of a "Hook" collector transistor following Shockley's idea, Ebers developed a two transistor circuit approximation for the p-n-p-n switch. Development of the p-n-p-n device moved very slowly for a time, until the first successful silicon four layer device was built in 1956 at Bell Telephone laboratories. Then an article by Moll et al (1956) established the foundations for the theory and design of devices of the SCR family.

In 1956 and 1957 the pnpn switch was not well understood and had been ignored as a practical device. In 1958 I.M. Mackintosh extended the theory to the proper three terminal (SCR) device. Since then it has made a spectactular progress. At present the greatest impact of the device is in the high

power field of applications. A good deal of the development effort is directed towards making devices of high power handling capacity.

The rapid and successive development of silicon controlled rectifiers in the ensuing years has added a new dimension and degree of freedom to the science of electric power conversion and control. Only in the past few years have the engineers in the electrical and electronics industries not to mention their colleagues in less directly involved technologies, begun to realize what tremendously powerful tools they now have at their disposal for fundamentally reshaping the way in which electrical energy is handled from generation to ultimate use. Because of their ability to handle large blocks of power at minimum cost per kilowatt, thyristors have no serious challengers in their control and conversion of static power.

1.2 The Device.

The silicon controlled rectifier is a four layer semiconductor device with either two or three electrical terminals. Its main fuction is the switching of electric current and it is notasymmetrical device. Under reverse bias the SCR blocks the flow of current, but in the forward direction it has two stable states. In the "ON" state the characteristic is similar to that of a diode rectifier (PIN Diode).

In the "OFF" state the characteristic is similar to that of the reverse bias. The device is switched from OFF to ON state by passing a small current pulse into the gate (three-terminal) or by exceeding the maximum blocking voltage (two-terminal) in the forward direction. To switch the device OFF the current through the device is reduced almost to zero to below the holding current to allow recovery or de-ionisation to take place.

A typical "Forward" V-I characteristic for a silicon p-n-p-n diode is shown in figure (1-1). In the forward direction, region P_1 is positive with respect to region N_2 figure (1-2), so that junctions J_1 and J_3 act as forward biased emitters and J_2 as a reverse biased collector.

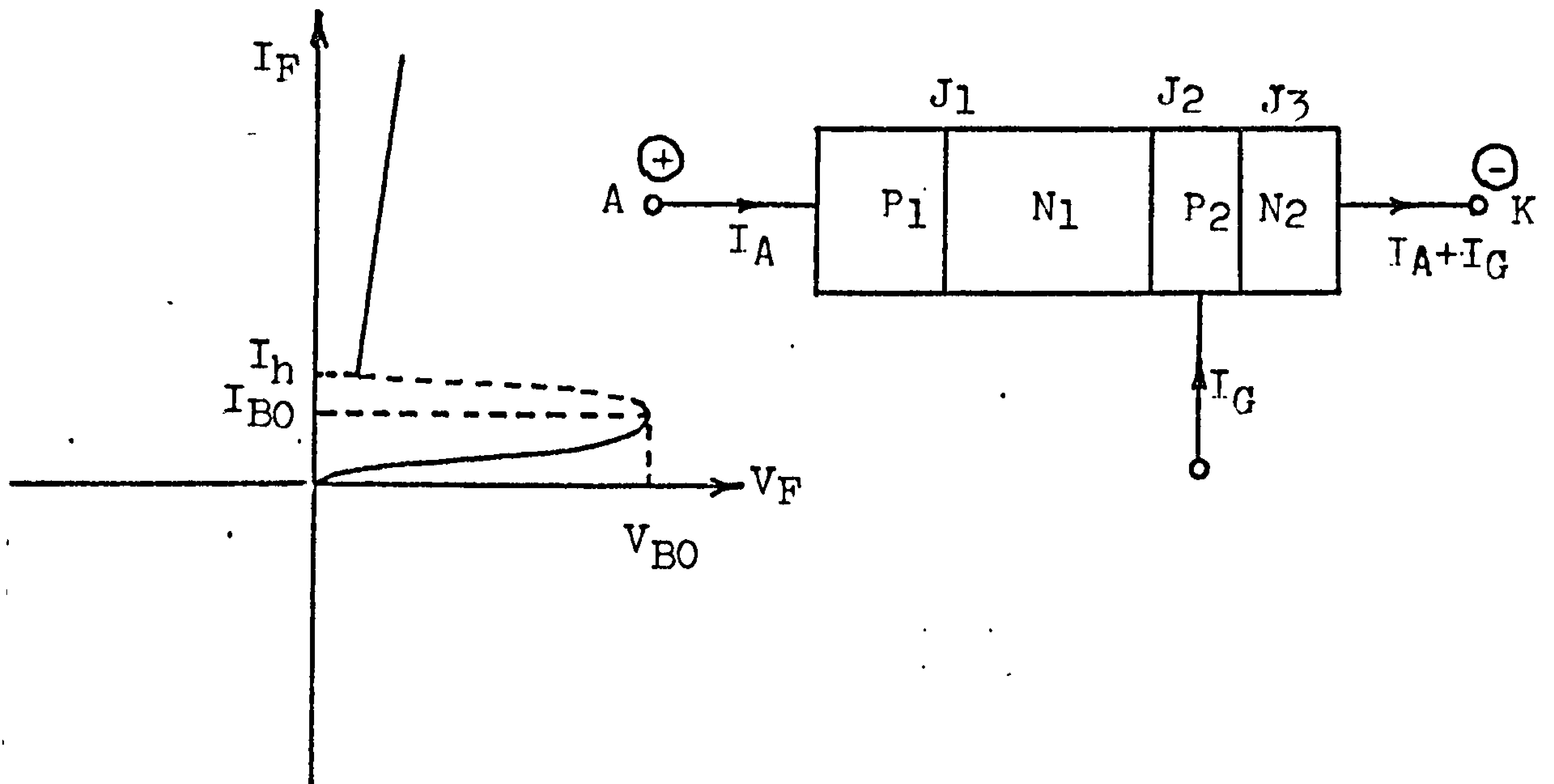


Figure (1-1) Forward I-V characteristic of pnpn.

Figure (1-2) pnpn under forward bias.

The four principal regions of the forward characteristic can be described as follows.

(1) OFF State.

In this case the reverse biased junction J_2, blocks the voltage and most of the current applied to the device. The characteristic is similar to that of a transistor without any base drive. The leakage current of J_2 is somewhat amplified by the two transistors but as the sum of α's is well below unity in this region the amplification is probably less than in a transistor.

(2) The Breakover Region.

Here the voltage across J_2 is so high that serious avalanche effects set in. Leakage current of J_2 is amplified by avalanche multiplication factors M_n and M_p for electrons and holes respectively. This increases the forward bias on J_1 and J_3 and further minority carriers arrive at J_2, and the junction J_2 breaks down. The breakover point is defined by dV/dI=0. At this point the voltage and current have values V_{BO} and I_{BO} respectively (in two terminal operation). The sum of αM products for the two transistors approaches unity.

<u>(3) Negative Resistance Region.</u>

The voltage across J_2 falls sharply with only slight increase of current. This means the M'S must be falling rapidly.

<u>(4) ON region</u>

When the sum of α's is unity the low impedance region starts. At this point the voltage across J_2 is zero. Junction J_2 receives such large minority carrier currents from J_1 and J_3 that it loses its reverse bias, goes through zero bias point and is positively biased in the ON region. When the sum of α's is greater than unity, the sum of the two

minority components reaching J_2 is greater than the total current through the device. Therefore J_2 must be at positive bias to re-inject some of the minority carriers back into the appropriate bases. Perhaps a more physical picture is that J_2 fails to collect all the minority carriers, there is a buildup of carriers at J_2 which produces a positive bias on the junction. In any case J_2 changes the polarity of its voltage when the device switches from "OFF" to "ON" state. The low-current limit of this "ON" region is designated the turn-off current I_t.

The device can be turned on without the assistance of the multiplication effect. This can be achieved by connecting a third terminal to deliver a current I_G to the base of device, figure (1-2). This base current can now increase the current gain α_{npn} of the n-p-n transistor section independently of V and I. In other words, α_{npn} is a function of $(I+I_G)$, α_{pnp} is a function of I only, and the value of sum of α's which controls the shape of the V-I characteristic can be modified by the flow of base current . Thus the increase in the current gains enables the switching condition to be reached at lower M_n and M_p values, i.e. at voltages well below V_{BO}.

2. The Theory of pnpn Devices.

2.1 General Theories.

The theory of four-layer pnpn semiconductor devices has been extensively analysed in two distinct ways.

The first method considers the device as an npn transistor superimposed on a pnp transistor and uses the general transistor parameters to obtain an expression for the V-I characteristics. This was introduced by Moll et al (1956) in order to consider the theory of two terminal pnpn devices. Then Mackintosh (1958) extended this to the three terminal (SCR) device.

A second approach analyses the flow of minority carriers in the device to obtain expressions for the V-I characteristic. This method was used by Jonscher (1957) to explain a pnpn diode and was extended to the SCR by Muss and Goldberg (1963). These theories have been developed in many other papers.

Muss and Goldberg pointed out that Jonscher's model is more accurate and less arbitrary. However, it leads to expressions for V-I characteristic which require a great deal of detailed knowledge about the carrier diffusion parameters in the various layers of the device for any calculation to be carried out. Thus the first approach gives more practical results.

W. Fulop (1963) proposed a method of analysis in which he measures the effective current gains (α) as a function of frequency. Underlying this method is the two transistor analogy of thyristor operation.

Crees and Hogarth (1963) also confirmed the theory independently by current gain measurements on four terminal SCR's.

J.F. Gibbons (1964) and Gentry et al (1964) in their investigations found a result very similar to Mackintosh's.

Mackintosh's paper was criticised by Kuzmin (1963) and also Gibbons (1964), because of neglect of the leakage current in his expression for the turn-off current. Jonscher (1960) also corrects for the recombination generation current term which has been neglected by Mackintosh in his calculation. Gentry et al (1964) take account of it by using exp qV/nkT to express forward current.

2.2 Transistor Analogue Theory.

Physical explanations for some of the more detailed behaviour of the pnpn analysis is required. The fundations have been laid by Moll et al and Mackintosh as mentioned in the previous section. Figure (2-1) shows schematically the structure to be considered.

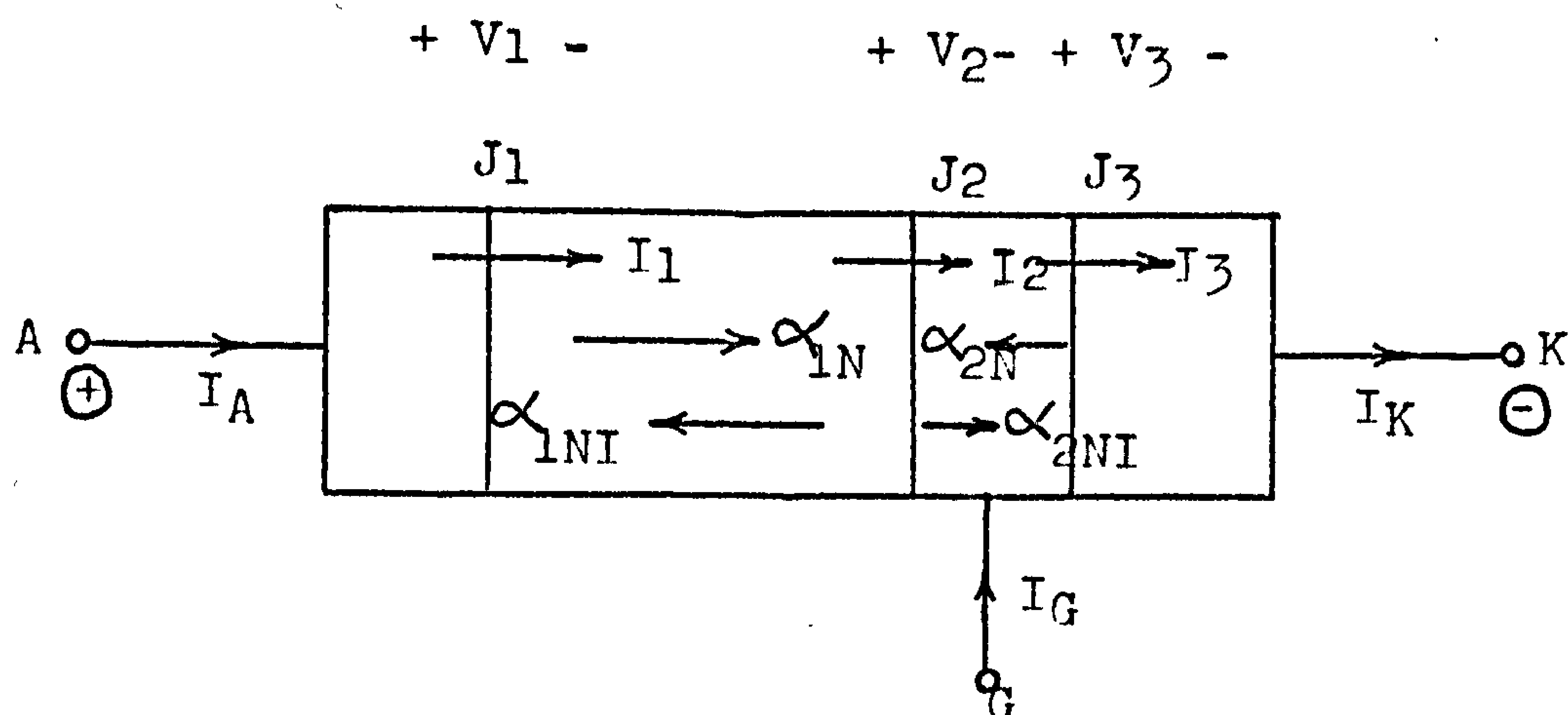


Figure (2-1) Schematical structure of PNPN

the voltage across the junctions J_1 , J_2 , J_3 are V_1, V_2, V_3 respectively, and taken as a positive from left to right. The saturation current of each junction, when the other two junctions are short-circuited are I_{S_1}, I_{S_2}, I_{S_3} respectively.

In general if a voltage V is applied to junction it will cause a current $I=I_S$ (exp qV /nkT) to flow through it, where n takes account of space charge recombination generation current. For reverse bias an extra voltage

dependent current I_0 (V) due to space charge generation will be added. The junction also collects minority currents in the form $\alpha I_S(\exp qV/nkT-1)$ where α is the appropriate current gain factor.

Under condition that anode is positive with respect to the cathode terminal, J_1 and J_3 are always forward biased and J_2 reverse biased. Thus the current through the junction J_1 is:

$$I_1=I_{S_1}\left[\exp(\beta V_1)-1\right]-\alpha_{1I}\, I_{S_2}\left[\exp-\beta V_2-1\right] \tag{1}$$

and the corresponding currents through the junctions J_2 and J_3 are

$$I_2=\alpha_{1N}\, M_p\, I_{S_1}\left[\exp\beta V_1-1\right]-(M_pI_{ps}+M_nI_{ns})\left[\exp-\beta V_2-1\right]+\alpha_{2N}\, M_n\, I_{S_3}\left[\exp\beta V_3-1\right]+I_0(V_2) \tag{2}$$

and

$$I_3=-\alpha_{2I}\, I_{S_2}\left[\exp-\beta V_2-1\right]+I_{S_3}\left[\exp\beta V_3-1\right] \tag{3}$$

where α_1 and α_2 refers to PNP and NPN transistor sections respectively and $\beta=\dfrac{q}{nkT}$.

To obtain the relationship between terminal current and voltage, the above equations are solved for the $\left[\exp \beta V-1\right]$ functions and give the following expressions:

$$I_{S_2}\ (\exp-\beta V_2-1) = \frac{I_2-\alpha_{1N}M_pI_1-\alpha_{2N}\ M_n\ I_3-I_0\ (V_2)}{M_p(\alpha_{1N}\alpha_{1I}-\gamma_2)+M_n(\alpha_{2N}\alpha_{2I}-1+\gamma_2)} \tag{4}$$

and

$$I_{S_1}(\exp\beta\ V_1\ -1)= \frac{I_1\left[M_n(\alpha_{2N}\alpha_{2I}+\gamma_2-1)-M_p\gamma_2\right]+\alpha_{1I}I_2-\alpha_{1N}\alpha_{2N}M_nI_3}{M_p(\alpha_{1N}\alpha_{1I}-\gamma_2\ )\ +\ M_n(\alpha_{2N}\alpha_{2I}-1+\gamma_2)}$$

$$\frac{-\alpha_{1I}I_0(V_2)}{(\ldots\ldots\ldots'')} \tag{5}$$

and

$$I_{S_3}\ (\exp\beta V_3-1)= \frac{I_3\left[M_p(\alpha_{1N}\alpha_{1I}-\gamma_2)+M_n(\gamma_2-1)\right]+\alpha_{2I}I_2\ -}{M_p(\alpha_{1N}\alpha_{1I}-\gamma_2)+\ M_n(\alpha_{2N}\alpha_{2I}-1+\gamma_2)}$$

$$\frac{-\alpha_{1N}\alpha_{2I}M_p\ I_1-\alpha_{2I}\ I_0(V_2)}{(\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots)} \tag{6}$$

where $\gamma_2 = \dfrac{I_{ps}}{I_{S_2}}$

These are the basic equations which will be used to consider V-I characteristic.

(a) OFF or High Impedance Region.

In this case with the device under forward bias, J_2 is reverse-biased and junctions J_1 and J_3 are forward biased. Since V_1 and V_3 are very small, with a good approximation, one can obtain the V-I characteristic in this region by considering V_2 as a function of I and I_G. With J_2 reverse biased the inverse α's are small, as there can not be any injection of minority carriers. Since

$$I_1 = I_2 = I_A \tag{7}$$

$$I_3 = I_A + I_G \tag{8}$$

substituting for I_1, I_2 and I_3 and putting inverse alpha terms to zero, equation (4) will reduce to

$$I_{S_2}(\exp-\beta V_2 - 1) = \frac{I_A(1-\alpha_{1N}M_p - \alpha_{2N}M_n) - \alpha_{2N}M_n I_G - I_0(V_2)}{-M_p\gamma_2 + M_n(\gamma_2 - 1)} \tag{9}$$

substituting for $\gamma_2 = \frac{I_{ps}}{I_{S2}}$ and solving for I_A

$$I_A = \frac{\alpha_{2N}M_n I_G - (M_p I_{ps} + M_n I_{ns})(e^{-\beta V_2} - 1) + I_0(V)}{1 - \alpha_{1N}M_p - \alpha_{2N}M_n} \tag{10}$$

Equation (10) gives the V-I characteristic in the OFF state since at voltages below avalanche effects $M_n = M_p = 1$ and $\exp-\beta V_2 = 0$ for several volts, then equation (10) reduces to:

$$I_A = \frac{I_{S_2} + \alpha_{2N}I_G + I_0(V_2)}{1 - \alpha_{1N} - \alpha_{2N}} \tag{11}$$

It should be noted that α_{1N} is a function of I_A and α_{2N} of $I_A + I_G$, and with $I_G = 0$, I_A will refer to two terminal operation. Thus I_G gives a method of controlling the values of α_{1N} and α_{2N} and with sufficiently high values of I_G, $\alpha_{1N} + \alpha_{2N}$ approaches unity and denominator vanishes, then device switches on.

(b) The Breakover region.

It has already been mentioned that pnpn switching can be initiated either by an increase in applied voltage or by an increase in the gate current drive. These two factors will be considered here.

Equation (10) will reduce to (12) since $\exp -\beta V_2 = 0$ in this region, thus

$$I_A = \frac{\alpha_{2N} M_n I_G + (M_p I_{ps} + M_n I_{ns}) + I_0(V_2)}{1 - \alpha_{1N} M_p - \alpha_{2N} M_n} \tag{12}$$

As the voltage V_2 increases, the multiplication factors start increasing and as a result I_A increases. The increased current causes an increase in the alpha's. Eventually $\alpha_{2N} M_n + \alpha_{1N} M_p = 1$ and denominator of equation (12) vanishes. Switching therefore occurs and the device can no longer sustain a high voltage. The exact break over point is defined by $\partial V_2 / \partial I = 0$.

Differentiating equation (12) with respect to I_A, assuming I_G constant and M's and $I_0(V_2)$ are functions of V_2 only we have:

$$\frac{\partial M}{\partial I} = \frac{\partial M}{\partial V} \cdot \frac{\partial V}{\partial I}$$

Thus after some manipulation and solving for $\frac{\partial V}{\partial I}$ one gets:

$$\frac{\partial V_2}{\partial I_A} = \frac{1-M_p(\alpha_{1N}+\frac{\partial\alpha_{1N}}{\partial I_A}I_A)-M_n\left[\alpha_{2N}+\frac{\partial\alpha_N}{\partial I_A}(I_A+I_G)\right]}{I_A(\alpha_{1N}\frac{\partial M_p}{\partial V_2}+M_p\frac{\partial\alpha_{1N}}{\partial V_2})+(I_A+I_G)(\alpha_{2N}\frac{\partial M_n}{\partial V_2}+M_n\frac{\partial\alpha_{2N}}{\partial V_2})}$$

$$+\frac{\partial I_{S2}}{\partial V_2}+\frac{\partial I_0(V_2)}{\partial V_2}$$

(13)

where

$$\frac{\partial I_{S2}}{\partial V_2} = I_{ps}\frac{\partial M_p}{\partial V_2}+I_{ns}\frac{\partial M_n}{\partial V_2}$$

Comparing this equation with Mackintosh's equation one can see that he assumed α's as a function of current only and has neglected the effect of space charge variation with voltage. This effect is large and alpha's should be considered as a function of current and voltage. However putting $\partial V_2/\partial I_A=0$ gives:

$$1-M_p(\alpha_{1N}+\frac{\partial\alpha_{1N}}{\partial I_A}I_A)-M_n\left[\alpha_{2N}+\frac{\partial\alpha_{2N}}{\partial I_K}I_K\right]=0 \quad (14)$$

The small signal low frequency current gain of PNP and NPN transistor sections is defined as (Gentry, 1964):

$$\alpha_{1N0}=\alpha_{1N}+\frac{\partial\alpha_{1N}}{\partial I_A}I_A$$

and

$$\alpha_{2N0}=\alpha_{2N}+I_K\frac{\partial\alpha_{2N}}{\partial I_K}=\alpha_{2N}+(I_A+I_G)\frac{\partial\alpha_{2N}}{\partial I_K}$$

since $\frac{\partial I_A}{\partial I_K}=1$ for I_G constant.

Therefore equation(14) can be written in the form of

$$1 = M_p \alpha_{1NO} + M_n \alpha_{2NO} \tag{15}$$

Equation (15) thus gives the coordinates (V_2, I_A) at which the centre junction has zero dynamic impedance. At this point, the device still has a positive dynamic impedance since $\partial V_1/\partial I_A$ and $\partial V_3/\partial I_A$ are positive. Hence, the actual switching point should theoretically occur at a current greater than that given in (15) so that the dynamic impedance of the centre junction can become sufficiently negative to cancel the outer junction impedance. However, (15) is sufficiently accurate with good approximation for the study of switching condition.

With I_G=0 the breakover point is reached by increasing the voltage across the device until avalanche effects set in. But with $I_G > 0$ the value of M's required to satisfy (15) is near unity, hence the device will be switched on well below avalanche level of voltage. Therefore the effect of gate current is to reduce the voltage of the breakover point.

Assuming M_p=M_n=M and substituting the value of M in (15) the breakover voltage will be:

$$M = \frac{1}{1-(V_{BO}/V_B)^n}$$

$$\frac{V_{BO}}{V_B} = (1-\alpha_{1NO} - \alpha_{2NO})^{1/n} \qquad (16)$$

where V_B is the breakdown voltage of isolated centre junction, and for abrupt junction is defined by (Sze,1969):

$$V_B = 60\ (Eg/1.1)^{3/2} (N_B/10^{16})^{-3/4} \text{ volts}$$

$$\simeq K.N_B^{-3/4} \qquad (17)$$

where $K = 60\ (Eg/1.1)^{3/2} \times 10^{12}$, Eg is the bandgap and N_B is the background doping.

The depletion layer width of centre junction with device in forward bias is given by

$$W_{sc} \doteq \left(\frac{2K\varepsilon_o V}{qN_B} \right)^{1/2} = K' \left(\frac{V}{N_B} \right)^{1/2} \qquad (18)$$

where V is the applied voltage and $K' = \left(\frac{2K\varepsilon_o}{q} \right)^{1/2}$. Substituting the equation (17) into (18) and assuming that the device is operating at sôme fraction (F) of the avalanche voltage then, the depletion layer width at high voltage (breakover voltage) becomes:

$$W_{sc} = K\ (FK')^{-2/3}\ V_{BO}^{7/6} \qquad (19)$$

thus, increasing the voltage will expand the depletion layer which will reduce the base width and hence increase the alpha's to cause switching to occur. As the barrier

layer spreads through the base region to the opposite junction, punch through effect results. Thus wider base width is required in order to prevent the effective base width from becoming zero.

(c) Negative Resistance Region.

At this region $M_n\alpha_{2NO} + M_p\alpha_{1NO} > 1$ and voltage across the device starts falling and eventually $M_p = M_n = 1$. At the voltage very near $V_2 = 0$ the neglected $[\exp-(\beta V_2)-1]$ term is not negligible. Thus putting $\frac{\partial M}{\partial V} = 0$ in equation (10) and taking exponential term into account gives:

$$\frac{\partial V}{\partial I} = \frac{1-\alpha_{1NO}-\alpha_{2NO}}{\beta_2 I_{S2} e^{-\beta V_2} + \frac{\partial I_0(V_2)}{\partial V_2}} \tag{20}$$

This is negative impedance expression near $V_2=0$ point, since $\frac{\partial \alpha}{\partial V_2} \longrightarrow 0$

(d) The Forward Switched Condition.

In the ON state $M_n=M_p=1$ and $I_0(V_2) = 0$. The main interest here is the total voltage drop across the device. The effect of gate current is very small except near the turn off point thus it can be neglected. Rearranging equations 4,5,6 and putting $I_1=I_2=I_3=I_A$, $M_n=M_p=1$, one gets:

$$V_1 = \beta' \ln\left(\frac{A_1 I}{I_{S1}} + 1\right) \tag{21}$$

$$V_2 = -\beta' \ln\left(\frac{A_2 I}{IS_2} + 1\right) \tag{22}$$

$$V_3 = \beta' \ln\left(\frac{A_3 I}{IS_3} + 1\right) \tag{23}$$

where $\beta' = \frac{nkT}{q}$ and:

$$A_1 = \frac{1-\alpha_{2N}\alpha_{2I}+\alpha_{2N}\alpha_{1I}-\alpha_{1I}}{1-\alpha_{1N}\alpha_{1I}-\alpha_{2N}\alpha_{2I}}$$

$$A_2 = \frac{\alpha_{1N}+\alpha_{2N}-1}{1-\alpha_{1N}\alpha_{1I}-\alpha_{2N}\alpha_{2I}}$$

$$A_3 = \frac{1-\alpha_{1N}\alpha_{1I}+\alpha_{1N}\alpha_{2I}-\alpha_{2I}}{1-\alpha_{1N}\alpha_{1I}-\alpha_{2N}\alpha_{2I}}$$

In the ON state $\frac{AI}{I_S} \gg 1$, in addition if $\frac{A_2 I}{IS_2} > 0$, in order to satisfy equation (22) V_2 should be negative. This means that V_2 must be forward-biased when the device is in the conducting state. However, the total voltage drop across the device can be written

$$V_T = V_1 + V_2 + V_3 + V' = \beta'\left[\ln\frac{A_1 A_3}{A_2} + \ln\frac{IIS_3}{IS_1 IS_3}\right] + V' \tag{24}$$

where V' is the voltage drop through the wide base high resistivity region.

Conductivity modulation in N_1 occurs as soon as the density of injected carriers (holes) becomes comparable with the original doping of N_1. This can take place in the OFF state at values of current lower than the switching current. The same conductivity modulation is responsible

for the low voltage which is mentioned in the "ON" state.

The conductivity modulation description in the base N_1 is closely related to that of a PIN conductivity-modulated diode. The equivalence is complete when α_{2N} is close to unity since then the current at the junction J_2 is entirely electron current, and at junction J_1 entirely hole current. The voltage drop through the N base is then, (Hoerni and Noyce, 1958)

$$V' = 4(kT/q)\,(\tan^{-1} e^{W_N/L_P} - \frac{\pi}{4})\ \sinh\ (W_N/L_P)$$
$$= \tfrac{1}{2}\,(kT/q)\, e^{W_N/L_P} \qquad (\text{for } W/L \gg 1)$$

(25)

where L_P is the high level diffusion length for holes. V' increase with W/L, and reaches 1 volt for W/L = 4.4. Aside from any high speed behaviour consideration, this factor eventually limits the tolerable thickness of the switch. The voltage drops through the layer P_1, P_2, N_2 are negligible since these are highly doped.

Another importance feature in this region is the holding current. That is the point at which the forward V-I characteristic has its minimum value. In order to obtain the coordinates of the holding point, consider the current I_t at which the centre junction goes from reverse bias to forward bias, i.e. the current at which V_2=0 . Mackintosh calls it a turn-off current. Since I_0 (V) =0 and M_n =M_p=1, equation (4) reduces to :

$$I_{S2}(e^{-\beta V_2}-1) = \frac{I_A(1-\alpha_{1N}-\alpha_{2N}) - \alpha_{2N}I_G}{\alpha_{1N}\alpha_{1I}+\alpha_{2N}\alpha_{2I}-1}$$

therefore for $V_2=0$ and $I_A=I_t$ we have:

$$1=\alpha_{1N}+\alpha_{2N}+ \frac{\alpha_{2N}I_G}{I_t} \qquad (26)$$

In a pnpn diode $I_G=0$ so,

$$\alpha_{1N}+\alpha_{2N} = 1 \qquad (27)$$

but in a pnpn triode, $I_G > 0$ therefore $\alpha_{1N}+\alpha_{2N} < 1$ when $V_2=0$. The current at which $\alpha_{1N}+\alpha_{2N} = 1$ is then a point in the ON region, where the centre junction is forward biased and previous analysis does not apply; the reverse is true for negative I_G. However the condition $V_2=0$ does not give the current at which dV/dt has its low voltage zero. That is dV/dt=0 point in the low impedance region. This corresponds to the minimum voltage point on the V-I characteristic in the ON-state. Gibbons(1964) by setting an idealized model showed that,

$$I_h = 2.5I_t$$

for a two terminal device

W. Fulop (1966) analysed the holding point by means of zero bias at centre junction $V_2= 0$ and voltage minimum

point (VM), that is dV/dt = 0. He pointed out that for the direction of decreasing current and approaching V_{BO}, the precise location of the holding point is circuit dependent and will occur where the circuit resistance approaches to the numerically increasing negative resistance of the device. He also showed, that the VM point lies above in current compared to the zero centre voltage point for a given curve parametric in I_G and this appears to hold for positive, zero and negative gate current I_G and agrees with Gibbons' result.

(e) High Injection Level.

A. Herlet and K. Raithel (1966) pointed out that the forward characteristics of thyristor and PIN diode under the condition of high level injection in both base regions are completely identical if the width of swamped regions is equal. The argument was that at high current the n- and p base regions of the thyristor are so heavily con- -ductivity modulated by the injected carriers that the junction J_2 vanishes as far as carrier concentration is concerned. This is true for current above 10 amps. For current below 10 amps, the argument was that the injected carriers density is insufficient to swamp the p-base and hence V_T, the total drop for SCR deviates from the diode.

They also showed that, the doping concentration in the n base region has no influence upon this identity and

the quantitative behaviour of the forward characteristic. This is perhaps because the high level lifetimes of injected carriers are independent of conductivity and doping concentration up to 1.5 $x10^{17}$ cm^{-3} in the p-base.

R.A. Kokosa (1967) independently proved the similarity of characteristics of SCR's and PIN diodes. He used an abrupt junction model, which included effect of carrier-carrier scattering and emitter efficiency variation with current density to calculate the potential and carrier distribution of a pnpn diode in the base regions. He also measured these two factors by electrical and optical probing techniques, and found good agreement between the calculated and measured results. However the conclusion is that the SCR above a current density of 1 to 10 amps $/cm^2$ can be treated as a PIN diode.

2.3 The Device Switching Action.

2.3.1 Turn-On

The time taken for the transition of thyristor from the non-conducting state to conducting state is known as a turn-on time. This time has been divided into three different regions, the delay time t_d , the rise time t_r and the conduction spreading time to t_s. These times are illustrated in figure (2-2)

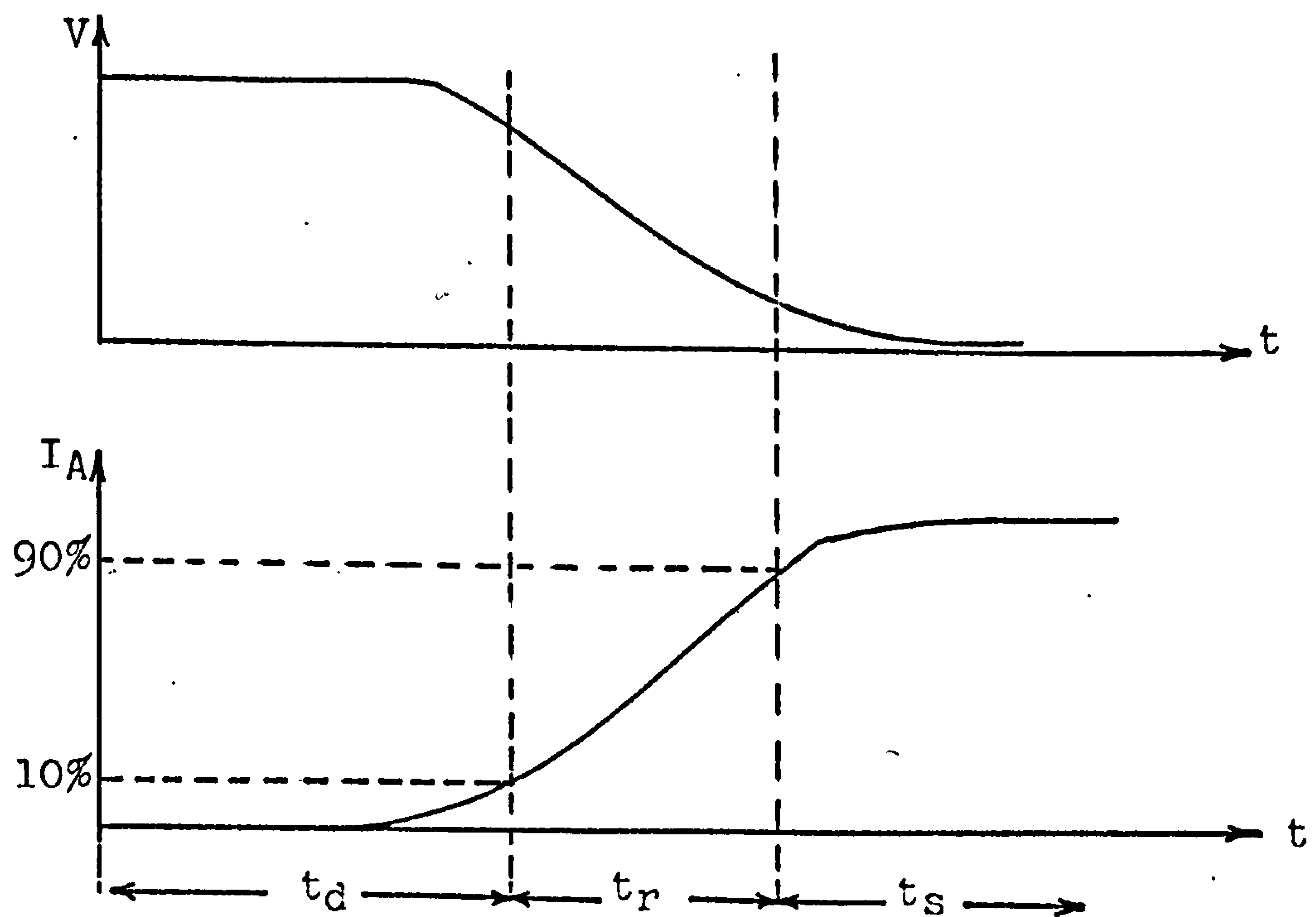


Figure (2-2) Delay and rise time during turn-on process.

At the instant when a gate-to-cathode current is initiated there is no appreciable change either in anode to cathode voltage, or in anode to cathode current. After a short time the anode current I_A starts to increase and at the same time voltage across the device falls. The rise time t_r, is thetime taken for the anode current to

increase from 10 to 90 percent of I_A. The anode voltage then continues to fall slowly, and the anode current to rise, until a steady state value is reached after t_s.

The delay time is the time during which charge is being established in the device sufficient in magnitude to support a current greater than the holding current of the device. Once this charge has been established a loop gain of greater than one prevails and the device turns itself on. The rise time is the time during which this takes place.

There are several time constants contributing to the delay time. Due to gate current flow the junction injects electrons into base(P_2), and they begin diffusing towards J_2. It takes some time for these electrons to move across base layer P_2. This time is very short and given by:

$$t_2 = \frac{W^2_{B2}}{2D_n} \qquad (28)$$

These electrons will be collected by junction J_2. In order to maintain charge ne trality, every collected electron must be compensated by a hole injected across J_1. Again another time is required for holes to pass the base region so:

$$t_1 = \frac{W^2_{B1}}{2D_p} \qquad (29)$$

When they arrive and are swept by J_2 into P_2, the holes cause

a further increase in injected electrons by J_3. This process continues until the current reaches its steady state load current level.

R. Davies, takes the lifetime of the carriers into account and shows a more accurate expression for base transit time which is

$$t_t = \frac{4W^2}{\pi^2 D(1+\frac{4W^2\tau}{\pi^2 D})} \tag{30}$$

where D is the diffusion constant.

Another contribution is the time taken to charge the junction capacitance C_3 of junction J_3. This is given by:

$$t_3 = \int_0^{V_G} \frac{C_3(V)\, dV}{I_G} \tag{31}$$

where C_3 (V) is the gate-to cathode capacitance, and is a function of gate-to-cathode voltage V. Thus the delay time can be the sum of three transit times which is taken to conclude at 10% of the anode current,

$$t_d = t_1+t_2+t_3$$

The rise time depends on the geometric mean of the transit times of both of the transistors and is equal to (Bergman, 1965),

$$t_r = 2\left[\frac{t_1\ t_2}{\alpha_{1N}+\alpha_{2N}-1}\right]^{1/2} \tag{32}$$

After the rapid rise time a small area near the vicinity of the gate is turned on, causing the current I_A to flow. The area of conduction spreads simply by lateral diffusion of minority carriers from the turned on region where their density is high into the non conducting regions during the spreading time t_s, until the whole cathode area of the thyristor is conducting. This conduction spreading is associated with a drop in the anode-to-cathode voltage of the device as the current density decreases.

Different approaches were used for the calculation of the spreading velocity. Longini and Melngailis (1963) for a rectangular bar shaped thyristor, showed that:

$$V_S = \frac{F}{N_0} - \frac{N_0}{F}\left(\frac{D}{\tau} + \frac{\pi^2 D^2}{a^2}\right) \tag{33}$$

where $2F/\pi$ is the flux of carriers that is fed to the OFF region perunit thickness per unit length of periphery of the ON region.

a   is the thickness of each base

D   is the diffusion constant of minority carriers

τ is lifetime of minority carriers.

In another paper, Dodson and Longini (1966) put equation (33) in the form

$$V_S = G_1 I/S - G_2 S/I \qquad (34)$$

where G_1 and G_2 are independent of current, but G_2 involves the temperature dependent parameters, and S is the peripheral length of the on region. At higher load currents, the first term of (34) dominates and velocity will be pro--portional to the load current. They showed experimentally that the measured velocity increases with load current, but the proportionality is not a direct one except for a small range of low currents. And at high currents the following relationship holds approximately,

$$V_S \propto I^{1/n} \qquad (35)$$

where n usually lies between 2 and 6.

Bergman (1965) obtained the equation

$$V_S = 1.48 \left(\frac{D}{t_r}\right)^{1/2} \qquad (36)$$

where D is the diffusion constant and t_r is the rise time at the relatively low anode-cathode voltage, which occurs across the thyristor during the spreading process.

Ruhl (1970) pays more attention to this, and assumes that the spreading velocity is a linear function of the lateral hole current. He also assumes that the lateral field in the transition region is a constant and this shows that the spreading velocity is given by:

$$V_S = \frac{AMkT}{q} \ln\left(\frac{J_e}{J_0} + K\right) + C \tag{37}$$

where J_e is the active area emitter current density, at the edge of active region.

A   is an unspecified function independent of J_e and temperature.

C   is a device constant independent of J_e and K and has a value usually near 1.

2.3.2 dV/dt problem and the shorted emitter.

By applying a rapidly rising positive voltage to the thyristor, it can be made to turn-on if the rate of rise and magnitude of the anode voltage are sufficiently large. This phenomenon can cause undesired switching of the device.

When the device is in the blocking state a rapidly rising voltage applied to the anode lead will cause current to flow throughjunctions J_1 and J_3 and collector junction capacitance C_2. Since the alpha's increase with emitter current, the current which flows as a result of a rapid change in voltage may cause the alpha sum to become unity; switching then occurs. For rating and application purposes, the dV/dt capability of a device is defined as the maximum rate of rise of forward voltage that the device will support without triggering, at a specified percentage of the rated blocking voltage.

Depletion of junction J_2 due to the flow of holes to

the cathode and electrons to the anode creates a displacement current which is equal to:

$$I_{D1S} = C_2 \frac{dV}{dt} + V \frac{dC_2}{dt} \tag{38}$$

The second term is very small in comparison to the first term and can be neglected. Its effect is to make the current fall slightly with time, because as the depletion layer spreads C_2 decreases. However (38) can be simplified to

$$I_{D1S} = C_2 \frac{dV}{dt} \tag{39}$$

thus the dV/dt capability of device is influenced by the capacitance of the centre junction.

The dV/dt performance depends on geometry (such as effective base widths) and mostly on the lifetime of the minority carriers. That means lowering minority carrier lifetime will reduce emitter efficiency and transport factor, which needs more displacement current to trigger the device.

The performance with respect to dV/dt can be improved by negatively biasing the gate, as then the displacement current can partly flow straight from the p-base and across the gate, bypassing the n emitter, and thus not

releasing electrons from the n-emitter. Junction J_3 is then not biased in the forward direction owing to the negative voltage from the gate applied to the p-base. Not until the desired moment of triggering is the gate briefly positive.

The stability of the device in respect of dV/dt also falls off rapidly with temperature, figure (2-3), because the current gain factors increases with temperature and reach the critical value of unity at quite small currents.

Another possibility of improving dV/dt performance is by careful control of the impurity concentration between emitter and base. This will control the emitter efficiency of the device, hence the current gain.

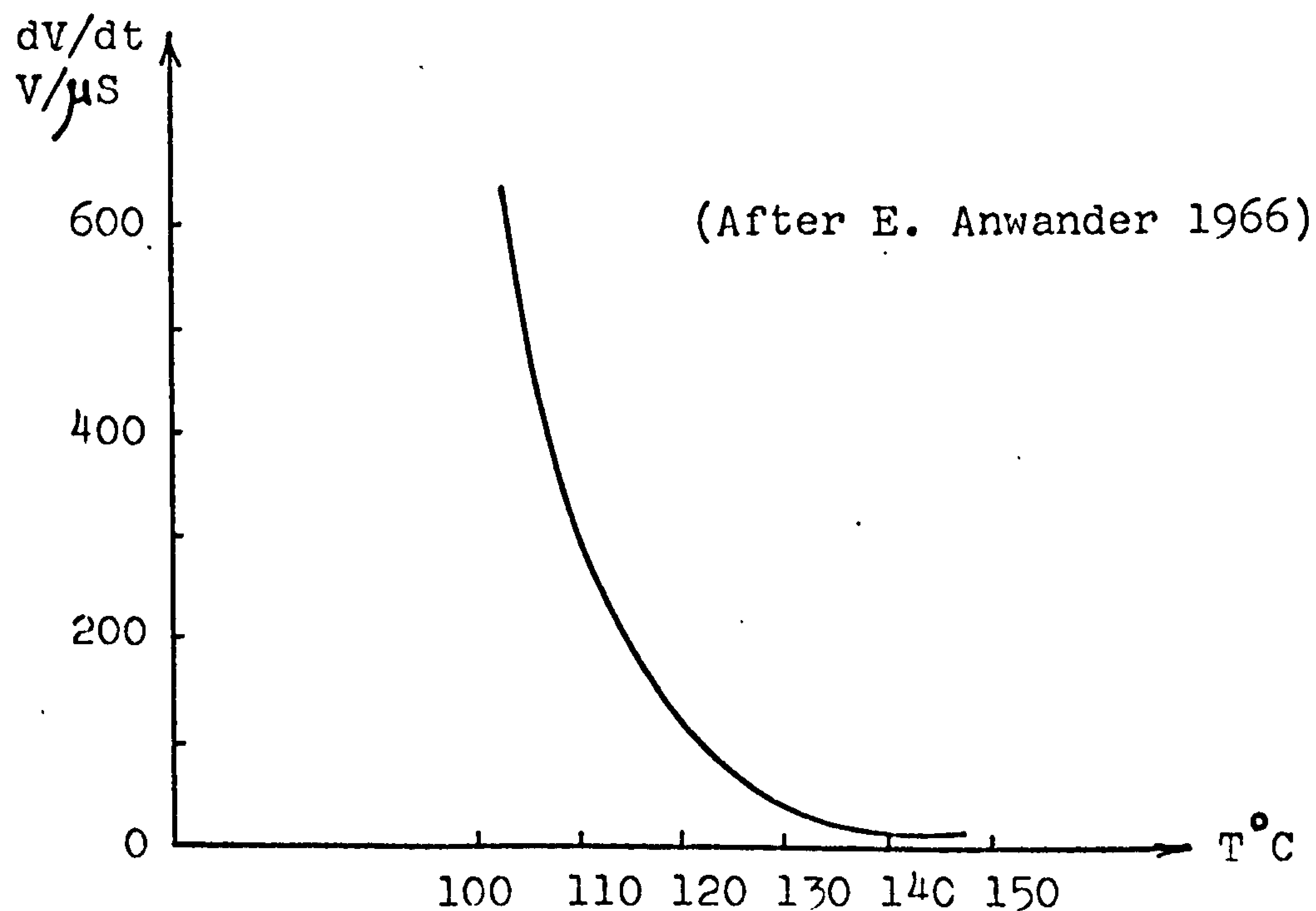


Figure (2-3) The rate of voltage rise in relation to temperature for device without shorted emitter.

Emitter efficiency can be controlled structurally by introducing shorting resistance between the underlying base region and the emitter, figure (2-4)

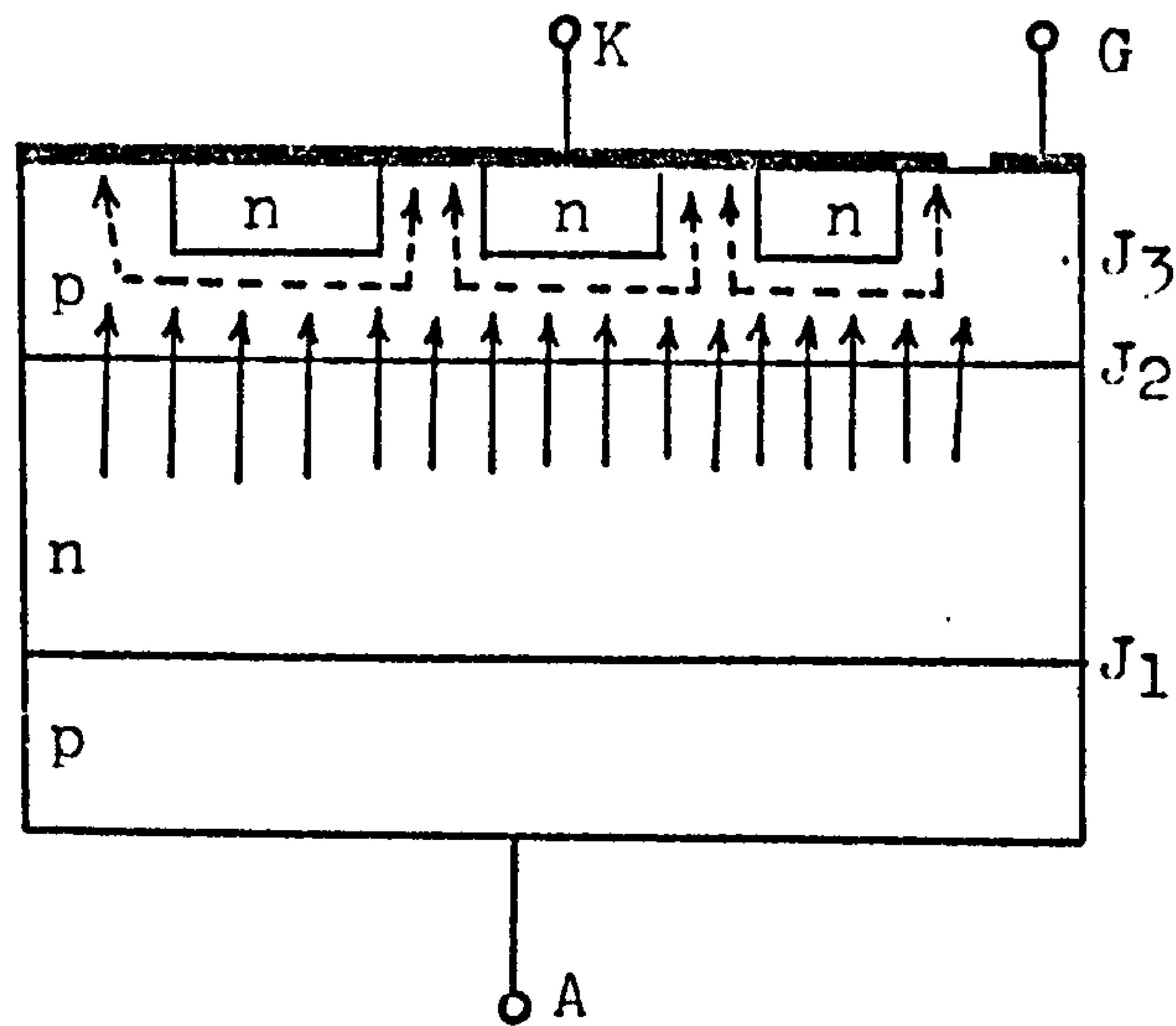


Figure (2-4) pnpn with shorted emitter

The primary function of "shorted emitter" is to reduce the n-emitter efficiency at low current levels. In this way the shorts serve to increase the high temperature forward blocking voltage capability of the device and also to improve the dV/dt rating. They also provide a path for the removal of stored charge from the p-base and increasing the holding current of the device, thereby reducing the time required to turn the device off.

However with the anode biased positively, the hole current collected at J_2 will flow laterally beneath the emitter junction until the voltage drop reaches a sufficient level (V_0) to cause J_3 to emit electrons into the base region. Thus, we have an emitter which has essentially a zero emitter efficiency at very low currents, but as the current

through the structure increases, the emitter efficiency increases. The variation of emitter efficiency with current can be easily controlled by adjustment of the base sheet resistivity and the spacing between shorted regions.

Aldrich and Holonyak (1959) used metallic contact forming a short circuit between the emitter and adjacent base region of the pnpn device and showed that, by varing the shorted area it is possible to fabricate the device with turn-on currents less or greater than the hold current.

They also showed that the holding current I_h changes only a little over an extensive temperature range, whereas the turn-on current I_{BO} changes appreciably with increasing temperature. Also the breakover voltage remains relatively constant, because of the small temperature coefficient of avalanche breakdown.

C.K. Chu (1970) experimentally showed that the dV/dt performance not only depends on the shorted area but also on the shorting pattern. By increasing the shorted area, the distance between the shunts will be decreased and actual dV/dt will be increased. He eliminated one row of shunts around the gate, and observed that the dV/dt performance was lowered and turn-on time decreased, but on the other hand the loop effect could be minimized in the forward V-I characteristic.

Raderecht (1971) approach was graphical and he showed that, the degree of improvement depends directly on the number and spacing of the shorting dots. A small number of dots (i.e.6) appeared to have no significant effect on the dV/dt capability or voltage performance of the device, but as the number of dots was increased the dV/dt performance gradually improved and the forward blocking voltage rapidly increased to maximum and then a slight difference was observed in voltage performance as the number of dots was increased further. The interesting result was that, a large number of small shorts was more effective than few a large shorts. The table below shows some of the results.

No. of dots	Approx. spacing of dots (thou)	Average V_{BO} (volts)		Ave. gate firing chara. mA V I_{GF}/V_{GF}	Ave. dV/dt at 640 V & 125°C V/µS
		21° C	125° C		
6	175	910	860	64/1.4	23
12	125	1050	975	83/1.6	42
24	93	1060	1005	93/1.6	49
30	78	1040	1020	84/1.6	101
75	46	1060	980	110/1.6	>200

(After Raderecht, 1971). The size of dots were 0.027"

2.3.3 di/dt problem.

As mentioned previously the gate triggered thyristor

does not turn on over its entire area immediately after the application of the trigger signal. Conduction is at first confined to a small area under the cathode which is physically close to the gate electrode. The conducting state then diffuses radially outwards with time from this initiated point.

At the initial stage, if the power dissipated during the early turn-on process is high and the initial conducting area small, a large amount of energy will be dissipated in the initial region. This causes rapid localized heating and can result in the destruction of the device by excessive temperature or thermal shock. A thyristor's ability to switch into fast-rising currents without damage is termed "di/dt" capability.

The energy dissipated per unit volume in the initiated region during early conducting period is defind by (Cordingley, 1971)

$$E = \frac{\int_{0}^{t_1} \frac{P(t)A_0}{A(t)}\,dt}{A_0 \cdot d} \qquad (40)$$

where A(t) is the instantaneous conducting area, A(t) = A_0 at t=0.

A_0 is the initial conducting area.

d is the thickness of silicon slice.

E is the energy supplied per unit volume to the initiated point after t_1 seconds ($t_1 < 20\,\mu S$)

P(t) is the instantaneous power dissipated in the silicon slice, and is a function of the SCR's rise time.

A demand for power devices to be capable of turning on into fast-rising high-current waveforms with low transient-energy dissipation and without damage, persuaded investigators to work more closely at the problems involved. However in order to improve di/dt capability, Somos and Piccone (1967) experimentally showed that decreasing the initial thermal resistance from the conducting area to the heat sink and decreasing the current density will increase the initial conducting area of the device which improves its di/dt rating.

High voltage thyristors have inherently lower di/dt capability, their crossover point [a point at which at given current density, the heat generated in the cell decreases with increasing temperature and above this current density the generated heat increases with temperature] is lower, and for a given current density they have a higher conducting voltage drop. Hence for high voltage designs, to obtain a di/dt capability comparable with low voltage designs, the initial conducting area must be increased. This can be achieved by alteration to the device's physical geometry and increased gate drive.

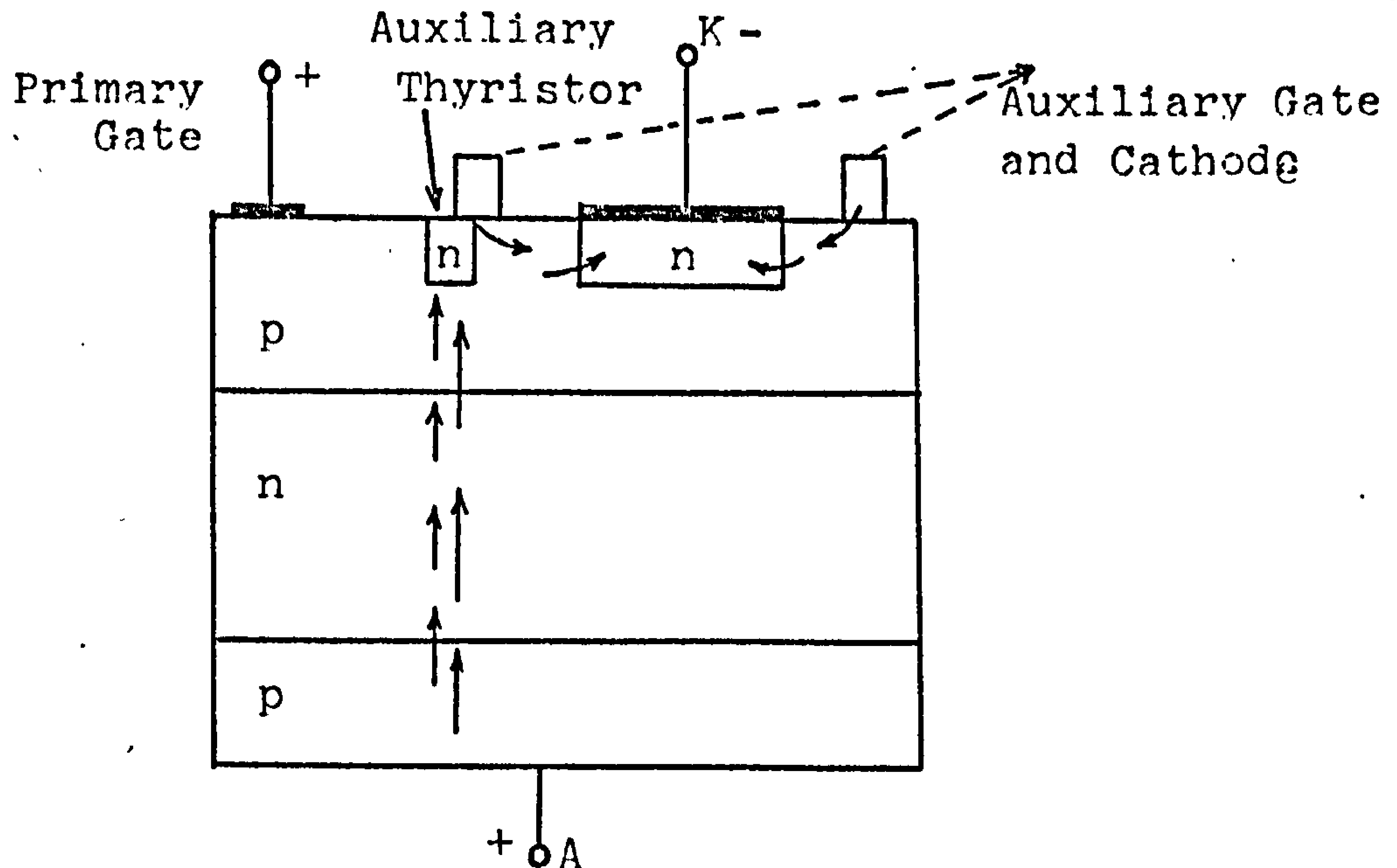
A circuit solution to overcome di/dt (Maphan 1962) was the use of saturable reactors in series with the device;

this limits the current after turn on. During the delay period the turned-on area has time to increase so that the current density is reasonably low when the bulk current flows. The problem withasaturable reactor is that if the current density is low during the reactor's delay period, the conducting region will not spread and all the current will still flow through one small area. Therefore, the designer of such a circuit must consider the current during the reactor delay period and the delay characteristics of the reactor.

To solve the di/dt problem rather than circumvent it, manufacturers have tried a variety of gating configurations other than the simple side-fire gate. The centre-gate, ring-gate and multiple-gate structures are theoretically supposed to reach full area conduction about twice as quickly as a side-fired device, but they have not increased di/dt ratings appreciably. In these devices, just as in the side-fired gate, more current is carried at the initiating point than elsewhere, and local burn out is a problem. However multiple -gate and ring-gate structures require a large gate signal, or "Hard firing". Ring-gate thyristors because of their long-gate cathode perimeter for a constant emitter depth, suffered from reduced gate sensitivity. In order to overcome this problem devices have been developed that incorporate a gate amplification facility.

Figure (2-5) illustrates the structure of the amplifying

gate thyristor. When the device is in the forward blocking



Figure(2-5) Amplifying gate thyristor.

state, the cathode of auxiliary thyristor is at the same potential as the main cathode, and negative with respect to the anode. Upon applying a positive voltage to the primary gate, the auxiliary thyristor is switched on, and the anode current starts to flow in the direction as in indicated by the arrows figure (2-5). This lateral flow of anode current in the p-region acts as a very large gate drive for the main thyristor. Eventually the main thyristor is switched on, and the auxiliary thyristor is switched off.

Cordingley (1971) showed that such a structure has low switching loses and good di/dt capability with high gate sensitivity at low values of gate drive. At high values of gate current the amplifying structure has poorer switching characteristic than a ring gate structure. This

is probably because the area over which the auxiliary thyristor can dissipate the early switching energy is small, where as with the large ring-gate structure the whole of the switching energy can be dissipated over a much larger area and hence volume.

The amplifying gate structure as well as the ring-gate devic have the disadvantage that during the steady-state conducting period the position of silicon used for the gating mechanism is inactive. In this case at low frequencies and suitable switching condition, the short gate device is to be preferred, since it provides a larger effective area for steady state condition.

The inverse gate thyristor has been developed to eliminate the high gate drive failure. Figure (2-6) shows the structure of such a device.

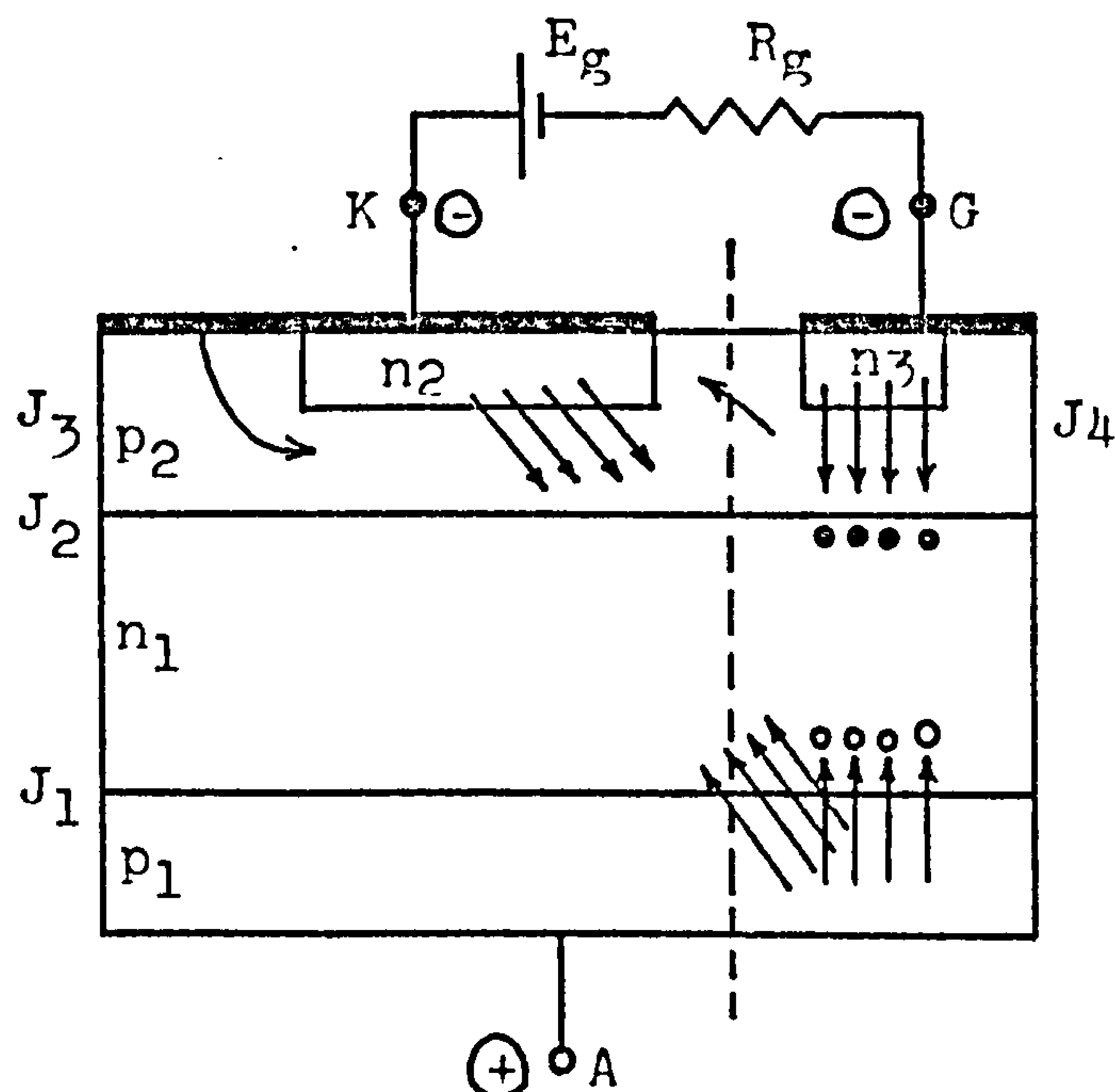


Figure (2-6) Inverse gate thyristor.

Upon applying a negative voltage to the n_3 region, an ohmic current will flow from the gate pulse generator through the ohmic short common with the main cathode, across the p_2 region and back across the J_4 junction. This causes electrons to be injected from the n_3 into the p_2 region building up the concentration of carriers under the junction in the p_2 region. This difference in carrier concentration through the p_2 region enables a current of diffusing carriers to cross the p_2 region to be collected at the J_2 junction immediately beneath the n_3 region. Switching then occurs in this region. Before this point the J_3 junction is reverse biased. Once switching takes place at the J_2 junction in the vicinity of the n_3 region. A large current typically 20 to 30 amps. is available to switch on the main cathode. Thus a heavy current drive to the main cathode has been generated so that the large di/dt (1000 A/μS) can be absorbed by the main cathode.

Gray (1968) developed another gate structure device to improved di/dt capability. This device is called a regenerative gate structure which is shown in figure(2-7)

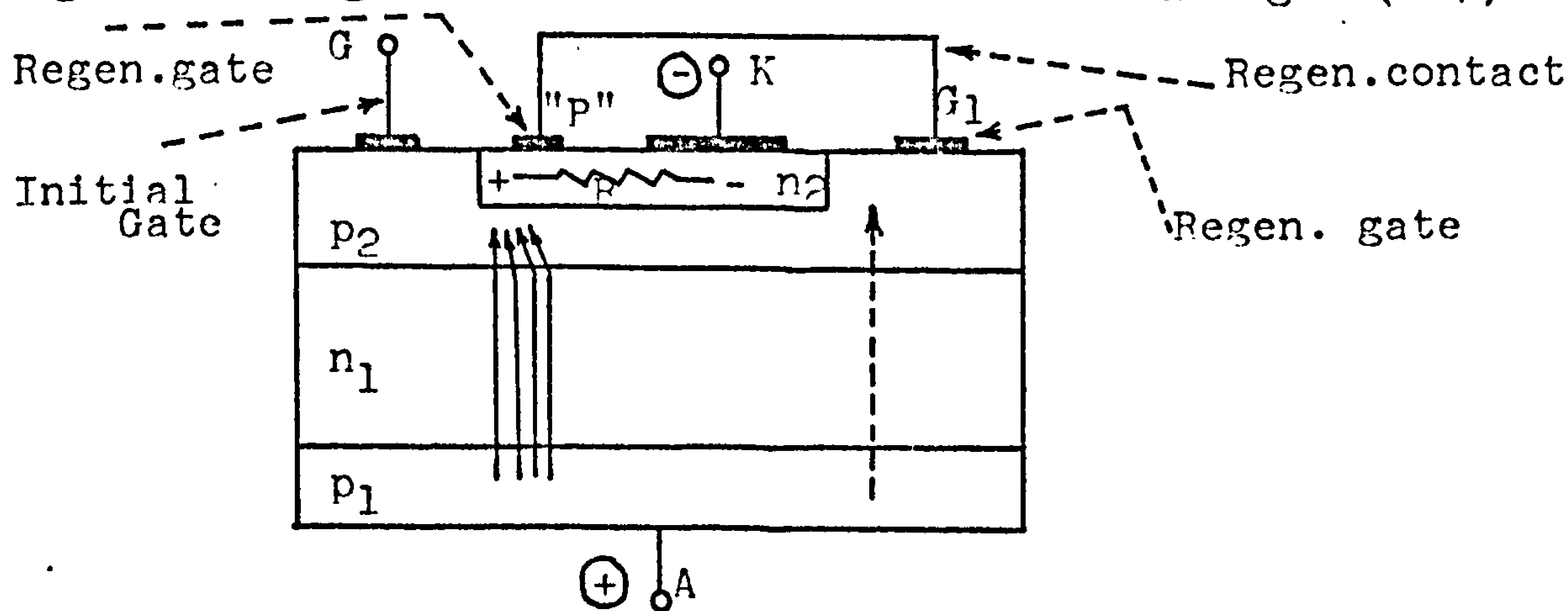


Figure (2-7) Regenenerative gate thyristor.

Once the device is switched on, the current flowing along the emitter produces a voltage drop. This voltage drop in the "P" lip acts as a signal generator. The magnitude of the output voltage V_0 is equal to

$$V_0 = \frac{Vr}{R+r} \tag{41}$$

where R is the variable resistance of the conducting area, r is the emitter lip lateral resistance and V_r is the anode voltage. This voltage which is positive with respect to the cathode can be picked off the emitter lip contact "P" and fed to point G_1 on the p_2 base layer. This offers the current an alternative path to the emitter contact with a lower resistance. Thus most of the current will flow in this direction and will provide a powerful gate drive G_1 the regenerative gate. This current will turn the device fully on. Thus the regenerative action can improve the di/dt capability. Multiple gates were used successfully with consistant firing at all of them.

2.3.4. Turn Off.

The turn off process is the regaining of the forward blocking state after termination of a forward current. When the device is in the conducting state, all three junctions are forward biased. Therefore both bases contain excess minority carriers figure (2-8) which increase with forward current. In order to turn off the device,

these excess carriers must be removed from the bases, by an electric field by reversing the applied voltage, or decay by recombination. This can also be done by removal of base current from the gate contact.

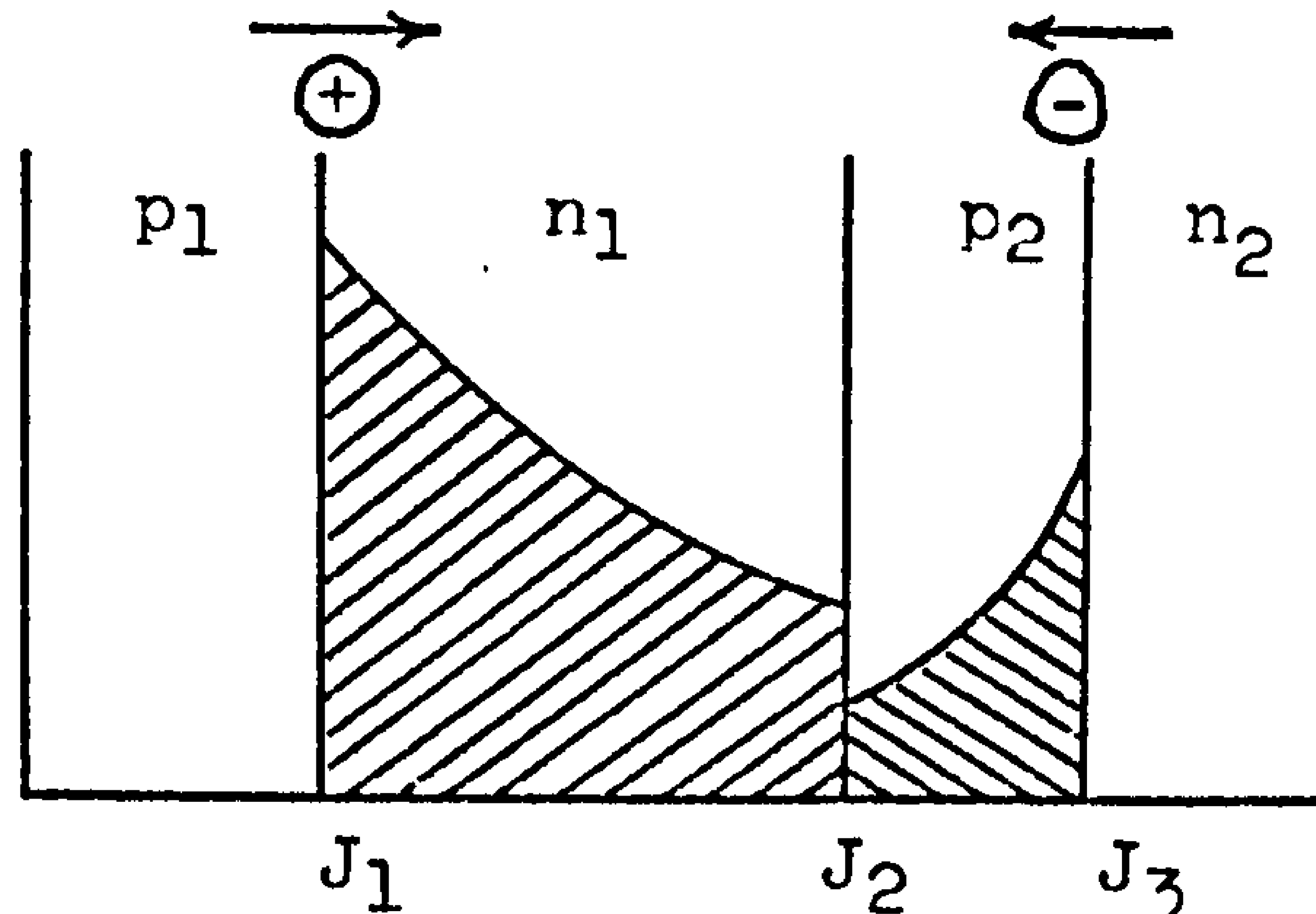


Figure (2-8) Charge distribution in bases in the conducting state.

When the voltage across the device is reversed, the junctions J_1 and J_2 become reverse biased whereas the junction J_2 remains forward biased. Junction J_3 because of high impurity concentration on both sides, will have a low avalanche breakdown compared with the two other junctions. Figure(2-9) illustrates the current wave form and charge distribution.

At the point just before t_0 on the time axis the device is fully on and carrying heavy forward current. When reverse bias is applied, junctions J_1 and J_3 starts collecting the minority carriers which have been injected under forward bias. When the excess minority carriers concentration at junction J_3 reaches zero (time t_1), its depletion layer starts spreading and J_3 becomes reverse

biased. The current through the circuit decays until the avalanche-breakdown of the junction is reached (time t_2). At this time the voltage across J_3 has risen to its break down value and the voltage across the device reaches an avalanche value of J_3. The current through junction J_2 during reverse recovery mostly consists of hole current injected from p_2 into n_1. Thus as holes leave base region n_1 to J_1 and are swept into the anode emitter, other holes enter the n_1 base by means of injection at junction J_2. On the other hand as electrons diffuse across p_2 to J_3 and are swept into the cathode emitter, only a small fraction of the base current near J_2 consists of electrons injected into p_2.

Thus electrons are being swept out of base p_2 by J_3 at a much faster rate than they are injected by J_2. Therefore the regions p_2 and n_2 are swept free of charge prior to n_1, i.e. the excess charge in the n_1 base cannot be removed readily but decays by recombination at a rate proportional to the minority carrier lifetime. Furthermore because of the lower doping and large width of the n_1 base, this region has more excess charge to lose than the p_2 base, and because of this the turn-off time is determined primarily by the charge decay in the n base of a conventional thyristor. However at time (t_3) the excess hole density at J_1 becomes zero. Then the voltage across J_1 begins to build-up, and the current decays to its steady-state blocking value.

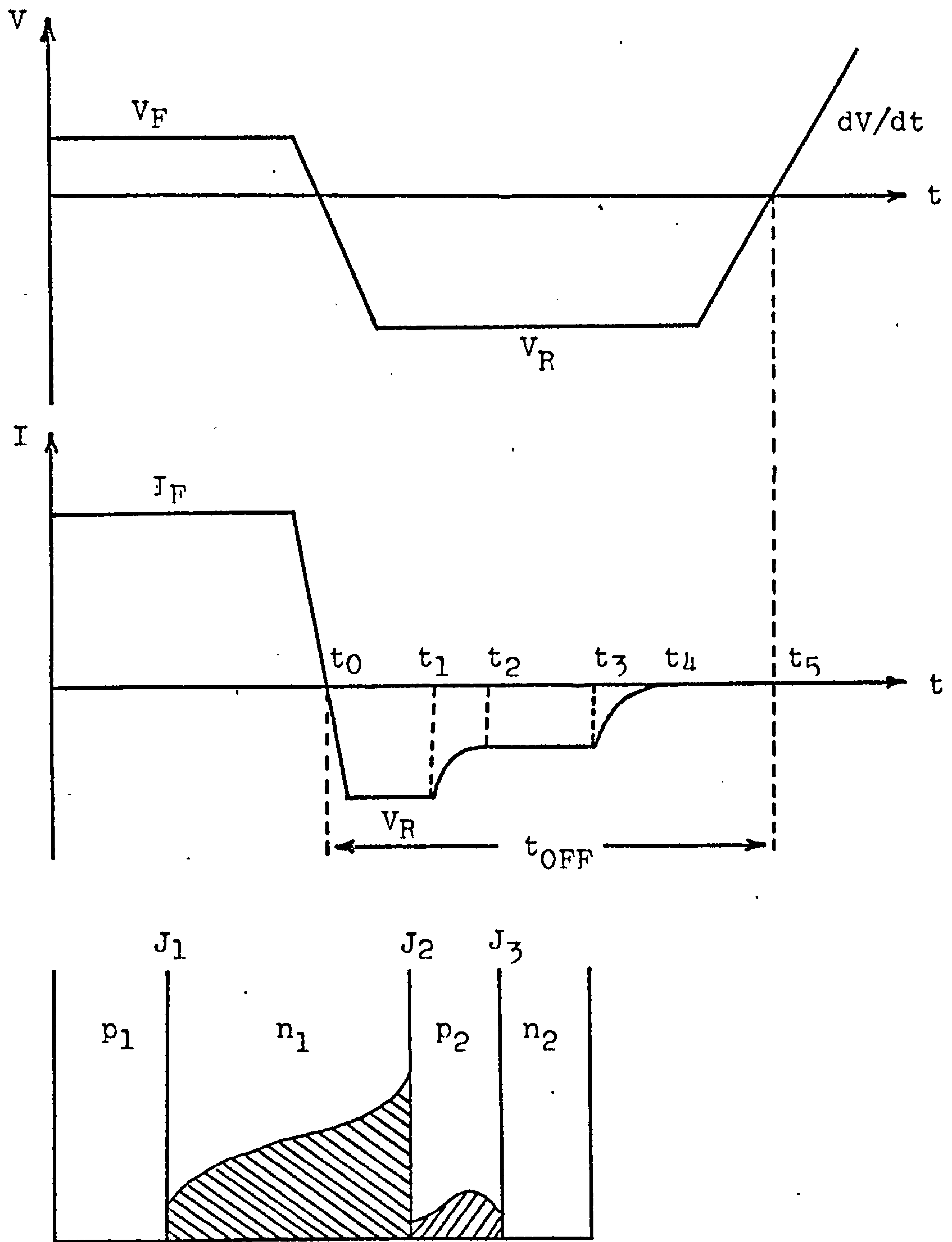


Figure (2-9) Current waveforms and charge distribution during turn-off.

The turn-off time, i.e. the time which must elapse after conduction before the device will block reapplied forward voltage is measured between the points, where current crosses the axis (t_5), and is theoretically defined

by figure (2-9):

$$t_{OFF} = \tau_p \ln \frac{I_F}{I_H} \tag{42}$$

under assumption that dV/dt and temperature effects are negligible. In equation (42) τ_p is the lifetime of the high resistivity base layer and I_F the forward current and I_H is the holding current.

Equation (42) shows that the turn-off time can be effectively lowered by lowering the lifetime of the minority-carriers (holes) or by increasing the holding current I_H, which may not be much help. For obtaining good dV/dt performance, this parameter is already made as high as possible.

Minority carriers lifetime can be controlled by diffusing impurity atoms into the base regions of the device. In practice gold is a convenient impurity, which acts as an effective recombination centre for minority carriers (Bullis 1966).

Lowering the minority carrier lifetime τ_p reduces the L_p and will lead to higher forward voltage drop of the device. W_n may be reduced to counteract this but then V_{BO} will suffer. Thus considerable compromise between parameters must be tolerated.

An improvement in the characteristics may be obtained if gold is diffused from the p_1 side of the wafer, therefore there is a fairly heavy concentration around J_2 but small along most of W_n. This requires a steep profile. In this way t_{OFF} can be reduced without affecting L_p to the same extent as with uniform diffusion.

It was already mentioned that the turn off process can be achieved by removing the base current from the gate lead, but this technique is limited to low currents or specially designed devices. In the gate turn off devices the carriers are removed from one of the base regions while the device is in the ON state. This can be done by application of reverse bias to the p-base (gated) region. Figure (2-10)

The removal of carriers will start from the edge of emitter adjacent to the gate contact; as a result, the lateral base voltage drops, causes junction J_3 to become reverse biased in the vicinity of the gate region and therefore ceases to conduct current. Thus the gate current will flow laterally through a base resistance. However, in this case, the anode current is determined by the same external circuit current. Since the ON area has been reduced, the current density in the remainder is higher than when the whole device was ON. As more and more gate current is withdrawn from the base, the region of cathode emitter junction J_3 at the vicinity of the gate lead finally avalanches, with the result that a shunt path for the

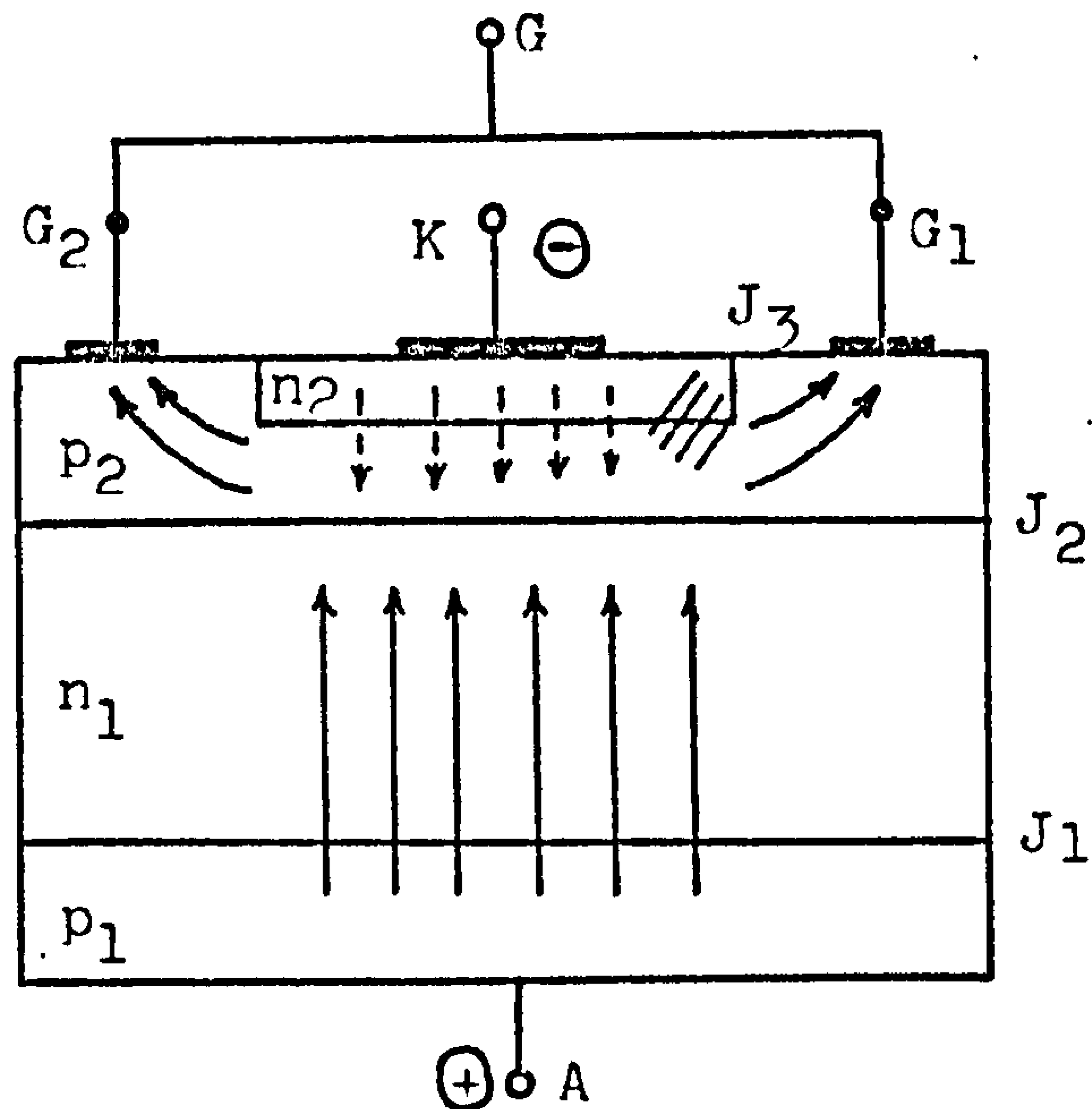


Figure (2-10) Gate turn-off thyristor

current developes between gate and cathode.

The magnitude of the reverse gate bias is limited to the reverse breakdown voltage of junction J_3 and can not be increased indefinitely.

In order to reduce the turn off time, Raderecht (1974) developed a device by combining the conventional thyristor and the gate controlled switch. By design of such a device he reduced the turn-off time quite remarkably (from 20μS to 6 μS) for a device with no gold doping. Then by introducing a gold impurity to provide trapping centres in the base region of the device, he achieved a turn-off time of 1-2 micro seconds with dV/dt capability of 600 V/μS rate of rise to 600 volts forward blocking voltage at 100°C, but at 25°C the rate of rise capability was reduced. This anomaly possibly could be altered by careful adjustment of

• the silicon resistivity and thickness or by introducing metallic impurities other than gold to reduce the lifetime of silicon.

3. Current Gain Measurement of High-Power Thyristors.

3.1 Introduction.

The characteristics of the silicon controlled rectifiers is determined, by the two component alphas, i.e. the current gains of the NPN and PNP transistor sections constituting the PNPN configration of the SCR. Thus a measurement of the two component alphas would appear to be as important in the design, fabrication and commercial manufacture of the SCR.

Several techniques are commonly employed in an effort to measure the two component alphas of the thyristor. One method consists of fabricating separately PNP and NPN sections of the SCR and measuring the two component alphas by means of transistor measurement. This method deviates from the desired degree of accurate simulation of the actual PNPN configuration in the measurements performed separately on PNP and NPN sections and do not reflect the subtle interplay of gate, cathode and anode current flow in the device.

Another method of measuring current gains of two transistor section is by connecting a lead to each section of the PNPN structure (Crees and Hogarth, 1963) and therefore measuring the two alphas by standard techniques employed on transistors. Utilization of the method is impeded by the inconvenience

and difficulty experienced in attaching a fourth lead to the n-base region since the commercial SCR is a three-lead device. However Fulop(1963) suggested a method for alpha measurements on the three terminal SCR, treating it as a hook transistor. His determination was based on the idea of cut-off frequencies of the PNP and NPN sections which are not identical and the alphas will have frequency characteristics from which one will be able to measure the PNP and NPN alpha values.

To represent the operation of the thyristor two equivalent circuits will be needed,

a. <u>DC equivalent circuit.</u>

From the two transistor analogue of the thyristor can readily be shown the relationship between dc currents flow and current gain factors, figure (3-1).

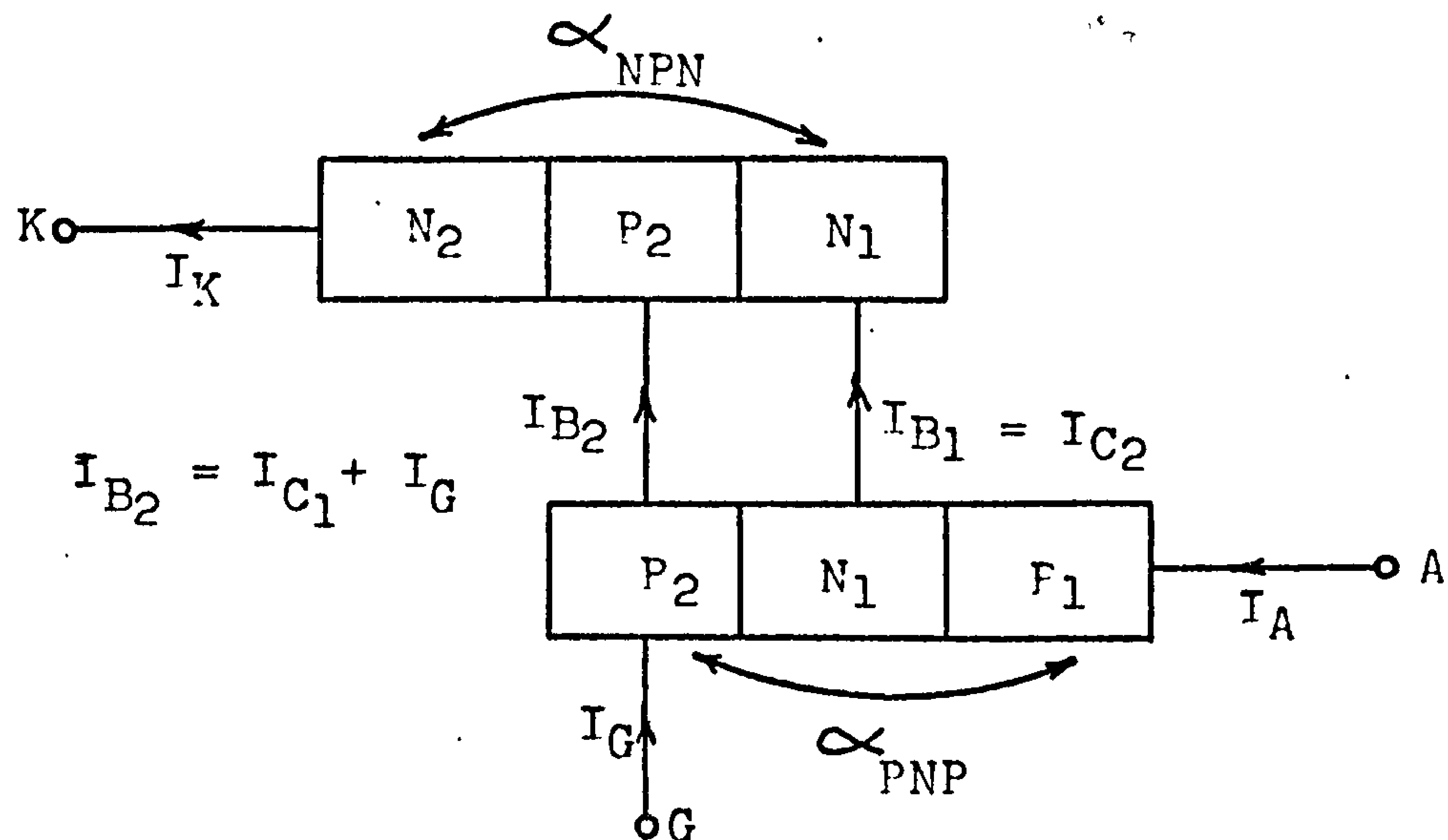


Figure (3-1) Two-transistor analogue of PNPN switch.

The base current of the PNP transistor is

$$I_{B_1} = (1-\alpha_{PNP})\, I_A - I_{CBO_1} \tag{43}$$

which is supplied by the collector of NPN transistor. However, the collector current of NPN section is

$$I_{C2} = \alpha_{NPN}\, I_K + I_{CBO_2} \tag{44}$$

where I_{CBO1} and I_{CBO2} are saturation current of reverse bias junctions of PNP and NPN transistors. The effective dc current gain of the SCR is given by

$$\alpha_{dc} = \frac{I_A}{I_K} \tag{45}$$

Neglecting multiplication at the reverse-biased centre junction and substituting equations (43) and (44) into (45), noting that $I_{B_1} = I_{C_2}$ the dc alpha willbe

$$\alpha_{dc} = \frac{\alpha_{NPN}}{1-\alpha_{PNP}} \tag{46}$$

The dc alpha is measurable but to obtain the values for α_{PNP} and α_{NPN} we resort to ac values where a frequency separation of alphas will yield their values.

b. AC Equivalent Circuit.

If the dc currents are held constant at a fixed bias, then a small signal ac current superimposed on the cathode current will causeasmall ac variation to appear in the anode current. The small signal effective alpha is defined as

$$\alpha_e = \frac{i_a}{i_k} \tag{47}$$

where i_a and i_k are the ac component of anode and cathode currents. From combination of the equivalent circuits for the two transistor sections, the small signal ac equi--valent circuit for PNPN can be shown as figure (3-2).

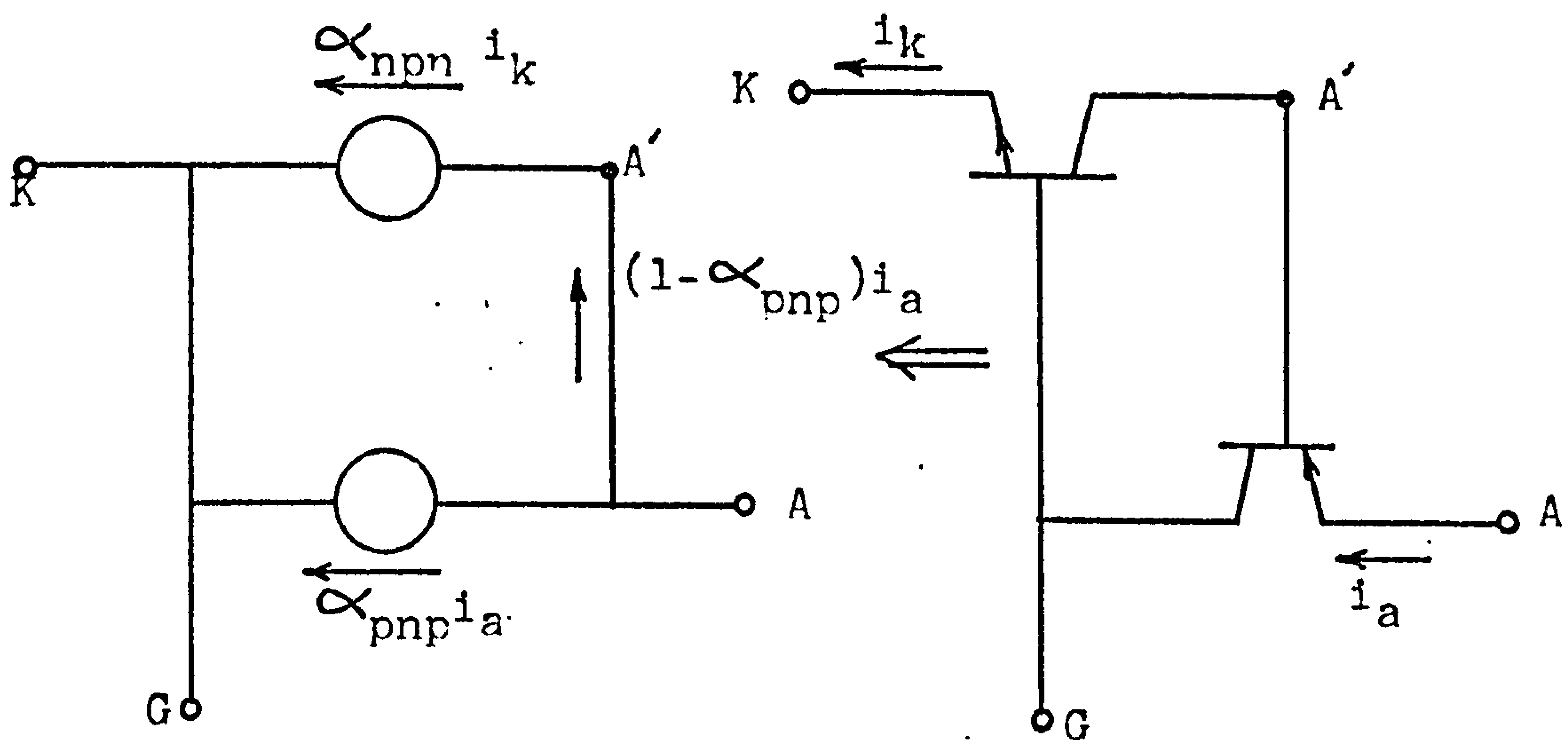


Figure (3-2) ac equivalent circuit of PNPN switch.

The current at point A is continuous thus:

$$(1 - \alpha_{pnp})\ i_a = \alpha_{npn}\ i_k \tag{48}$$

where α_{pnp} and α_{npn} are small signal current gain factors

of the thyristor. From equations (47) and (48) we have:

$$\alpha_e = \frac{\alpha_{npn}}{1-\alpha_{pnp}} \tag{49}$$

α_{npn} and α_{pnp} are limited by the cut-off frequency for minority carriers across the P and N base regions of the thyristor. The frequency variation of alpha can be equationated to (single pole approximation)

$$\alpha_{npn} = \frac{\alpha_{npn0}}{1+jf/f_n} \quad \text{and} \quad \alpha_{pnp} = \frac{\alpha_{pnp0}}{1+jf/fp} \tag{50}$$

where α_{pnp0} and α_{npn0} are low-frequency small signal current gains and f_p and f_n are cut-off frequencies for PNP and NPN transistors respectively. Substituting equation (50) into (49) we obtain:

$$\alpha_e = \frac{\dfrac{\alpha_{npn0}}{1+jf/fn}}{1-\dfrac{\alpha_{pnp0}}{1+jf/f_p}} \tag{51}$$

Since the base width of the PNP transistor is normally greater than the NPN section, therefore the cut-off frequency of the NPN is higher than the cut-off frequency of the PNP transistor. Figure (3-3) shows the frequency variation of α_e.

At the low frequency plateau region A of figure (3-3) the $f < f_p < f_n$, therefore $f/f_p < 1$ but $f/f_n \ll 1$ thus:

$$\alpha_e = \alpha_{e0} \cong \frac{\alpha_{npn0}}{1-\alpha_{pnp0}} \tag{52}$$

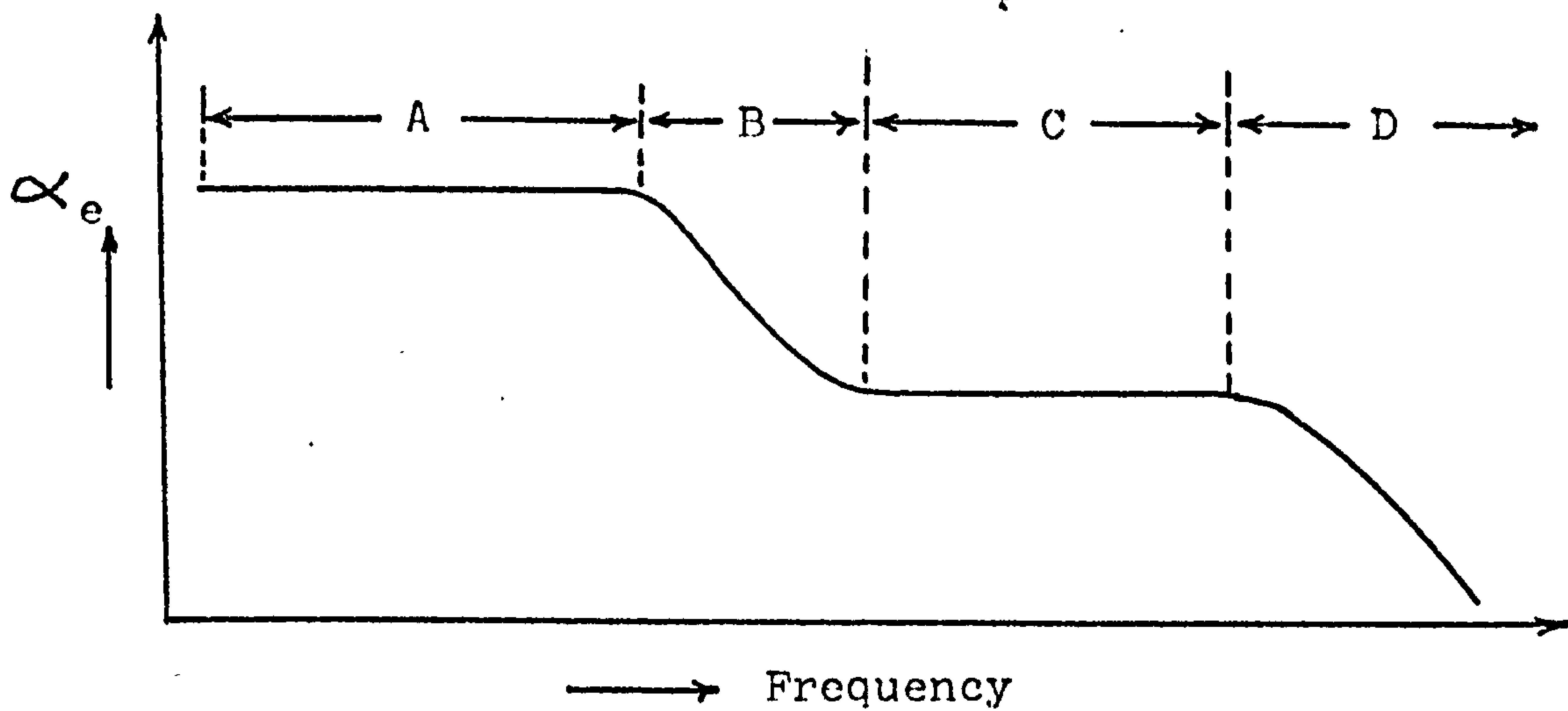


Figure (3-3) Frequency variation of effective alpha of PNPN switch.

and is measurable. At the plateau region C, $f_p < f < f_n$ therefore $f/f_p \gg 1$ and $f/f_n \ll 1$ thus:

$$\left| \alpha_e \right|_C = \alpha_{npn0} \tag{53}$$

Hence from the experimental measurement, α_{e0} and α_{npn0} are obtainable, and α_{pnp0} can be derived. Therefore the small signal alphas for the two transistor sections are known. At the frequency equal to the cut-off of two transistors the effective alpha is equal to

a) $f = f_n$ $\quad\quad f/f_p \gg 1$

$$\left| \alpha_e \right|_D = \frac{\alpha_{npn0}}{\sqrt{2}} \tag{54}$$

b) $f = f_p$ $\qquad f/f_n \ll 1$

$$\left|\alpha_e\right|_B = \frac{\alpha_{npn0}}{1 - \frac{\alpha_{pnp0}}{\sqrt{2}}} \tag{55}$$

As mentioned before the dc alphas α_{PNP} and α_{NPN}, can be readily defined from the ac values of current gains. The dc current gains of two transistor sections are defined by

$$\alpha_{PNP} = \left| I_{CP} / I_A \right| \quad \text{and} \quad \alpha_{NPN} = \left| I_{CN} / I_K \right| \tag{56}$$

where I_{CP} and I_{CN} are dc collector currents of the PNP and NPN sections respectively, with the total collector current given by

$$I_A = \left| I_{CP} \right| + \left| I_{CN} \right|$$

Thus to know dc current gains of two transistor sections one requires to know the I_{CP} and I_{CN} values. In order to obtain these, the frequency variation of effective alpha should be repeated for a series of measurable I_A values at fixed V_{AK} anode to cathode voltage. From this one will obtain the alphas as a function of their relevant emitter current.

$$\alpha_{npn0} = \alpha_{npn0}\,(I_K) \quad \text{and} \quad \alpha_{pnp0} = \alpha_{pnp0}\,(I_A)$$

Plotting the curve of alphas as a function of their emitter current, and by integration from the definition of alphas, one obtains I_{CN} and I_{CP}, thus:

$$\alpha_{npn0} = \left| \partial I_{CN} / \partial I_K \right| \qquad \text{and} \qquad \alpha_{pnp0} = \left| \partial I_{CP} / \partial I_A \right|$$

$$I_{CN} = \int_0^{I_K} \alpha_{npn0} \, d\, I_K$$

$$I_{CP} = \int_0^{I_A} \alpha_{pnp0} \, d\, I_A \tag{57}$$

and from the numerical integration of the α versus emitter current plots, one can obtain the separate dc. collector currents, I_{CN}, I_{CP}. This makes a plot of the emitter-collector dc current of each transistor section possible and the α_{PNP} and α_{NPN} readily follow according to equation (56).

3.2 Method of Measurement.

The circuit employed is shown in figure (3-4). The small signal anode and cathode currents i_a and i_k respectively were measured on an oscilloscope (later by sensitive valve-voltmeter) and the ratio of i_a/i_k was plotted as a function of frequency.

$$\alpha_e = i_a/i_k = \frac{V_a / R_A}{V_k / R_K} = \frac{V_a}{V_k} \quad \text{since } R_A = R_K = 5.7\,\Omega$$

Signal level of the order of $\sim$1mV across the 5.7 ohms

Figure (3-4) Circuit used for current gain measurements.

resistor of the cathode was employed. In order to get such a signal level across the cathode resistor a signal of order 3.0 mV to 15 mV was employed at the cathode -gate terminal. This variation of applied ac voltage was dependent on the size of the device. Therefore in comparison with the dc signal, the ac signal was low enough to call it "small signal".

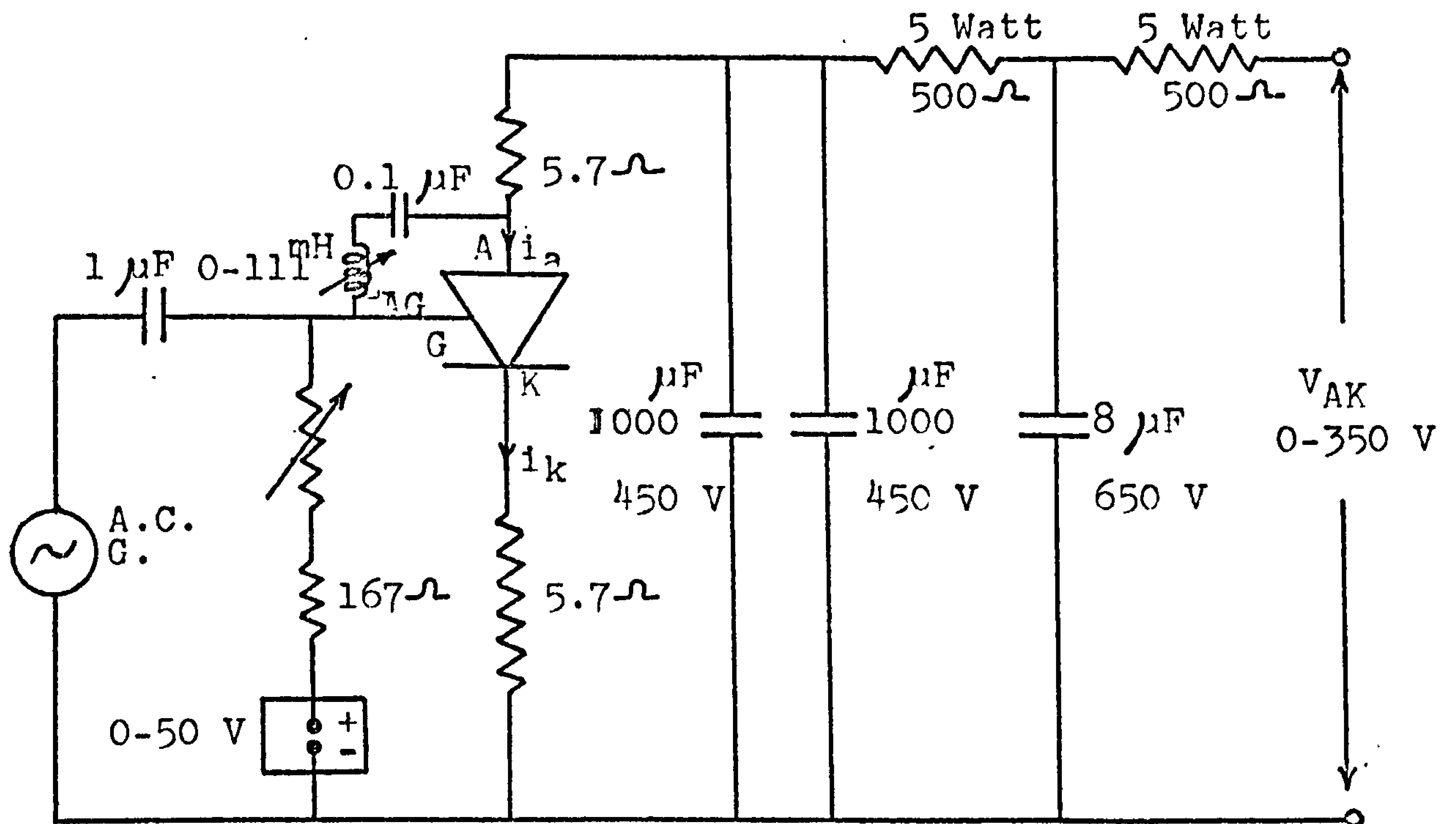


Figure (3-4) Circuit used for current gain measurements.

A variable inductance L_{AG} between the gate and anode was employed to tune out the unwanted feedback due to the centre junction capacitance at high frequencies (above 100 KHZ) to show up the decline of the second plateau. At high enough frequencies, the reverse biased junction capacitance acts as a parallel path to the anode current, shown in figure (3-5).

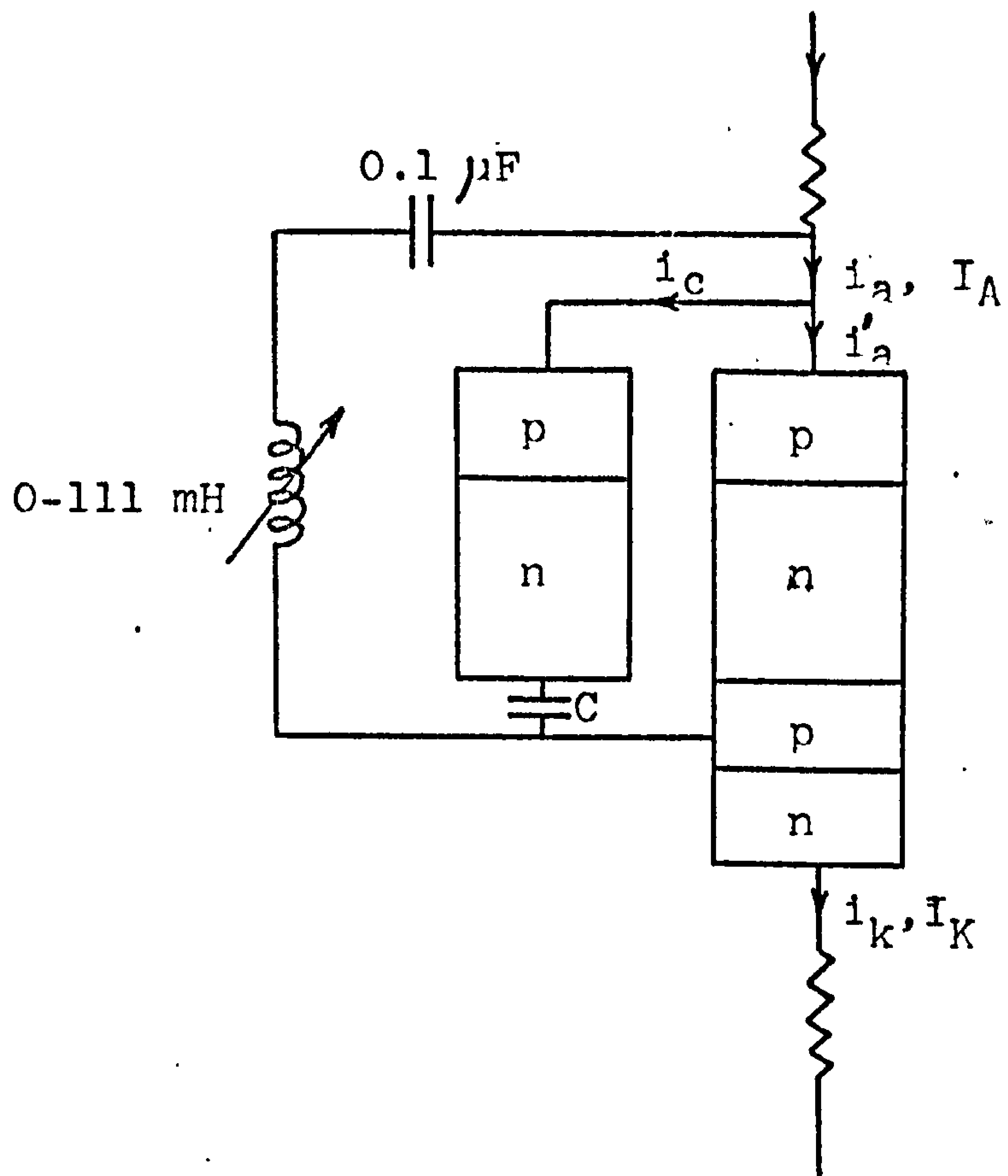


Figure (3-5) High frequency equivalent circuit.

The upper pn junction has a very low impedance as it is forward biased. The dominant term is the capacitance C and reverse biased junction capacitance. C has a very low impedance at high frequency. However, at low frequencies, capacitance C has very low admittance, hence i_c is very low and negligible compared to i'_a. Thus the effective alpha is

$$\alpha_e = \frac{i'_a}{i_k} \simeq \frac{i_a}{i_k}$$

where i'_a = true anode current.

At high frequency i_c is not negligible because of the lowered impedance of the C. Thus

$$\alpha_e = \frac{i_a'}{i_k} = \frac{i_a - i_c}{i_k} \neq \frac{i_a}{i_k}$$

Hence, by taking the ratio of i_a to i_k at high frequencies, the obtained value for the effective alpha will be high. However the inductance L_{AG} will tune out this capacitance and therefore i_c will find no path to by-pass and the obtained alpha will be near the true value. However it should be remembered that in this case the cut-off frequency obtained for α_{npn} is not a true value because the emitter-base capacitance will be tuned out at the same time.

3.3. Measurements:

A number of devices were measured and some details of their design where known are shown in the following table.

Device No.	Slice diameter	Slice thickness	Depth of P diffusion	Width of n type base	V_{BO}	I_{peak}	cal. f_{pnpt}
	cm	μm	μm	μm	KV	A	KHZ
1	1.8	175	37	100	0.8	116	39
2	3.7	450	87	275	2	500	5.1
3	3.7	1625	200	625	6	1000	1.0
4 not Au-doped					0.5	10	--
5 Au-doped					0.5	10	--

TABLE (1)

The calculated values of $f_{(pnp)t}$ were obtained from

Pritchard (1952).

$$f_{(pnp)\,t} = \frac{1.22\,D_p}{\pi W_n^2}$$

which assumes a purely diffusive minority carrier transport across W_n with a diffusion length $L_p \gg W_n$ relating in an approximate triangular excess carrier concentration profile. A value of order 10 cm^2/sec for D_p was assumed. These conditions may well not prevail and part of the small differences between $f_{(pnp)t}$ and their measured counterparts could be due to this.

3.3.1 Device No. 1

The measured α_e values versus frequency for anode-to-cathode voltages V_{AK} = 50 V and 200 V are plotted in figures (3-6) and (3-7) for a number of anode currents. Also the calculated value of α_{pnp0} and α_{npn0} as well as their sum α_{t0} are shown in figure (3-8) plotted as a function of I_A.

This device, in spite of its relatively small W_n shows low α_{pnp0} values. This could be due to a very low lifetime in the n base. The value of α_{t0} increased with V_{AK} and I_A but even at the highest V_{AK} and I_A values it is still well below the critical value of unity.

The anode-cathode dc-current characteristics of the

thyristor is shown in figure (3-9). However for 200 V V_{AK} the device was found to switch at 22 mA. The calculated $f_{(pnp)t}$ value agrees reasonably well with the measured value of f_{pnp} according to equation (55).

From the above curves and by utilizing equation (57) one can readily calculate the dc collector current of the NPN and PNP transistors (I_{CN}, I_{CP}) respectively, and hence the dc current gains of two transistor sections. At the point near the switching the values of I_{CN} and I_{CP} are equal to :

$$I_{CN} = \int_0^{I_K} \alpha_{npn0}\, dI_K \quad \text{and} \quad I_{CP} = \int_0^{I_A} \alpha_{pnp0}\, dI_A$$

$\therefore$

$I_{CN} = 19.38$ mA and $I_{CP} = 1.5$ mA

where

$V_{AK} = 200$ V and $I_A = 20$ mA

$\therefore$

$I_A(\text{cal.}) = I_{CN} + I_{CP} = 20.88$ mA

Comparing the calculated value of I_A with value of I_A directly obtained by measurement (20 mA) shows favourable agreement. Thus from this the sum of dc alphas can be calculated, which is well below unity.

$$\alpha_{PNP} + \alpha_{NPN} = 0.42$$

whereas at this point the sum of small signal alpha is considerably closer to unity.

$$\alpha_{t0} = \alpha_{npn0} + \alpha_{pnp0} = 0.74$$

This confirms that it is the small signal alphas which control the switching point.

3.3.2 Device No. 2

Values of V_{AK} = 10 and 50 V were chosen and the measured values of α_e versus frequency are shown plotted in figures (3-10) and (3-11). Figure (3-12) shows the values of α_{pnp0} and α_{npn0} versus I_A as well as α_{t0}. This device although it has the same slice diameter (3.7 cm) as device No. 3, in keeping with its much smaller n base width W_n value has much higher α_{pnp0} and f_{pnp} values. There is reasonable agreement between $f_{(pnp)t}$ and measured f_{pnp} values.

Figure (3-13) shows the dc anode-cathode characteristics of the device. This device switches at I_A = 10 and 12 mA for V_{AK} = 10 and 50 V, respectively, and α_{t0} is seen to be very close to unity near these values.

For this device the calculated value of dc collector currents I_{CN}, I_{CP} from the corresponding curves are:

I_{CN} = 0.5 mA and I_{CP} = 6.2 mA

where

$V_{AK} = 50$ V and $I_A = 10$ mA

therefore the calculated I_A value at the point near the switching is equal to

$$I_A \text{ (cal.)} = I_{CN} + I_{CP} = 11.2 \text{ mA}$$

which with a 10% error compares favourably with the value of 10 mA obtained in direct measurement. Thus the sum of dc alphas can be obtained, which is still below unity.

$$\alpha_{PNP} + \alpha_{NPN} = 0.81$$

where as at the same point the sum of small signal alphas is somewhat closer to unity.

$$\alpha_{t0} = \alpha_{npn0} + \alpha_{pnp0} = 0.96$$

This again shows that the sum of dc alphas is lower than sum of small signal alphas at switching point.

3.3.3 Device No. 3

This device like device No. 2 has a slice diameter of 3.7 cm but is capable of withstanding 6KV with a corresponding large W_n value. Figures (3-14) and (3-15) show the effective alpha α_e values as a function of

frequency for a number of anode values with V_{AK} = 50 and 200 V respectively. Figure (3-16) shows the calculated α_{pnp0} and α_{npn0} as well as α_{t0} the sum of alphas plotted as a function of I_A with V_{AK} as a parameter. Although reasonable agreement was obtained between $f_{(pnp)t}$ and f_{pnp}, it was not as good as expected. The reason for this being the wide n-region, which will yield a higher f_{pnp}.

The α_{npn0} values are comparable with those obtained for device No. 2 but α_{pnp0} is, because of the much wider W_n, considerably reduced.

The dc anode current as a function of cathode dc current is shown in figure (3-17).

The dc collector currents of npn and pnp transistor sections (I_{CN} , I_{CP}) were calculated according to their respective curves and from this the dc current gains.

I_{CN} = 18.36 mA $\qquad\qquad$ I_{CP} = 3.2 mA

$\therefore$

I_A (cal.) = $I_{CN} + I_{CP}$ = 21.56 mA

where V_{AK} = 200 V and I_A = 20 mA.
This again shows reasonable agreement between calculated I_A and measured I_A. So the dc sum alpha will be:

$$\alpha_{NPN} + \alpha_{PNP} = 0.33$$

This is lower than small signal alpha sum, because at this point α_{t0} is equal to

$$\alpha_{t0} = \alpha_{npn0} + \alpha_{pnp0} = 0.49$$

Once again this shows the dominant influence of small signal alphas in controlling the switching point.

3.3.4 Device No. 4 (Not Au-Doped)

Measured α_e values versus frequency for anode-to-cathode voltage V_{AK} equal to 50 V is plotted in figure (3-18) for a number of anode currents. The calculated values of α_{pnp0} and α_{npn0} and their sum are shown in figure (3-19) plotted versus I_A the anode current.

The anode-cathode dc current characteristics of the small not Au-doped 10A thyristor is shown in figure (3-20). The slope of this is α_{e0} and agrees well with the measured value at one point. For 50 V anode to cathode voltage the device was found to switch round about 3.5 mA.

Once again the calculated values of I_{CN} and I_{CP} were obtained from corresponding curves, and reasonable agreement was found between calculated I_A and measured one.

$I_{CN} = 2.8$ mA and $I_{CP} = 0.3$

where

$V_{AK} = 50V$ and $I_A \doteq 3mA$

$\therefore$

$I_A \text{ (cal.)} = I_{CN} + I_{CP} = 3.1$ mA

The sum of dc alphas at this point near the switching is

$$\alpha_{PNP} + \alpha_{NPN} = 0.45$$

which is below unity.

where as at this point the sum of small signal alphas is not far from unity.

$$\alpha_{pnp0} + \alpha_{npn0} = 0.90$$

3.3.5 Device No. 5 (Au-Doped)

This device is nominally identical to device No. 4 except that it was gold doped. This is in order to reveal the influence, if any, such doping might have on the current gains as well as the known effect on switching speed. The value of $V_{AK} = 50V$ was chosen and the measured values of α_e versus frequency are shown plotted in figure (3-21). Figure (3-22) shows the values of α_{pnp0} and α_{npn0} versus

I_A as well as α_{t0} the sum of alphas. The effect of gold doping on α_{pnp0} is particularly pronounced. This value has been depressed because of the considerably reduced lifetime in the wider ungated region. However, figure (3-23) shows the anode-cathode dc current curve of such a device. For this device the switching current found to be 10 mA at $V_{AK} = 50^V$ and α_{t0} is seen to be very close to unity near this value.

For this device the calculated values of dc collector currents I_{CN} and I_{CP} from their respective curves versus emitter currents at point near the switching are

$I_{CN} = 8.2$ mA $\qquad$ $I_{CP} = 0.45$ mA

where

$V_{AK} = 50$ V $\qquad$ and $\qquad$ $I_A = 9$ mA

therefore the calculated I_A will be:

I_A (cal.) $= I_{CN} + I_{CP} = 8.65$ mA

which is in reasonable agreement with measured I_A. The sum of dc alphas at this point is

$$\alpha_{NPN} + \alpha_{PNP} = 0.49$$

whereas the sum of small signal alphas is very close to unity at this point.

$$\alpha_{t0} = \alpha_{npn0} + \alpha_{pnp0} = 0.92$$

This once again confirms that it is the small signal alphas which control the switching point.

3.4 Discussion of Results.

The manner in which the devices were measured showed that the Fulop method (1963) originally employed for the measurement of small current gain factors can be successfully applied to the measurements of high-power thyristors, provided that certain precautions are taken with the measuring system. The method ensured that the centre junction was reverse-biased and the outer junctions were forward biased. The thyristor is therefore in the high impedance domain and dc anode current I_A is varied by varying the gate forward bias on the p-type base p_2.

The measured values of α_{npn0} and α_{pnp0} together with the values of f_{pnp} and f_{npn} would be expected to yield some qualitative, if not quantitative, information on the dimensions and material properties (lifetime, doping profile, etc.) of the thyristor. By repeating these measurements at a number of fixed current levels, the dc component of currents in the separate transistor sections can be cal--culated and from this the dc current gains α_{NPN} and α_{PNP} can be readily obtained. It was found that the

$\alpha_{t0} = \alpha_{npn0} + \alpha_{pnp0}$ were near unity at switching of the thyristor. But at the voltage similar to that applied to measure the small signal current gain factors the sum of dc current gains $\alpha_{NPN} + \alpha_{PNP}$ was found well below unity. This shows that, it is the small signal alphas that control the switching point rather than dc alphas. That means switching occurs when $\alpha_{npn0} + \alpha_{pnp0} \geqslant 1$.

In a fuller investigation of the switching process in high-power thyristors, consideration would need to be given to the degree that the two-dimensional or lateral aspects of these measurements on these large area thyristors play a part. Emitter fringing of the cathode due to lateral gate current flow in the p-type base would be a case in point and here the influence of the shorting dots in the cathode would be interesting to evaluate. The currents flowing in the above measurements are admittedly small but apart from the low value of V_{AK}, not all that far removed from the switching condition. In fact I_A was increased as far as permissible without switching the device.

W.C. Un (1974) proposed an automatic system for measuring small signal current gain factors of thyristor. His method is much faster and also accurate than hand plot method.

4. The Current Gain Temperature Dependence in Thyristors.

4.1 Introduction.

From early papers one gains the impression that the effect of temperature on thyristors is to degrade their voltage blocking characteristics, quite remarkably so in some cases. This was shown by Smobyanski (1963). In many cases the degradation is due to increased surface leakage current which is very sensitive to temperature.

One of the important effects of temperature is to increase the saturation current of the reverse biased junction which increases the two alphas of separate sections. Another effect is that the injection efficiency of emitters γ increases with temperature because of the rapid increase of diffusion components of current compared to the recombinat - generation component with temperature.

Raderecht and Hogarth (1964) did measurements on four-terminal SCR's investigating temperature dependence. At low currents the variation of α_{npn} will depend largely on the variation of emitter efficiency which increases as temperatur rises. α_{pnp} which can be shown to be $\beta\gamma$ at this level of current also increases with temperature. At medium currents there is small change of α_{npn} with increasing temperature which is ascribed to a decrease of resistivity of the p-base canally not a tendency for the diffusion length of holes in the emitter region.

But α_{pnp} remains fairly constant or shows a slight increase, due to the increasing transport factor β, as the temperature increases. At high currents due to the dominant effect of resistivity of the base on diffusion length of minority carriers, the emitter efficiency hence α_{npn} will decrease as the temperature rises. α_{pnp} will remain small and fairly constant over a range of temperature because the emitter efficiency decreases with current and temperature since the transport factor β increases as temperature rises; therefore α_{pnp} depends on two opposing trends.

Buhana (1969) investigated the temperature variation of current gain of transistors. He showed that lifetime τ_b varies as n_i^2 and thus as $T^3 e^{-Eg/kT}$. The transport factor is given by

$$\beta = \text{sech} \frac{W}{L_{nb}} \qquad (58)$$

and

$$L_{nb} = \sqrt{D_{nb} \tau_b}$$

The decrease of D_{nb} with increasing temperature which is caused by increased lattice scattering, will compensate by increase of τ_b with temperature. The overall effect on L_{nb} will be an increase with increasing temperature and therefore of β with temperature.

In his paper he claimed that a heavy emitter causes a

decrease of energy gap E_g due to lattice stress. This is because at high doping levels lattice deformations and dislocations produce a change in energy gap. This in turn, leads to a different value of n_i in emitter than in base. The emitter efficiency expression for an NPN transistor corrected for the effect of ΔE becomes:

$$\gamma = \frac{1}{1 + (D_{pe}/D_{nb})(W/L_{pe})\ k\ \exp(\Delta E/kT)} \qquad (59)$$

This introduces an exponential temperature dependence into the expression. In thyristors the only emitter which may have such higher doping in N_2 region, therefore γ_{NPN} shows this effect in some devices.

4.2. Method of Measurement.

Measurements of current gain values were made by the method described in the previous section. The thyristor was placed in an oven with a temperature controller and also an electronic thermometer with a copper-constantan thermocouple which was used to record the device temperature. Temperature was checked during measurements with an accuracy of $\pm$ 2°C.

Measurements were carried out on devices as previously employed (table 1). For a given constant temperature reading, the usual voltage anode/cathode ratio was taken for various frequencies of the small ac signal between 500 C/S

and 500 KC/S. The dc conditions were set by measuring the anode-cathode voltage V_{AK} and anode current I_A. The anode-cathode voltage was kept constant and the readings were repeated for a number of different anode currents up to permissible current values. The temperature setting on the oven was then altered and the whole series of experiments was repeated at the new temperature setting.

Switching parameters were then recorded over the range of temperature, $20^\circ C$ to $160^\circ C$ except for device No. 5 for which measurements over the range of 20 to $200^\circ C$ were made.

4.3 Results.

Figure (4-1) shows for device No. 1 the variation of α_{npn0} and α_{pnp0} with temperature at a number of fixed anode currents. The sum $\alpha_{t0} = \alpha_{npn0} + \alpha_{pnp0}$ is also plotted and from this one can derive the variation of I_{BO} the breakover current, with temperature; I_{BO} is defined as a current through the device at the point of breakover under two-terminal operation and is governed by the condition $\alpha_{t0} = 1$. Therefore the curve $I_{BO}(T)$ as a function of temperature is the locus of all points as T is varied for which $\alpha_{t0} = 1$ at of course the prevailing breakover voltage V_{BO}.

This can be closely simulated under three-terminal operations, and at a considerably reduced voltage

compared to the two terminal breakover voltage V_{BO}, by moving along a line of constant α_{tO}, such as is plotted in figure (4-1), as close to unity as possible. Observing the intersection with curves plotted for constant I_A , it will be seen that initially curves of decreasing I_A values are intersected and then as temperature increases further, increasing I_A values are intersected. Figure (4-2) shows the measured I_{BO} values plotted versus temperature and this confirms the trend predicted from figure (4-1).

Gate firing current I_G is found to decrease linearly as the temperature rises. This was expected since the generated minority carrier current increases with temperature, therefore I_G for a fixed I_A should decrease. This is shown in figure (4-3). The variation of breakover voltage V_{BO} decreases with increasing temperature, as a result of injection due to increased current carried by junction J_2.

For devices Nos. 2,3,4 and 5 the corresponding curves are shown in figures (4-5),(4-6), (4-7) , (4-8),(4-9),(4-10) (4-11),(4-12),(4-13) ,(4-14),(4-15) and (4-16) respectively. Once again the effect of gold doping emerges from figures (4-11) and (4-14) which are for two nominally identical small thyristors (10A) except that one is made from deliberately gold-doped silicon.

4.4 Analysis of Instability of pnpn devices.

It is well known that the small signal low-frequency alphas which for $\alpha_{t0} = \alpha_{npn0} + \alpha_{pnp0} = 1$, determines the point of instability. We shall now discuss some aspects of instability. In particular we are interested in what role the variation of α_{npn0} and α_{pnp0} with temperature and anode current play. We shall assume multiplication to occur across the central reverse-biased junction and for mathematical convenience shall put $M = M_n = M_p$ where M_n and M_p are the multiplication ratioes for electrons and holes respectively. Also to put the operative transistor section beyond doubt we write for the large signal alpha of the npn section α_{NPN} and that for the pnp section, α_{PNP}.

For the anode current I_A we have therefore

$$I_A = M\alpha_{PNP}I_A + M\alpha_{NPN}I_K + MI_{c0} + I_{Dis} \tag{60}$$

where $I_K = I_A + I_G$, I_K being the cathode current, I_G the gate current, I_{c0} the saturation current of the isolated reverse-biased centre junction, and I_{Dis} is the displacement or capacitive current flowing due to a rate of change of voltage across the depletion layer capacitance C_J of the centre-junction.

This can be written as

$$I_{Dis} = \frac{d}{dt}(C_J V) \tag{61}$$

where V = voltage across the centre junction which to a good approximation is the total applied voltage.

From this it follows that

$$I_A = \frac{M(\alpha_{NPN} I_G + I_{cO}) + I_{Dis}}{1 - M(\alpha_{PNP} + \alpha_{NPN})} \quad (62)$$

Thus I_A is not only the dc current but may also contain (large-signal) transient due to $I_G(t)$ or I_{Dis}.

Considering I_A as the large signal emitter current of the pnp section with a corresponding collector current I_{CP}, and similarly for the npn section I_K and I_{CN}, then clearly:

$$I_A = I_{CP} + I_{CN} \quad (63)$$

$$I_{CN} = M\alpha_{NPN} I_K + M\, I_{cOn} + I_{Dis} \quad (64)$$

$$I_{CP} = M\alpha_{PNP}\, I_A + MI_{cOp} \quad (65)$$

where $I_{cO} = I_{cOn} + I_{cOp}$ are the electron and hole current contributions coming respectively from the p and n type case and I_{Dis} has been arbitrarily assigned to the npn section. Alternatively MI_{cO} can be assigned only to one or other of the sections, but together with I_{Dis} can only be "counted once".

In the previous section we showed how the dc components of I_{CN} and I_{CP} can be calculated from graphs α_{npn0} versus I_K, and α_{pnp0} versus I_A respectively and thus we can evaluate the large signal alphas α_{NPN} and α_{PNP}.

Following Gentry (1964) but including the multiplication factor,

$$\frac{dI_{CN}}{dI_K} = \alpha_{npn0} = M\alpha_{NPN} + MI_K \frac{d\alpha_{NPN}}{dI_K} = M\alpha^0_{npn0} \tag{66}$$

$$\frac{dI_{CP}}{dI_A} = \alpha_{pnp0} = M\alpha_{PNP} + MI_A \frac{d\alpha_{PNP}}{dI_A} = M\alpha^0_{pnp0} \tag{67}$$

where α^0_{npn0} and α^0_{pnp0} are the low-voltage values of α_{npn0} and α_{pnp0}. Differentiating equation (60) with respect to x where x could be any parameter likely to influence current flow, e.g. temperature T, applied voltage V or currents (I_G, I_{Co}, or I_{Dis}) we have with the help of the above equation:

$$\frac{dI_A}{dx} = \frac{I_{A0}\dfrac{dM}{dx} + \alpha^0_{npn0}\dfrac{dI_G}{dx} + M\cdot\dfrac{dI_{c0}}{dx} + \dfrac{dI_{Dis}}{dx}}{1-M\alpha_{t00}} \tag{68}$$

where

$$I_{A0} = \alpha_{PNP}I_A + \alpha_{NPN}I_K + I_{c0} = (\alpha_{NPN}I_G + I_{c0})\left[1-(\alpha_{NPN}+\alpha_{PNP})\right]^{-1}$$

is the "low (constant) voltage" value of I_A and

$$\alpha_{t00} = \alpha^0_{npn0} + \alpha^0_{pnp0}$$

In the derivation of equation (68) terms such as $(d\alpha_{NPN}/dx)$ have been converted to $(d\alpha_{NPN}/dI_K)(dI_K/dx)$ with $d\alpha_{NPN}/dI_K$ being substituted from equation (66). Since x could represent either I_{c0} or I_{Dis} and I_K as well as I_A do contain these currents, it might be thought that these terms ought to be retained in equations (66), (67). For instance from equation (64) $M(dI_{c0n}/dI_K)$, dI_{Dis}/dI_K may be thought to qualify for inclusion into equation (66). However the small signal differentiation of equations (66) and (67) refer to "externally and deliberately applied" changes in I_A and I_K so that for instance $d\alpha_{NPN}/dI_{c0}$ is legitimately split into the product $(d\alpha_{NPN}/dI_K)(dI_K/dI_{c0})$, the changes of I_K due to I_{c0} being accounted for by the second factor. The various instability conditions can now be derived from equation (62).

a) Two Terminal Instability Due to Incease in I_{c0}

$$\frac{dI_A}{dI_{co}} = \frac{M}{1 - M\alpha_{t00}} \qquad (69)$$

assuming M to be only a function of the voltage V across the centre junction, which to a good approximation is the total applied voltage across the device.

α^0_{npn0} and α^0_{pnp0} are of course functions of the current flow through the device as the above measurements confirms. The instability condition $M\alpha_{t00} = 1$ could thereforebe reached because of an increase in I_{c0} and hence I_A with substantially $M \simeq 1$. However correct design and operation aims at the condition $M > 1$ for breakover, so that the full blocking capability of the centre junction is utilised.

b) Two Terminal Instability Due to Voltage Increase.

$$\frac{dI_A}{dV} = \frac{I_{c0}\left[1-(\alpha_{PNP} + \alpha_{NPN})\right]^{-1} \frac{dM}{dV} + M\frac{dI_{c0}}{dV}}{1 - M\alpha_{t00}} \tag{70}$$

With I_{c0} being proportional to space charge width of the centre junction the dI_{c0}/dV will be a slowly varying function compared to the dM/dV term, particularly as with $M > 1$ the breakover region is being approached and once more will be governed by $M\alpha_{t00} = 1$, with M often quoted as equal to $\left[1-(V/V_B)^m\right]^{-1}$ where V_B is the breakdown voltage of the junction, and m is an empirically determined index.

$$\frac{dM}{dV} = mM^2\left(\frac{V}{V_B}\right)^{m-1} \tag{71}$$

c) $\frac{dV}{dt}$ Switching.

Premature two terminal switching can occur if I_{Dis}

and hence I_A, as a consequence of a rapid rise in V, increases to a value such that $\alpha_{t00} = 1$ with V well below V_{BO}. Thus from equation (68)

$$\frac{dI_A}{dI_{Dis}} = \frac{1}{1 - M\alpha_{t00}} \tag{72}$$

Considering I_A from the point of view of time variation

$$\frac{dI_A}{dt} = \frac{I_{c0}\left[1-(\alpha_{NPN}+\alpha_{PNP})\right]^{-1} \frac{dM}{dV}\cdot\frac{dV}{dt} + M\frac{dI_{c0}}{dV}\cdot\frac{dV}{dt} + \frac{d^2}{dt^2}(C_jV)}{1-M\alpha_{t00}} \tag{72}$$

for two terminal operation.

Equation (61) for I_{Dis} was utilised and $\dfrac{d^2(C_jV)}{dt^2}$ could well, for a rapidly rising voltage, be the dominant term.

d) Gate Triggering.

From equation (68)

$$\frac{dI_A}{dI_G} = \frac{M\alpha^0_{npn0}}{1-M\alpha_{t00}} \tag{73}$$

Here use is made of the current dependence of α_{t00}, I_A being substantially increased by deliberate application of I_G (equation 62) with breakover now occurring at a very

low voltage compared to V_{BO}.

e) Temperature Instability.

Equation (68) now yields

$$\frac{dI_A}{dT} = \frac{I_{AO} \frac{dM}{dT} + M \frac{dI_{cO}}{dT}}{1 - M\alpha_{tOO}} \tag{74}$$

where for two terminal operation $I_{AO} = I_{cO}\left[1-(\alpha_{PNP}+\alpha_{NPN})\right]^{-1}$
Avalanche multiplication does depend upon temperature, due to increased Phonon scattering for increasing temperature. However $\frac{dM}{dT}$ term will be very small compared to the second term so that approximately

$$\frac{dI_A}{dT} \simeq \frac{M \frac{dI_{cO}}{dT}}{1 - M\alpha_{tOO}} \tag{75}$$

Because of the exponential temperature dependence of I_{cO} and its influence via I_A upon the sum alpha α_{tOO} this can lead with two terminal operation to a rapid rise of I_A with temperature and finally to an instability due to $M\alpha_{tOO} = 1$ at a voltage $V_{BO}(T)$ considerably reduced compared to its value at room temperature.

Figure (4-17) shows for device No.1 the variation of I_A with temperature for a number of fixed gate current I_G values.

It is perhaps of interest to investigate equation (75) further and examine the influence of the temperature and anode current I_A dependence of α_{npn0} and α_{pnp0} upon the instability of the device. Under a two-terminal blocking condition as T increases so will I_A, due to $I_{c0}(T)$ and thus the total T dependence of the alpha's will be involved. We have therefore equation (76) for the total temperature dependence.

$$\frac{d\alpha^0_{npn0}}{dT} = \frac{\partial\alpha^0_{npn0}}{\partial T} + \frac{\partial\alpha^0_{npn0}}{\partial I_A}\cdot\frac{dI_A}{dT} = \frac{\partial\alpha^0_{npn0}}{\partial T} + \frac{\partial\alpha^0_{npn0}}{\partial I_A}\cdot\frac{\frac{dI_{c0}}{dT}}{1-M\alpha_{t00}} \tag{76}$$

and similarly for α^0_{pnp0} involving $\partial\alpha^0_{pnp0}/\partial I_A$. Differentiating equation (75) once more with respect to temperature

$$\frac{d^2I_A}{dT^2} \simeq \frac{M\frac{d^2I_{c0}}{dT^2}}{1-M\alpha_{t00}} + \frac{M^2\frac{dI_{c0}}{dT}}{(1-M\alpha_{t00})^2}\left[\frac{\partial\alpha_{t00}}{\partial T} + \frac{\partial\alpha_{t00}}{\partial I_A}\cdot\frac{M\frac{dI_{c0}}{dT}}{1-M\alpha_{t00}}\right] \tag{77}$$

once more neglecting terms due to dM/dT. Here again the dominant influence of I_{c0} due to its exponential temperature dependence can be seen at once. Not so clear perhaps is the relative influence of the term involving $\partial\alpha_{t00}/\partial T$ and $\partial\alpha_{t00}/\partial I_A$. Though for some devices $\partial\alpha_{t00}/\partial T < 0$ in some regions, $\partial\alpha_{t00}/\partial I_A > 0$ overall regions and is the dominant term in the $d\alpha_{t00}/dT$ total variation, not least due to the dI_{c0}/dT term. We have plotted α^0_{npn0} and α^0_{pnp0} versus temperature at fixed I_G values thus

allowing I_A to increase with temperature and this is shown in figure (4-18) for device number 1. For this device $(d\alpha_{t00}/dT) > 0$ seems to be borne out.

The Raderecht and Hogarth (1964) results on four-terminal pnpn devices confirm ours. They ascribed the $(\partial \alpha^{0}_{npn0}/\partial T) < 0$ values which occur at the higher temperatures, (which we also observed) due to the increasing conductivity of the p-base region with increasing temperature causing a drop in emitter efficiency of the npn section.

However it was observed that $(\partial \alpha^{0}_{pnp0}/\partial T) > 0$ which, apart from device No.1 at higher temperatures also occurred in our experiments, is due to the increasing lifetime in the n-type base and hence increasing minority carriers diffusion length L_{pb} with increasing temperature, this would increase β, the minority carrier transport factor which for most devices is very small. The one exception in our measurements, device No. 1, for which $(\partial \alpha^{0}_{pnp0}/\partial T) < 0$ at the higher temperature, figure (4-1), could well be due to the low doping of the p-region. The increasing conductivity of the n-region with temperature could thus have such a pronounced effect on lowering the emitter efficiency of the pnp section as to exceed the improvement in alpha due to the increasing minority carrier lifetime with temperature in the n-type base.

4.5 Conclusion.

The small-signal lowlfrequency current gains of the constituent transistors of thyristors were measured as a function of anode current, temperature and gold-doping.

The measurement showed, not surprisingly, that the I_{c0} dependence upon temperature exercises the most serious influence upon instability. This has a large impact upon the partial derivative on the sum alpha with current which is always positive. The corresponding partial derivative with temperature, which is sometimes negative has much less influence.

From the curve of current gain versus temperature, taken at a series of anode currents, the temperature dependence of $I_{BO}(T)$, the two-terminal breakover current at which switching occurs, could be qualitatively estimated. Gold-doping predictably resulted in a low current gain for the pnp section.

5. The Current Gain Measurements of Devices with a Shorted Emitter and Their Dependence Upon Temperature.

5.1 Introduction.

We have already shown (section 3&4) that the switching mechanism in the thyristor is dependent upon the variation of alpha with current and temperature. We have also mentioned that one method of controlling the current gain of a device is by careful control of the impurity concentration between emitter and base. This will improve the dV/dt performance of the device.

Another possible method of controlling the current gain values of the system with optimum resistance by means of current is to introduce some acceptable impurity into the basic silicon to give rise to trapping levels. At low currents, these traps will be partially filled, hence will reduce lifetimes; but at high currents, they will be filled and the normal values of lifetime will be regained (Tokumaru 1963).

The emitter efficiency and therefore current gain can be externally controlled by introducing a shorting resistance between the emitter and the underlying base. In this case the current gain is prevented from rising rapidly and will be rising slowly as the current through a device rises.

At high temperatures the shorting dots are still effective for better high temperature operation of the device. The requirements for these are as follows. J_2 has a higher leakage current which will cause higher lateral voltage drops in the base on being collected by the shorting dots. The efficiency of J_3 rises at lower currents and therefore lower voltages are required to turn the emitter on effectively. Thus in working out the spacings between the dots these two factors have to be taken into account. The variation of α_{NPN} at higher currents, after the device switches on, is of little interest from high voltage point of view.

The reverse is true for α_{PNP}. Without shorting dots γ the emitter efficiency of PNP section rises to high values at quite low currents even at room temperature. Therefore the low current end is of little interest and what matters is the variation of peak value with temperature. It was shown that the main effect is an increase in L_{pb} with temperature.

This section represent the results of current gain measurements for some sample thyristors with and without shorted emitters from the same silicon slice resistivity.

5.2. Method of Measurements.

Measurements of current gain values were made by

the method described in previous sections (3 & 4). A number of new devices were measured and some details of their design where known are quoted in table (No. 2).

They were gold doped devices from the same material and diffusion batch, but have been processed with and without shorted emitters.

The f_{pnpt} has calculated from Pritchard's (1952) formula.

$$f_{pnpt} = \frac{1.22\ Dp}{\pi W_n^2}$$

5.3 Results and Discussion.

For a given constant temperature reading the effective alpha was taken for various frequencies of the small ac signal. The dc conditions of the thyristor were set by measuring the anode current and anode-cathode voltage. The anode-cathode voltage was kept constant and the effective alpha measured for number of different anode currents and plotted on a graph. The calculated values of α_{pnp0} and α_{npn0} the current gains of two transistor sections and their sum α_{t0} plotted versus anode current. Then the temperature setting was changed and the whole series of experiments was repeated and the calculated values of

Device No.	Slice diameter	Resistivity of silicon slice	Slice thickness	Depth of n-base	Depth of p(Ga)diff	Depth of Au/sb	V_{BO}	f_{pnpt}
	cm	Ω cm	μm	μm	μm	μm	V	KHZ
6 (shorted)	2.5	4-10	250	134	57.5-58.75	42.5-45	300-550	21
7 "	"	"	"	"	"	"	"	"
8 "	"	"	"	"	"	"	"	"
9 "	"	"	"	"	"	"	"	"
10 (not shorted)	"	"	"	"	"	37.5-40	"	"
11 "	"	"	"	"	"	"	"	"
12 "	"	"	"	"	"	"	"	"
13 "	"	"	"	"	"	"	"	"

TABLE (NO. 2)

α_{pnp0} and α_{npn0} plotted as a function of temperature as well as α_{t0} the sum alpha.

The measured V_{BO} the breakover voltage under two-terminal conditions,is also plotted as a function of temperature. Figures (5-1) to (5-20) represents a whole group of graphs for devices No. 6 to 13.

The variation of gate firing current as a function of anode current and temperature is presented in tables 3 to 8 in tabulated form.

Current gain measurement of above devices showed an almost similar variation with frequency. The temperature operation and variation of current gains, specially α_{npn0} is almost the same for devices with and without shorted emitters except for device No.12 which has higher α_{npn0}. At high temperature (100°C) these values are much closer than room temperature as shown in figure (5-21), histogrammatic diagram of α_{npn0}. Then it was thought that shorted emitter devices are conducting in the area of gate between gate contact and the nearest shorting dot. An alternative is that the current gain of NPN transistor section may have been controlled by adjustment of silicon resistivity and thickness by means of introducing some acceptable impurity (gold) to the basic silicon over the whole operating temperature range (20 to 150°C), in order to improve dV/dt performance of the device.

For devices without shorting dots the breakover voltage (V_{BO}) decreases as temperature increases. This is expected since the device switches by injection due to increased current carried by junction J_2. For devices with shorted emitter, the breakover voltage was found to be constant or to slightly increase with increasing temperature. This was thought to be due to avalanche breakdown which has a small temperature coefficient.

The gate firing current as expected, due to increased minority carrier current with temperature, decreases as the temperature rises. It was seen that gate firing current required to trigger the devices without shorting dots to conduction is less than required for shorted emitters. This increased gate current can be controlled by varying gate contact area, alloying temperature, p-type basewidth, etc. The calculated f_{pnpt} values agrees reasonably well with the measured value of f_{pnp} for all devices.

Gate switching characteristics of devices with and without shorted emitter.

Device No.	V_{AK} V	Temperature = 20°C I_A/I_G (mA)	I_{AS}/I_{GS}
6	200	10/62 - 15/66 - 20/68 - 25/69 - 30/70	35/71.5
7	200	20/93 - 25/97 - 30/100 - 35/103 - 40/105	50/110
8	200	25/89 - 30/91 - 35/93 - 40/94 - 44/96	55/105
9	200	7/35.5 - 10/37 - 12/38 - 14/38.5 - 16/39	17.5/39
10	150	7/27 - 10/30 - 13/32 - 15/32.5 - 17/33	17.5/34
11	200	20/56.5 - 25/59 - 30/60.5 - 35/61.5 - 38/62	40/64
12	200	25/32.5 - 30/34.5 - 35/36.5 - 40/37.5 - 44/38.5	55/44
13	200	7/24.5 - 10/27 - 13/28.5 - 15/29 - 18/30	20/31

TABLE (NO. 3)

I_A = Anode dc current.

I_{AS} = Anode switching current.

I_G = Gate firing current.

I_{GS} = Gate switching current.

Gate switching characteristics of devices with and without shorted emitter.

Device No.	V_{AK} V	Temperature = 60°C I_A/I_G (mA)	I_{AS}/I_{GS}
6	200	6/44 - 8/46 - 10/47 - 12/48 - 14/50 —	18/52
7	200	10/68 - 15/72.5 - 20/76 - 25/78 - 30/80 —	36/81.5
8	200	15/64 - 20/66 - 25/68 - 30/71 - 35/75 —	43/78
9	150	4/27 - 6/29.5 - 8/31 - 10/32.5 - 12/33 - 14/34	17/35
10	150	4/16.5 - 6/19 - 8/21 - 10/22.4 - 12/23 —	13/23.5
11	200	8/30 - 10/32 - 12/34 - 14/36 - 18/37.5 - 25/40	31/43
12	200	15/19 - 20/21 - 25/22.5 - 30/24 - 35/25 —	42/26
13	150	4/16 - 6/18 - 8/19.5 - 10/21 - 12/22 - 14/22.5	17.5/23

TABLE (NO. 4)

I_A = Anode dc current.

I_{AS} = Anode switching current.

I_G = Gate firing current.

I_{GS} = Gate switching current.

Gate switching characteristics of devices with and without shorted emitter.

Device No.	V_{AK} V	Temperature = 80°C I_A/I_G (mA)	I_{AS}/I_{GS}
6	200	6/38 - 8/40 - 10/41 - 12/41.5 - 14/42.5 —	17/43
7	200	10/60 - 15/63 - 20/65.5 - 22/66 - 25/67 —	30/69
8	200	15/58 - 20/60 - 25/62 - 30/64 - 35/65 —	40/67
9	150	4/23 - 6/25 - 8/27 - 10/28 - 12/29 - 14/29.5	15/30
10	150	4/13 - 6/15 - 8/17 - 10/18 - 12/19 —	13/19.5
11	200	8/26 - 10/28 - 12/29.5 - 14/31 - 18/33 - 25/35	29/36
12	200	15/17 - 20/18.5 - 30/21 - 35/22 — —	37/22.5
13	150	4/13 - 6/15 - 8/17 - 10/18 - 12/19 - 13/20	14/21

TABLE (NO. 5)

I_A = Anode dc current.
I_{AS} = Anode switching current.
I_G = Gate firing current.
I_{GS} = Gate switching current.

Gate switching characteristics of devices with and without shorted emitter.

Device No.	V_{AK} V	Temperature = 100°C I_A/I_G (mA)	I_{AS}/I_{GS} (mA)
6	200	6/33 - 8/34.5 - 10/35.5 - 11/36 - 12/37 —	14/38
7	200	10/51 - 15/55 - 17/56 - 20/57 - 22/57.5 —	24/58
8	200	15/51 - 20/52.5 - 25/53.5 - 30/55 - 35/56 —	37/58
9	150	4/20 - 6/21.5 - 8/23.5 - 10/24 - 12/25 —	13/25.5
10	150	4/10.5 - 6/12 - 8/14 - 10/15 - 12/16 —	13/16.5
11	200	8/21 - 10/23 - 12/25 - 14/26 - 18/28 - 25/30	28/30.5
12	200	15/14 - 20/15 - 25/17 - 30/18 - 32/18.5 —	33/19
13	150	4/10.5 - 6/12.5 - 8/14 - 10/15.5 - 12/16.5 - 13/17	14/17.5

TABLE (NO. 6)

I_A = Anode dc current.
I_{AS} = Anode switching current.

I_G = Gate firing current.
I_{GS} = Gate switching current.

Gate switching characteristics of devices with and without shorted emitter.

Device No.	V_{AK} V	Temperature = 120°C I_A/I_G (mA)	I_{AS}/I_{GS} (mA)
6	200	6/27 - 8/29 - 10/29.5 - 11/30.4 - 12/31 —	14/32
7	200	10/44 - 15/47.5- 17/48 - 20/49 - 22/49.5 —	22/49.5
8	200	15/42 - 20/43 - 25/44 - 30/45 - 33/45.5 —	35/46
9	150	4/15 - 6/18 - 8/20 --10/21 - 12/21.5 - 13/22	14/22
10	150	4/6 - 6/8 - 8/10 - 10/1.8 - 12/12.5 —	15.5/14.5
11	200	8/16 - 10/18 - 12/19.5 - 14/20.5 - 18/23 - 25/25	31/25.5
12	200	15/10 - 20/12 - 25/13.5 - 30/14 - 33/14.5 —	35/15
13	150	4/8.5 - 6/9.5 - 8/11 - 10/12 - 12/13 - 14/14	15/14.5

TABLE (NO. 7)

I_A = Anode dc current.
I_{AS}= Anode switching current.

I_G = Gate firing current.
I_{GS}= Gate switching current.

Gate switching characteristics of devices with and without shorted emitter.

Device No.	V_{AK} V	Temperature = 140°C I_A/I_G (mA)	I_{AS}/I_{GS}
6	200	6/18 - 7/20 - 8/22 - 10/23 - 12/24.5 - 13/26	15/27
7	200	10/36 - 15/40 - 17/40.5 - 20/41.5 - 22/42 —	22.5/42.5
8	200	15/33 - 20/35 - 25/36 - 30/37 - 32/37.5 —	33/38
9	150	4/0 - 6/11 - 8/13.5 - 10/16 - 12/17 - 14/18	16/19
10	150	(T=130°C)- 4/2 - 6/4 - 8/6.5 - 10/8 - 12/9	19.5/13.5
11	200	8/8 - 10/10 - 12/12 - 14/13 - 18/16 - 25/20	37/21
12	200	15/5 - 20/6 - 25/7 - 30/8.5 - 35/10 —	45/12
13	150	5.5/0 - 6/2 - 8/3.5 - 10/5.5 - 12/6.5 - 14/8	17/9

TABLE (NO. 8)

I_A = Anode dc current.
I_{AS} = Anode switching current.
I_G = Gate firing current.
I_{GS} = Gate switching current.

6. The Theory of Influence of Shorting Dots in PNPN Devices.

The theory and applications of emitter-shorts for improving the rate of rise of forward blocking voltage, dV/dt performance have been discussed by several authors.[10,20,23,30] As we have seen one effective method of improving dV/dt performance is to introduce a shorting resistance between the emitter and underlying base.

Two attempts are made to derive the influence of shorting dots, the first being the general case of resistance R, placed between the cathode and gate which simulates a shorting dot array. The second analyses current flow in a direct manner without using the general thyristor equations.

6.1 Resistance R between cathode and gate.

Experimental results showed that such a resistance stabilises the operation of thyristor. Recalling equations (1),(2),(3) and noting that $I_A=I_1=I_2$, $I_K=I_3=I_A+I_G$ these equations with assumption of $\left[\exp-\beta V_2 - 1\right] = -1$ it follows that:

$$I_A = I_{S_1}\left[\exp\beta V_1 - 1\right] + \alpha_{1I}\cdot I_{S_2} \tag{78}$$

$$I_A = \alpha_{1N} M_p I_{S_1}\left[\exp\beta V_1 - 1\right] + (M_p I_{ps} + M_n I_{ns}) + \alpha_{2N} M_n I_{S_3}\left[\exp\beta V_3 - 1\right] \tag{79}$$

$$I_K = \alpha_{2I} I_{S_2} + I_{S_3}\left[\exp\beta V_3 - 1\right] \tag{80}$$

Since there is an external shunt resistance between gate-cathode, figure (6-1), then the forward bias of gate-cathode will be

$$V_3 = I_{sh} R$$

but

$$I_{sh} = I_A + I_G - I_3$$

$$V_3 = R\left[I_A + I_G - \alpha_{2I} I_{S_2} - I_{S_3} (\exp\beta V_3 - 1)\right]$$

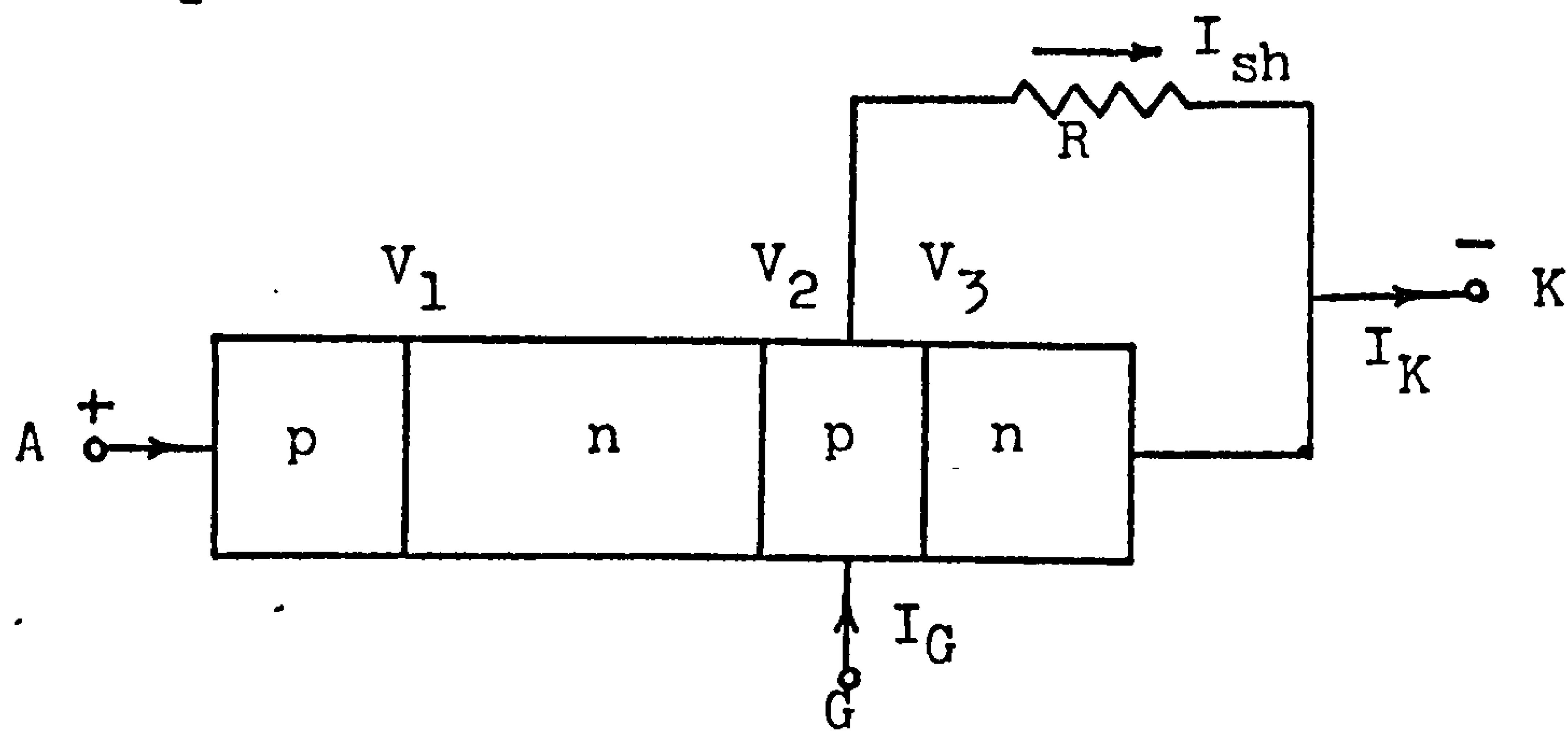


Figure (6-1) pnpn with external shunt resistance R.

For small V_3 we can write

$$(\exp\beta V_3 - 1) \approx \beta V_3 , \qquad \beta = \frac{q}{nkT} \tag{81}$$

therefore

$$V_3 = R(I_A + I_G - \alpha_{2I} I_{S_2} - I_{S_3}\beta V_3)$$

or

$$V_3 = \frac{R(I_A + I_G - \alpha_{2I} I_{S2})}{1 + R\beta I_{S_3}} \qquad (82)$$

Using equations (81) and (82) in (78), (79) and (80) after considerable manipulation, one obtains:

$$I_A = \frac{\hat{I}_{S2} - \alpha_{1N}\alpha_{1I} M_p I_{S2} + \beta RI_{S3}\left[\hat{I}_{S2} - I_{S2}(\alpha_{1N}\alpha_{1I} M_p + \alpha_{2N}\alpha_{2I} M_n) + \alpha_{2N} M_n I_G\right]}{1 - \alpha_{1N} M_p + \beta RI_{S3}\left[1 - \alpha_{1N} M_p - \alpha_{2N} M_n\right]} \qquad (83)$$

where $\hat{I}_{S_2} = M_n I_{CN} + M_p I_{CP}$ and $I_{S_2} = I_{CN} + I_{CP}$.

Break-over condition occurs when $I_A \longrightarrow \infty$, this has been shown to occur for $\alpha_{pnp0} + \alpha_{npn0} \cong 1$ a condition confirmed by our measurements, rather than $\alpha_{PNP} + \alpha_{NPN} = 1$ which occurs at higher currents. However the condition $I_A \longrightarrow \infty$ leads to:

$$1 - \alpha_{1N} M_p + \beta RI_{S_3}\left[1 - \alpha_{1N} M_p - \alpha_{2N} M_n\right] = 0 \qquad (84)$$

substituting $M = M_p = M_n$ and also

$$M = \frac{1}{1 - (V/V_B)^n}$$

equation (84) reduces to

$$\frac{V}{V_B} = \left[1 - \frac{\alpha_{1N} + \beta RI_{S_3}(\alpha_{1N} + \alpha_{2N})}{1 + \beta RI_{S_3}}\right]^{1/n} \qquad (85)$$

From equation (85) one can readily deduce two conditions for

$R = 0$ and $R \longrightarrow \infty$ so:

$$\frac{V}{V_B} = (1 - \alpha_{1N} - \alpha_{2N})^{1/n} \qquad R \longrightarrow \infty$$

$$\frac{V}{V_B} = (1 - \alpha_{1N})^{1/n} \qquad R \longrightarrow 0$$

Comparing these two terms shows that as R decreases the breakover also decreases, though this is admittedly small and agrees with experimental results.

Equation (83) could be simplified by substituting $M = M_p = M_n$ so that:

$$I_A = \frac{M I_{S2}(1 - \alpha_{1N}\alpha_{1I}) + \beta R I_{S3}\left\{M I_{S2}\left[1 - (\alpha_{1N}\alpha_{1I} + \alpha_{2N}\alpha_{2I})\right] + M\alpha_{2N} I_G\right\}}{1 - M\alpha_{1N} + \beta R I_{S3}\left[1 - M(\alpha_{1N} + \alpha_{2N})\right]} \qquad (86)$$

Well away from breakover where little avalanching occurs $M = 1$. With R open circuited we can then obtain

$$I_{AR\infty} = \frac{I_{S2}(1 - \alpha_{1N}\alpha_{1I} - \alpha_{2N}\alpha_{2I}) + \alpha_{2N} I_G}{1 - \alpha_{1N} - \alpha_{2N}}$$

$$\cong \frac{I_{S2} + \alpha_{2N} I_G}{1 - (\alpha_{1N} + \alpha_{2N})} \qquad (87)$$

Since $\alpha_{1N}\alpha_{1I} + \alpha_{2N}\alpha_{2I} \ll 1$

With $R = 0$ (86) becomes:

$$I_{ARO} = \frac{I_{S_2}(1 - \alpha_{1N}\alpha_{1I})}{1 - \alpha_{1N}} = \frac{I_{S_2}}{1 - \alpha_{1N}} \qquad (88)$$

Comparing equations (87), (88) it can readily be seen that:

$$\left| I_{AR\infty} \right| > \left| I_{ARO} \right| \qquad (89)$$

This has also shown by W.Fulop (private communication).

Of great importance is the decrease in I_A for decreasing R. Another point of interest is that I_{ARO} seems entirely independent of α_{2N} or α_{2I}, i.e, the transport properties of an npn transistor. This can be lead to increased stability of device.

6.2 Current flow with shorting dots.

Before investigating the influence of shorting dots we shall look at the situation of currents without shorting dots and gate open-circuited.

a. Without shorting dots.

The saturation current I_{c00} flows across a reverse biased collector junction as across any reverse biased junction. If the injected emitter current is I_K, then by transistor action α_{NPN} I_K passes across to collector and $(1 - \alpha_{NPN})I_K$ "remains behind" (current due to recombination in the base) in the base of npn section, which is equal to I_{c00n}

disapparance from the base of npn, figure (6-2).

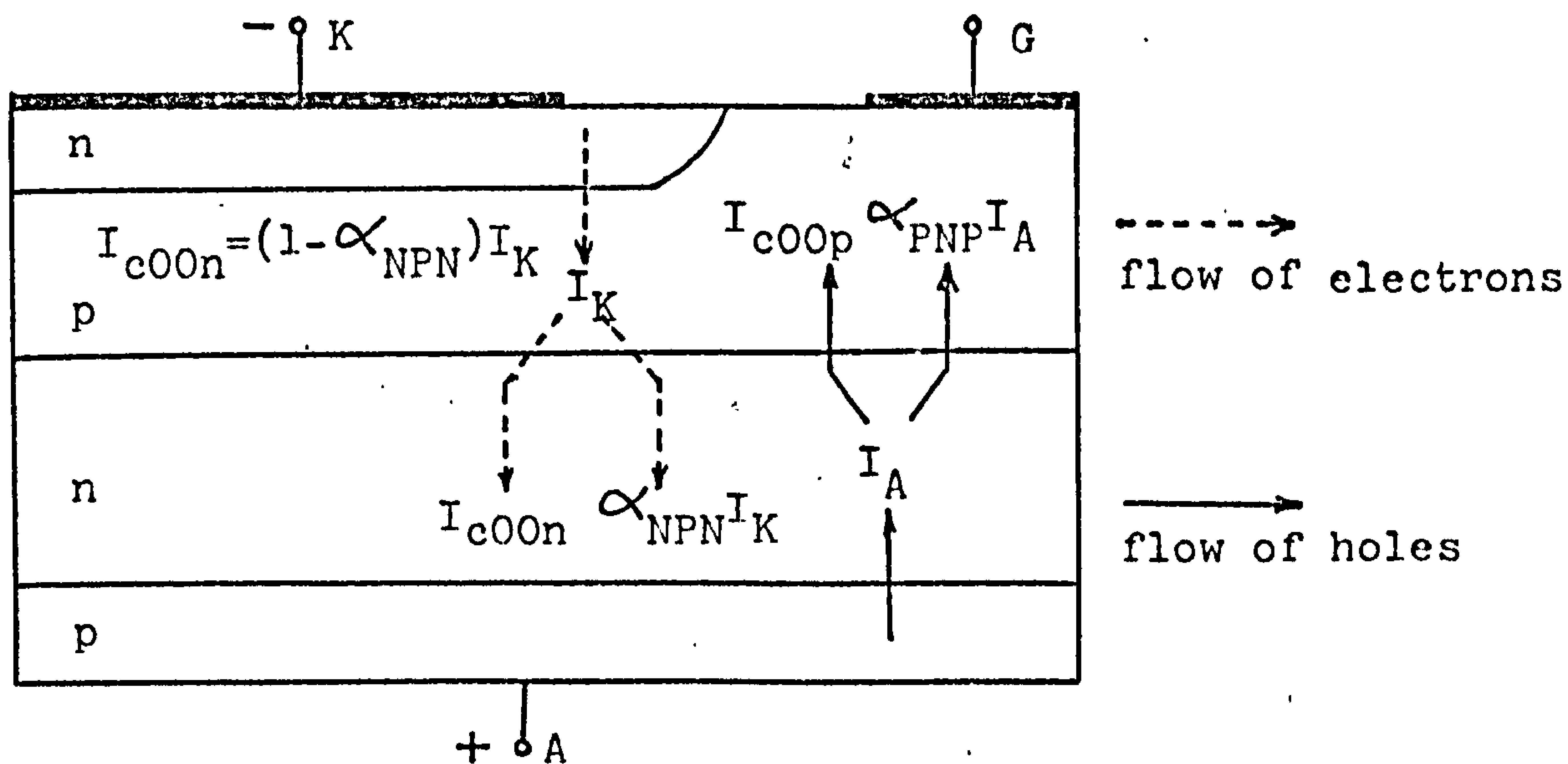


Figure (6-2) PNPN structure with current flow under forward bias.

$$I_K(1-\alpha_{NPN}) = I_{c00n}$$

i.e.

$$I_K = \frac{I_{c00n}}{1-\alpha_{NPN}} \tag{90}$$

Similarly for pnp transistor with correspoding α_{PNP} and I_A, hence the collected current by collector of device is:

$$I_A = \alpha_{PNP} I_A + I_{c00p} + \alpha_{NPN} I_K + I_{c00n}$$

$$I_A = \frac{I_{c00}}{1-\alpha_{PNP}-\alpha_{NPN}} \tag{91}$$

Since $I_A = I_K$ when $I_G = 0$ and $I_{c00} = I_{c00n} + I_{c00p}$.

Assuming the current contribution from the pnp side is small, therfore

$$I_{c00} \cong I_{c00n}$$

b. With shorting dots.

With a shorting dots the current across the device will be:

$$I_A = \frac{I_{c00}}{1-\alpha_{PNP} - \alpha_{eff}} \tag{92}$$

where α_{eff} is current-gain of npn transistor modified due to the shorting dot. Comparison with equation (91) shows that only α_{NPN} has replaced by α_{eff}. In order to evaluate α_{eff} consider figure (6-3),

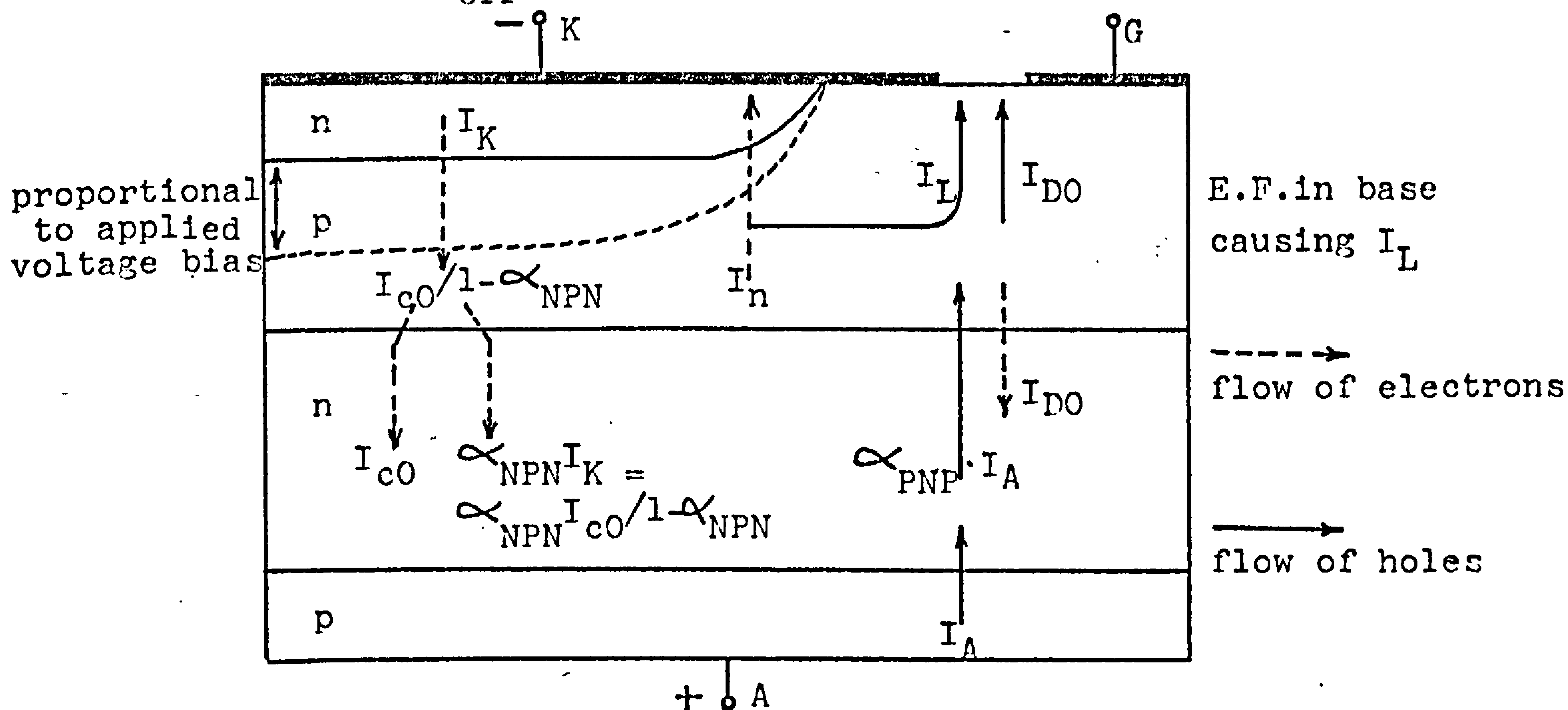


Figure (6-3) PNPN structure with shorted emitter with current flow under forward bias.

$I_{c0} = (1-A_S)I_{c00}$ is the saturation current across the collector junction of the npn section facing unshorted emitter.

$I_{D0} = A_S\ I_{c00}$ is the saturation current flowing across collector of npn opposite shorting dot.

I_{c00} = the total saturation current across the face of collector junction and A_S is the ratio of shorting dot area to total emitter area.

The emitter forward bias voltage will assume values schematically indicated by the dotted line in figure (6-3). This will cause a built-in electric field in the quasi-neutral p-base resulting in a leakage current I_L flowing as majority carrier hole current out of the shorting dot. This hole current I_L, must be compensated by an electron (particle) current out of the emitter. If this additional emitter electron is I_n then $\alpha_{NPN} I_n$ passes to the collector and $(1 - \alpha_{NPN})I_n$ remains behind in the npn base. Therefore

$$(1 - \alpha_{NPN})I_n = I_L \tag{93}$$

If we assume that all I's are positive and that the currents into the transistor are positive, then:

$$I_{EN} = I_n - \frac{(1 - A_S)I_{c00}}{1 - \alpha_{NPN}} - I_L - A_S I_{c00} \tag{94}$$

$$I_{CN} = (1 - A_S)I_{c00} + \frac{\alpha_{NPN}(1 - A_S)I_{c00}}{1 - \alpha_{NPN}} - \alpha_{NPN} I_n + A_S I_{c00} \tag{95}$$

Since $I_{EN} + I_{CN} = 0$ for $I_G = 0$ the equation (93) follows. Substituting equation (93) into (95), gives:

$$I_{CN} = \frac{I_{c00}(1 - A_S)}{1 - \alpha_{NPN}} - \frac{I_L \alpha_{NPN}}{1 - \alpha_{NPN}} + A_S I_{c00}$$

or:

$$I_{CN} = \frac{I_{c00}}{1 - \alpha_{NPN}} \left[1 - \alpha_{NPN}\left(A_S + \frac{I_L}{I_{c00}}\right) \right] \qquad (96)$$

Comparing this equation with equation (90), i.e. $I_{c00}/1 - \alpha_{NPN}$ one can clearly see the influence of A_S and I_L in reducing the current, therefore reducing the total current I_A.

Thus the effective alpha can be defined as;

$$1 - \alpha_{eff} = (1 - \alpha_{NPN}) / \left[1 - \alpha_{NPN}\left(A_S + \frac{I_L}{I_{c00}}\right) \right]$$

or:

$$\alpha_{eff} = \frac{\alpha_{NPN}\left[1 - \left(A_S + \frac{I_L}{I_{c00}}\right)\right]}{1 - \alpha_{NPN}\left(A_S + \frac{I_L}{I_{c00}}\right)} \qquad (97)$$

This clearly shows that:

$\alpha_{eff} \longrightarrow \alpha_{NPN}$ when $A_S \longrightarrow 0$ then $I_L \longrightarrow 0$, this is of course the case without shorting dot.

$\alpha_{eff} \longrightarrow 0$ if $A_S \longrightarrow 1$ then again $I_L \longrightarrow 0$, in this case the npn transistor tends to operate as a "pn" diode only.

Substituting equation (97) into (92) yields:

$$I_A = \frac{I_{c00}}{1 - \alpha_{PNP} - \alpha_{NPN}\left[\frac{1 - (A_S + I_L/I_{c00})}{1 - \alpha_{NPN}(A_S + I_L/I_{c00})}\right]} \qquad (98)$$

Equation (98) shows the effect of A_S and I_L in reducing the current which gives qualitatively good agreement with the previous analysis where R between gate and cathode reduced anode current, that is

$$|I_{AR\infty}| > |I_{ARO}|$$

6.3 Evaluation of I_L (Lateral hole current).

We earlier said that the rate of electron left behind in the p-base of npn transistor section is equal to the saturation current i.e.

$$\text{rate of electrons "left behind"} = I_{c00}$$

This shows that where $V_E(x) = V_{E00}$ the maximum value of emitter forward bias there is a perfect balance of the one dimensional ("vertical") current flow. For the device with shorting dot we can assume a distribution for emitter forward bias as shown in figure (6-3); this is indeed the case when $V_E(x) = V_{E0}$ only at the point x=0. At any other point x the rate of electrons left behind is smaller than at point x=0, because as one moves towards shorting dot from x=0, the emitter forward bias decreases. Hence the electrons injected by the emitter will be less than the case for maximum $V_E(x)$, and thus the rate of electrons "left behind" will be decreased.

Assuming I_{c00} flows at uniform density, then some electrons must be created in order to compensate the lower rate of electrons "left behind". These electron-hole pairs will be generated by "generation-recombination" in the p-base, thus the excess holes must be flow out of the base through a shorting dot, in order to keep charge neutrality in the base. These holes will constitute the leakage current I_L out of the base, therefore:

$$\frac{dI_L}{dx} = |I_{c00}| - |J_E(x)|(1 - \alpha_{NPN}) + |J_A| \alpha_{PNP} \tag{99}$$

where $I_{c00} = I_{c00n} + I_{c00p}$.

The injected emitter current I_E can be expressed in the usual way as Ebers and Moll (1954) as a function of emitter-base voltage $V_E(x)$:

$$J_E(x) = - \frac{J_{EO}}{1 - \alpha_{NPN}\alpha_{INPN}} \left[e^{qV_E(x)/kT} - 1 + \alpha_{NPN} \right] \tag{100}$$

where J_{EO} and I_{c00n}(current/area) are positive quantities.

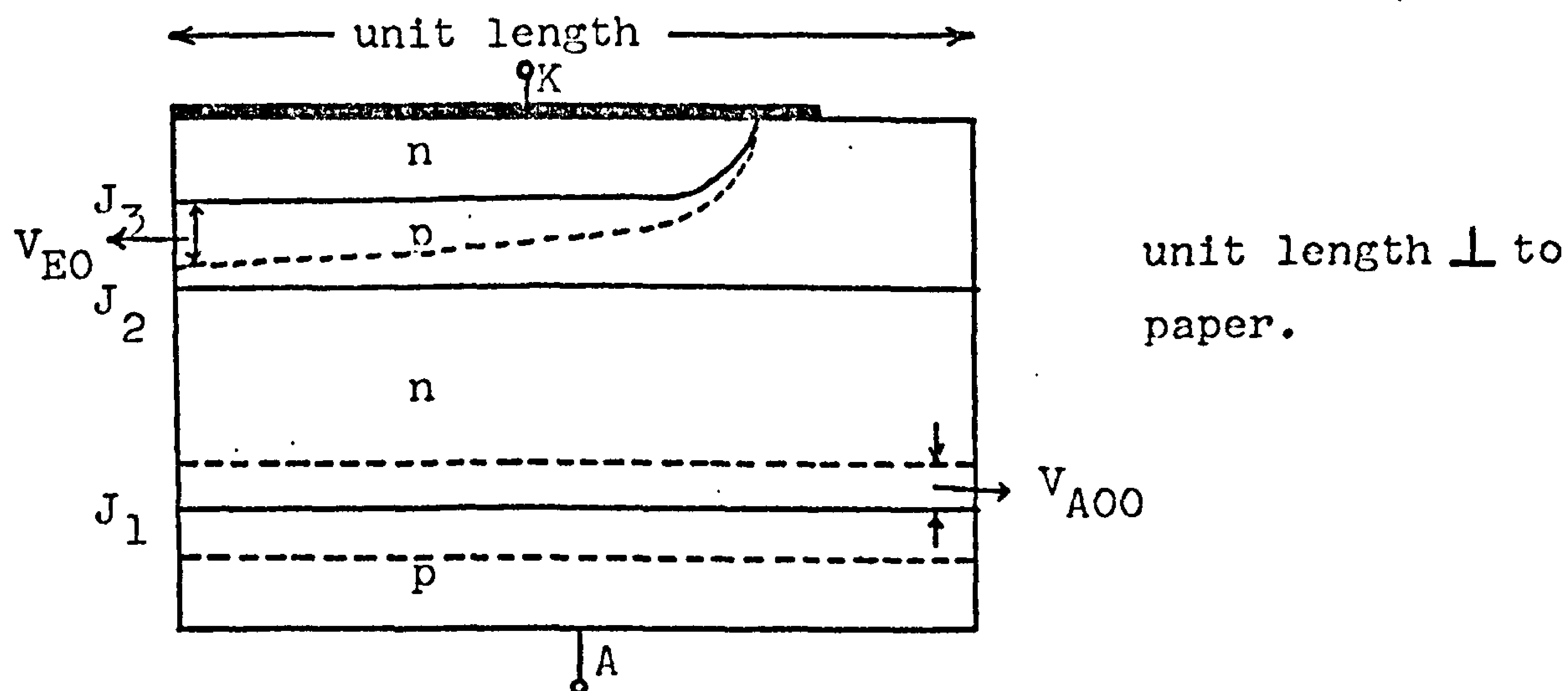


Figure (6-3) Schematic pnpn model under consideration.

Assuming a distribution for anode-forward bias (J_1 junction) as shown in figure (6-3), the current J_A will be:

$$\left| J_A \right| = \frac{I_{c00p}}{1 - \alpha_{PNP}} \tag{101}$$

substituting equation (100) and (101) into (99), after manipulation, one obtains:

$$\frac{dI_L}{dx} = \frac{I_{c00p}}{1 - \alpha_{PNP}} + I_{c00n} - \frac{J_{EO}(1 - \alpha_{NPN})}{1 - \alpha_{NPN}\, \alpha_{INPN}} \left[e^{qV_E(x)/kT} - 1 + \alpha_{NPN} \right]$$

Now letting

$$A = \frac{I_{c00p}}{1 - \alpha_{PNP}} + I_{c00n} + \frac{J_{EO}(1 - \alpha_{NPN})^2}{1 - \alpha_{NPN}\, \alpha_{INPN}}$$

$$B = \frac{J_{EO}(1 - \alpha_{NPN})}{1 - \alpha_{NPN}\, \alpha_{INPN}} \tag{102}$$

we will have:

$$\frac{dI_L}{dx} = A - B \exp qV_E(x)/kT \tag{103}$$

The current $I_L(x)$ causes a voltage drop given by

$$\frac{dV}{dx} = - \frac{\rho}{W} I_L(x) \tag{104}$$

where $\frac{\rho}{W}$ is a linear resistance of the base in the x direction and W is the width of p-base. Differentiating equation (103) with respect to x and substituting one gets:

$$\frac{d^2 I_L}{dx^2} = - \frac{qB}{kT} \exp \frac{qV_E(x)}{kT} \cdot \frac{dV}{dx}$$

$$= - \frac{q}{kT} \left(\frac{dI_L}{dx} - A\right) \cdot \frac{\rho}{W} I_L(x)$$

$$\frac{d^2 I_L}{dx^2} + \frac{q\rho}{kTW} \cdot I_L \cdot \frac{dI_L}{dx} - \frac{qA\rho}{kTW} \cdot I_L = 0 \qquad (105)$$

It is convenient to make the equation (105) non-dimensional, therefore noting that I_L is current/length, we will assume:

$$y = \frac{I_L(x)}{\frac{kT}{q\rho}} \qquad I_L(x) = \frac{kT}{q\rho} y$$

$$z = \frac{x}{W} \qquad x = z \cdot W$$

and

$$\frac{dI_L}{dx} = \frac{kT}{q\rho W} \cdot \frac{dy}{dz}$$

$$\frac{d^2 I_L}{dx^2} = \frac{kT}{q\rho W^2} \cdot \frac{d^2 y}{dz^2}$$

Substituting the appropriate terms into equation (105) yields:

$$\frac{d^2 y}{dz^2} + y \frac{dy}{dz} - \frac{q\rho W}{kT} \cdot A \cdot y = 0$$

and assuming $C = \frac{q\rho W}{kT} \cdot A$ we will get

$$\frac{d^2 y}{dz^2} + y \frac{dy}{dz} - Cy = 0 \qquad (106)$$

This is a self-consistent second-order non-linear differential equation defining hole current $I_L(y)$ as a function of $x(z)$.

Recalling equation (104) and differentiating once more with respect to x, one gets:

$$\frac{d^2V}{dx^2} = - \frac{\rho}{W} \cdot \frac{dI_L}{dx}$$

So that using our previous expression (103) for dI_L/dx we have:

$$\frac{d^2V}{dx^2} = - \frac{\rho}{W} \left(A - B \exp \frac{qV_E(x)}{kT}\right) \tag{107}$$

In equation (107) let $t = dV/dx$ then

$$\frac{d^2V}{dx^2} = t \frac{dt}{dV}$$

and we have:

$$t \frac{dt}{dV} = - \frac{\rho \cdot A}{W} + \frac{\rho \cdot B}{W} \exp \frac{qV_E(x)}{kT} \tag{108}$$

Integrating from the general point considered to $x = 1 - A_S$ using the fact that $V_E(1 - A_S) = 0$ and also $t(1 - A_S) = - \frac{\rho}{W} I_L(1 - A_S)$.

$$\tfrac{1}{2}t^2 = - \frac{\rho \cdot A}{W} \cdot V + \frac{\rho \cdot B}{W} \cdot \frac{kT}{q} \left[\exp \frac{qV_E(x)}{kT} - 1\right] + \frac{\rho^2}{2W^2} I_L{}^2(1-A_S)$$

$$\left(\frac{dV}{dx}\right)^2 = - \frac{2\rho A}{W} \cdot V + \frac{2\rho B}{W} \cdot \frac{kT}{q} \left[\exp \frac{qV_E(x)}{kT} - 1\right] + \frac{\rho^2}{W^2} I_L{}^2(1-A_S)$$

Assuming

$$D = \frac{2\rho_A}{W} \qquad \text{and} \qquad M = \frac{2\rho_B}{W} \cdot \frac{kT}{q}$$

$$\frac{dV}{dx} = \pm \left[M(\exp \frac{qV_E(x)}{kT} - 1) - D \cdot V + \frac{\rho^2}{W^2} I_L^2 (1 - A_S) \right]^{\frac{1}{2}}$$

$$\int_0^x \left[M(\exp \frac{qV_E(x)}{kT} - 1) - D \cdot V + \frac{\rho^2}{W^2} I_L^2 (1 - A_S) \right]^{-\frac{1}{2}} = \pm \int_0^x dx \tag{109}$$

and using the boundary condition $V_E(x) = V_{EO}$ and also $dV/dx = 0$ at $x = 0$, this is the complete solution in terms of an integral.

Computer Aided Solution of Equation (106).

The computer aided method of "Digital-Analogue Simulation" is used to solve the non-linear equation. Program uses the Merson's modification of the Runge-Kutta integration formula. This is a fourth order method which, can be made numerically stable by choosing a sufficient number of step-lengths and it permits reasonable economy of processing time by regulation of step-length according to integration error involved. The process uses the following equations (L. Fox, 1962).

$$Y_{n+1} = Y_n + \tfrac{1}{2}(K_1 + 4K_4 + K_5)$$

where Y_n is the known value of Y at time t_n

Y_{n+1} is the value obtained for Y at time $t_{n+1} = t_n + h$

$K_1 = \frac{1}{3} h \acute{Y}(t_n, Y_n)$

$$K_2 = \frac{1}{3} h\, \acute{Y}(t_n+1/3\, h,\ Y_n+K_1)$$
$$K_3 = 1/3\, h\, \acute{Y}(t_n+1/3\, h,\ Y_n+\tfrac{1}{2}K_1+\tfrac{1}{2}K_2)$$
$$K_4 = 1/3\, h\, \acute{Y}(t_n+\tfrac{1}{2} h,\ Y_n+3/8K_1+9/8K_3)$$
$$K_5 = 1/3\, h\, \acute{Y}(t_n+h,\ Y_n+3/2K_1 - 9/2K_3 + 6K_4)$$

in which h = time step = $t_{n-1} - t_n$

$\acute{Y}(t,a)$ is the value of Y' at solution time t, assuming that $Y(t) = a$.

The above formula specify the calculation of values for Y and the K's, given values for Y' at each value of time. At each attempt step carried out according to the above formula, the Merson truncation error formula is evaluated for each integration output;

$$e_Y = \frac{1}{5R_Y} (K_1 - 9/2K_3 + 4K_4 - \tfrac{1}{2}K_5)$$

where R_Y is a normalising parameter whose value depends on the error checking mode.

Figure (6-4) represents a block-diagram of the program used in terms of simple integrators, as is required in programming analogue computers. To represent figure (6-4), at the point "P" we may write:

$$y'' = -yy' + Cy$$

$$y'' + yy' - Cy = 0$$

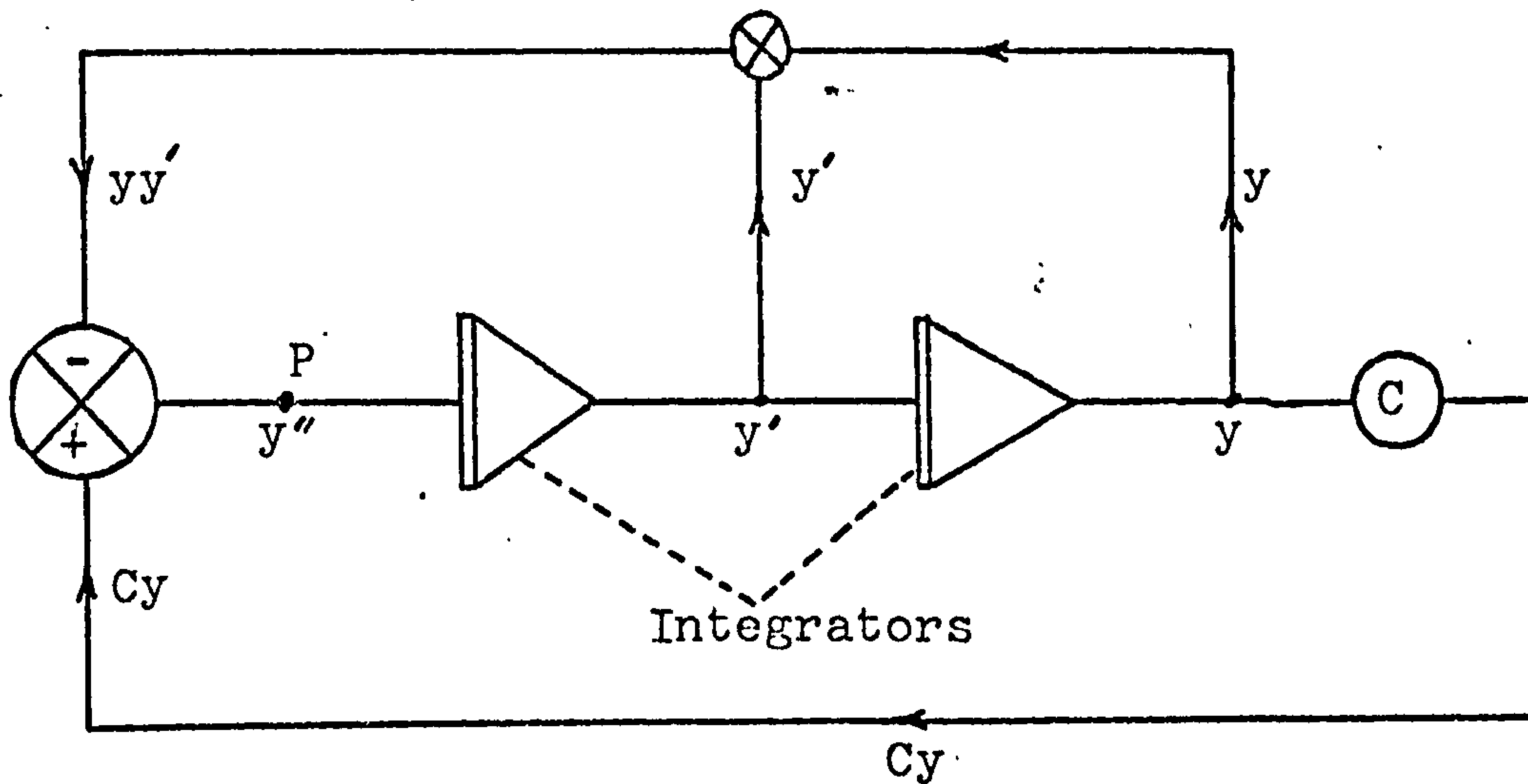


Figure (6-4) Simple block-diagram of program used.

The program is adopted to use the computer library manuals, D.E. Hirst, on CDC 7600 machine. The calculation takes about few seconds (4 sec.) on the CDC 7600.

Boundary Condition.

Recalling equation (99)

$$\frac{dI_L}{dx} = |I_{c00p}| + I_{c00n} - |J_E(x)|(1 - \propto_{NPN}) + |J_A| \propto_{PNP}$$

we can say that at the point x = 0 we have perfect balance between the rate of electron "left behind" in the base of npn and collector saturation current, that is:

$$I_{c00n} = |J_E(x)|(1 - \propto_{NPN})$$

Thus at this point with a good approximation we will have:

$$\frac{dI_L}{dx} = I_{c00p} + |J_A| \alpha_{PNP} = \frac{I_{c00p}}{1 - \alpha_{PNP}} \tag{110}$$

Also at this point the value of $I_L = 0$, i.e.

$$I_L = 0 \quad \text{at} \quad x = 0 \tag{111}$$

Hence with such an initial boundary condition and known parameters after calculating the constant C, we numerically solve the second-order non-linear differential equation of (106).

Figure (6-5) shows the variation of $y(I_L)$ as a function of $z(x)$ for various A_S at constant W for the non-linear equation of (106). This shows that as A_S increases $y(I_L)$ decreases at the point $(1 - A_S)$; this is expected since an increase in A_S for a fixed total emitter length will decrease the emitter junction area, and thus injected emitter electrons. Variation of I_L as a function of A_S at constant W is also shown in figure (6-6). The effect of A_S seems to be more pronounced than W at higher A_S in reducing the hole current I_L at the point $(1 - A_S)$.

Figure (6-7) illustrates the variation of $y(I_L)$ with $z(x)$ at constant A_S for set of different W. Of interest here is that the slope of curve increases with increasing W. The variation of I_L the hole current with respect to W is also shown in figure (6-8); this shows rapid increase for I_L as W becomes smaller. However the variation of

$I_L(1 - A_S)$ with A_S and W is tabulated in table (9).

$I_L\ (1 - A_S)$, $\mu A/cm$				
W (μm) \ A_S	0.0375	0.0675	0.125	0.20
15	84.3	80.6	75	68.1
20	82.5	78.7	73.7	66.8
30	80.0	77.5	72.5	65.6
40	78.7	76.5	71.8	65.4
50	78.0	75.6	71.2	65.2

Table (9)

7. Calculation of the Voltage Across the Junctions in the "OFF" Parts of the Thyristor Just After Turn-on.

One of the theoretical problems in the operation of thyristors is the voltage distribution in the two central base regions just after the device has switched on but before the plasma has had time to spread. With the overall voltage of the device having collapsed and the centre junction heavily forward biased in a very small switched-on region but being either reverse or at least not heavily forward biased over most of the device, this must lead to a very uneven voltage and field distribution in the two base regions. This could surely have a strong influence on the plasma spread as well as on the flow of majority carriers required as capacitive currents for charging up the central junction into forward bias in regions still switched-off.

The corresponding energy-band diagrams for the equilibrium, forward OFF state, and forward ON state are shown in figure (7-1a), (b), and (c) respectively. In equilibrium there is at each junction a depletion region with a built-in potential which is determined by the impurity doping profile. When a positive voltage is applied to the anode, junction J_2 will be reversed biased, while J_1 and J_3 will be forward-biased.

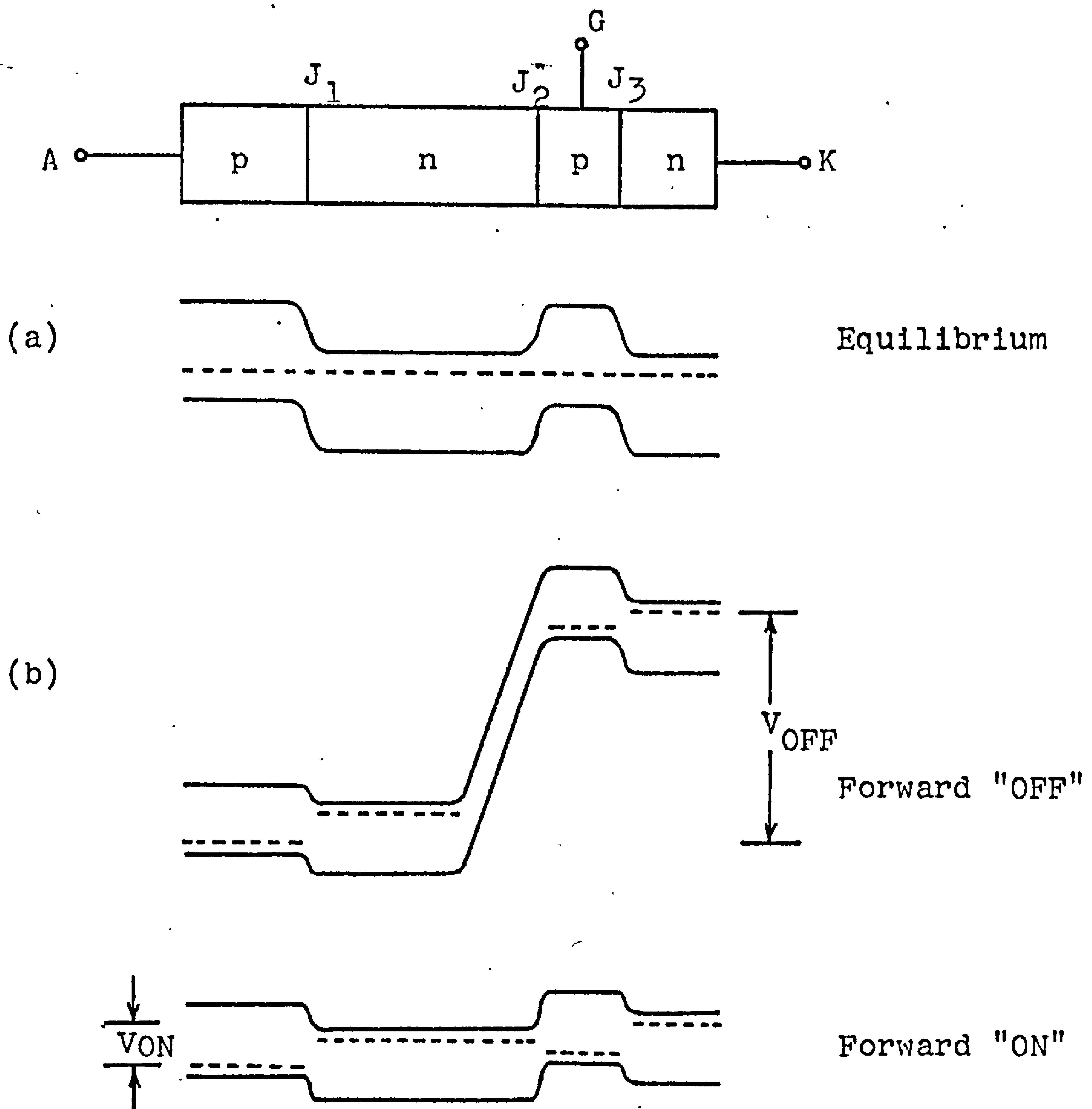


Figure (7-1) Energy band digrams of forward regions.

7.1 The Rubber Membrane Model.

In order to visualize the distribution of voltage in junctions, the rubber membrane is used. The rubber membrane used was of unstretched thickness 0.048 cm. and had a 15% stretch on a rectangular frame, the dimensions of which were large compared with the "electrode system". Figure (7-2) shows the frame with stretched rubber membrane and electrodes.

The rubber membrane was divided into two parts, one showing the potential distribution of the thyristor in the "ON" part of the device and second part showing the "OFF" part of the device just before plasma has had time to spread. In the "OFF" part of the device due to the presence of the cathode metallization, the voltage drop will be the same value as "ON" part, i.e. V_{ON}. The potential distribution just after the device switched "ON" in "OFF" part is shown in figure (7-3).

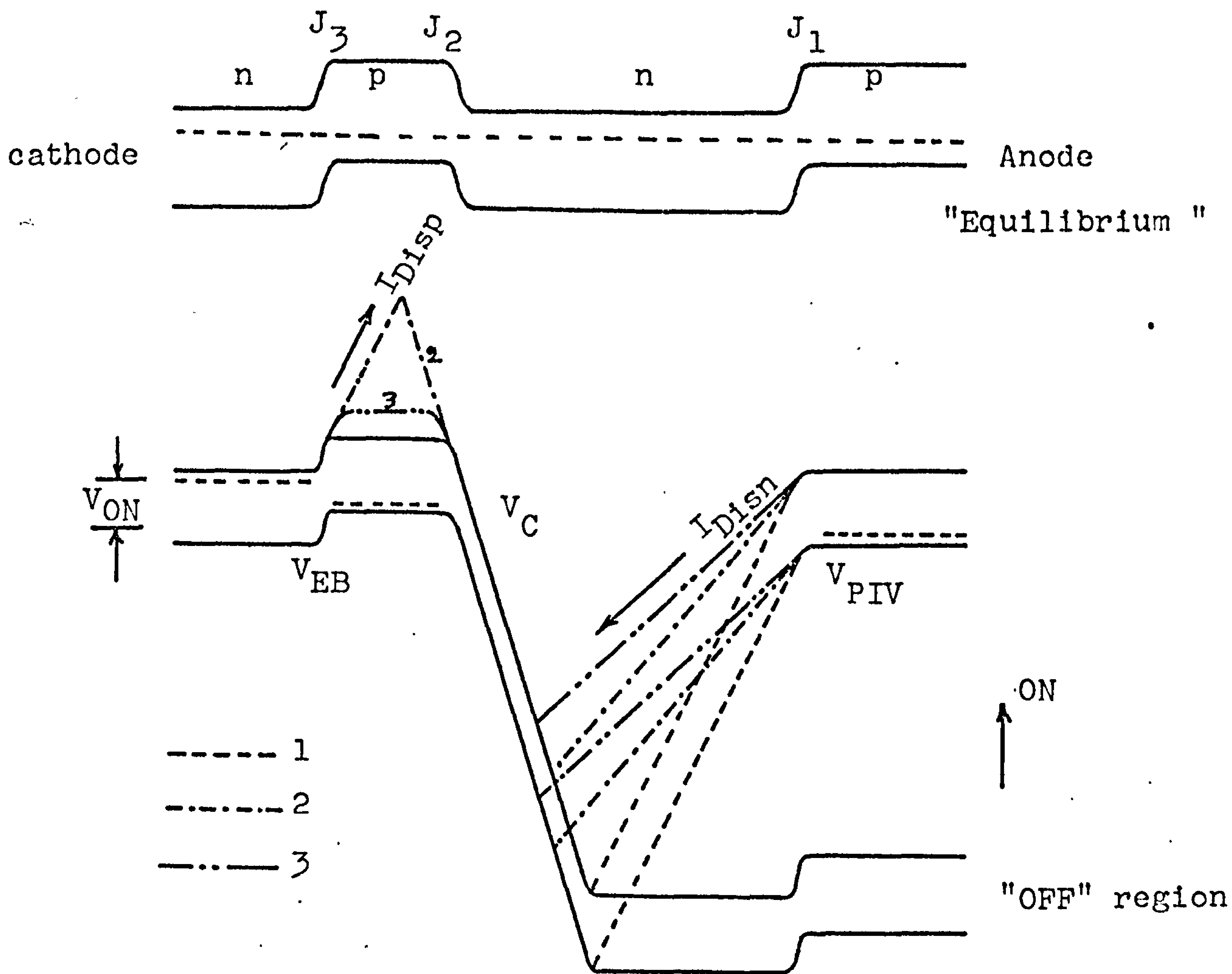


Figure (7-3) Potential distribution just after turn-on but before spreading.

Figure(7-2) The rubber membrane assembly.

What happens here is, the hole and electron displacement current ($I_{Disp} = I_{Disn}$) is discharging the V_{BO} junction and reverse biasing the PIV (Anode junction) and cathode junction "EB".

The maximum reverse voltage the cathode junction V_{EB}, can carry is probably less than 10V. This is because this junction has a very low breakdown voltage. So after the breakdown of the cathode junction the majority carriers will flow into the centre junction in order to reduce the reverse bias of the junction, and finally the junctions J_1 and J_2 will share the reverse voltage in the manner as shown in figure (7-4), which demonstrates the potential distribution at final stage after all events.

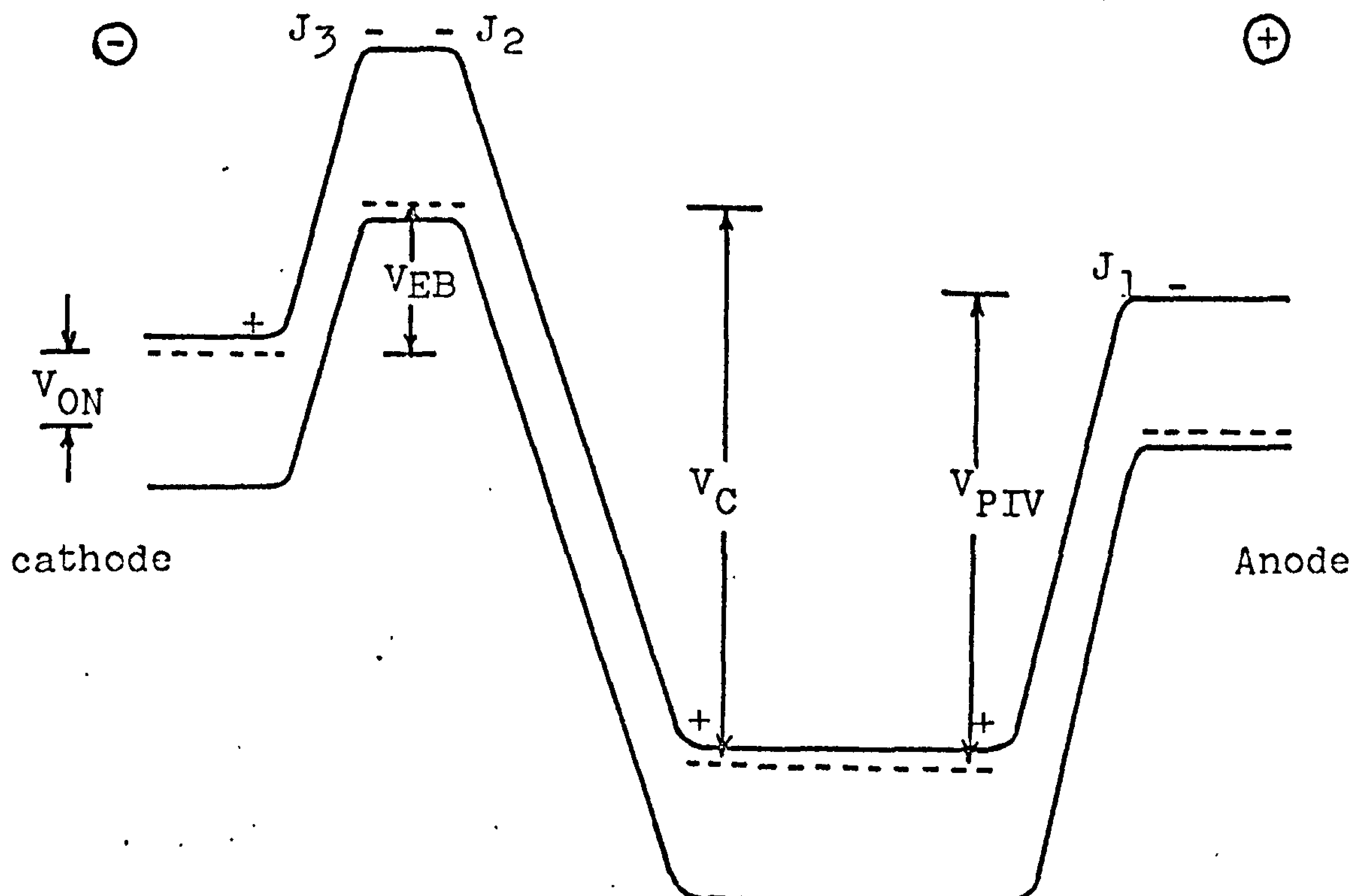


Figure (7-4) Distribution of potentials after settle-down of junctions.

Assuming that in the "OFF" portion of the thyristor the total voltages across the junction have remained at V_{OFF}, then:

$$V_{OFF} = V_{EB} + V_C + V_{PIV} \tag{112}$$

but the total voltage drop when all three junctions are reversed biased is:

$$V_{ON} = V_C - V_{PIV} - V_{EB} \tag{113}$$

Subtracting equation (113) from (112) one obtains:

$$V_{OFF} - V_{ON} = 2V_{PIV} + 2V_{EB}$$

therefore

$$V_{PIV} = \tfrac{1}{2}(V_{OFF} - V_{ON}) - V_{EB} \tag{114}$$

and also adding equation (112) to (113) will give:

$$V_{OFF} + V_{ON} = 2V_C$$

or

$$V_C = \tfrac{1}{2}(V_{OFF} + V_{ON}) \tag{115}$$

if V_{OFF} is very large then:

$$V_C = -V_{PIV} \tag{116}$$

7.2 Computer Simulation.

The exact numerical modelling approach recently has proved to be an efficient means of solving the general semiconductor transport equations accurately without the conventional restrictions such as locally neutral or space charge regions, constant mobilities, simplified doping profile, etc. This approch, involving the solution of the governing differential equation, was developed and applied for the first time by Gummel (1964).

Gummel described an efficient method for solving one-dimensional (1D) steady-state carrier transport equations. Later many authers published solution methods not only for small-signal and transient operation on 1D diode and transistor structures. With these methods it is possible to study how physical parameters such as doping profile, carrier mobilities, lifetimes, and geometry are related to the electrical behaviour of the device and to get a clear insight into high-level effects that are of growing importance for device optimization and design of accurate circuit models.

However, the basic equations governing the transport of carriers in semiconductor structurs are Poisson's equation, continuity equations for holes and electrons and current density equations.

$$\nabla^2\Psi = n - p - N \tag{117}$$

$$\nabla \cdot J_p = -R$$
$$\nabla \cdot J_n = R \tag{118}$$

$$J_p = -\mu_p(p\nabla\Psi + \nabla p)$$
$$J_n = \mu_n(n\nabla\Psi + \nabla n) \tag{119}$$

where

$\Psi(x)$ = electrostatic potential

$n(x)$, $p(x)$ = electron, hole density

$N(x)$ = net concentration of the ionised impurity atoms.

$J_n(x)$, $J_p(x)$ = electron, hole current density.

$R(x)$ = generation-recombination rate.

$\mu_n(x)$, $\mu_p(x)$ = electron, hole mobility.

We will introduce two variables defined by :

$$\phi_p = \exp\varphi_p$$
$$\phi_n = \exp(-\varphi_n) \tag{120}$$

where φ_p and φ_n are the hole and electron quasi-Fermi potentials:

$$\varphi_p = \Psi + \ln(p)$$
$$\varphi_n = \Psi - \ln(n) \tag{121}$$

Therefore the basic equations (117)-(118) reduce to three

elliptic partial differential equation in ψ, ϕ_p, ϕ_n (J.W. Slotboom, 1969):

$$\nabla^2\psi = \phi_n \exp(\psi) - \phi_p \exp(-\psi) - N \tag{122}$$

$$\nabla \cdot \left[\mu_p \exp(-\psi) \nabla \phi_p \right] = R \tag{123}$$

$$\nabla \cdot \left[\mu_n \exp(\psi) \nabla \phi_n \right] = R \tag{124}$$

with

$$J_p = -\mu_p \exp(-\psi) \nabla \phi_p$$
$$J_n = \mu_n \exp(\psi) \nabla \phi_n \tag{125}$$

Poisson's equation (122) is a second order non-linear elliptic partial differential equation in ψ and is linearized according to Newton's method. The procedure of obtaining a solution of this system of equations is the same as in the 1D Gummel method; first the non-linear Poisson's equation is solved, assuming ϕ_n and ϕ_p are known, and then each of the continuity equations is solved using the just calculated electric potentials from the Poisson's equation. This cycle is iterated until a sufficient accuracy is reached, figure (7-5).

Input data for the calculations are:

1. Doping profile for the thyristor.
2. Mobility as a function of doping and electric field.

3. Carrier generation-recombination law.

4. Applied voltage.

5. Geometry.

6. Right boundary condition.

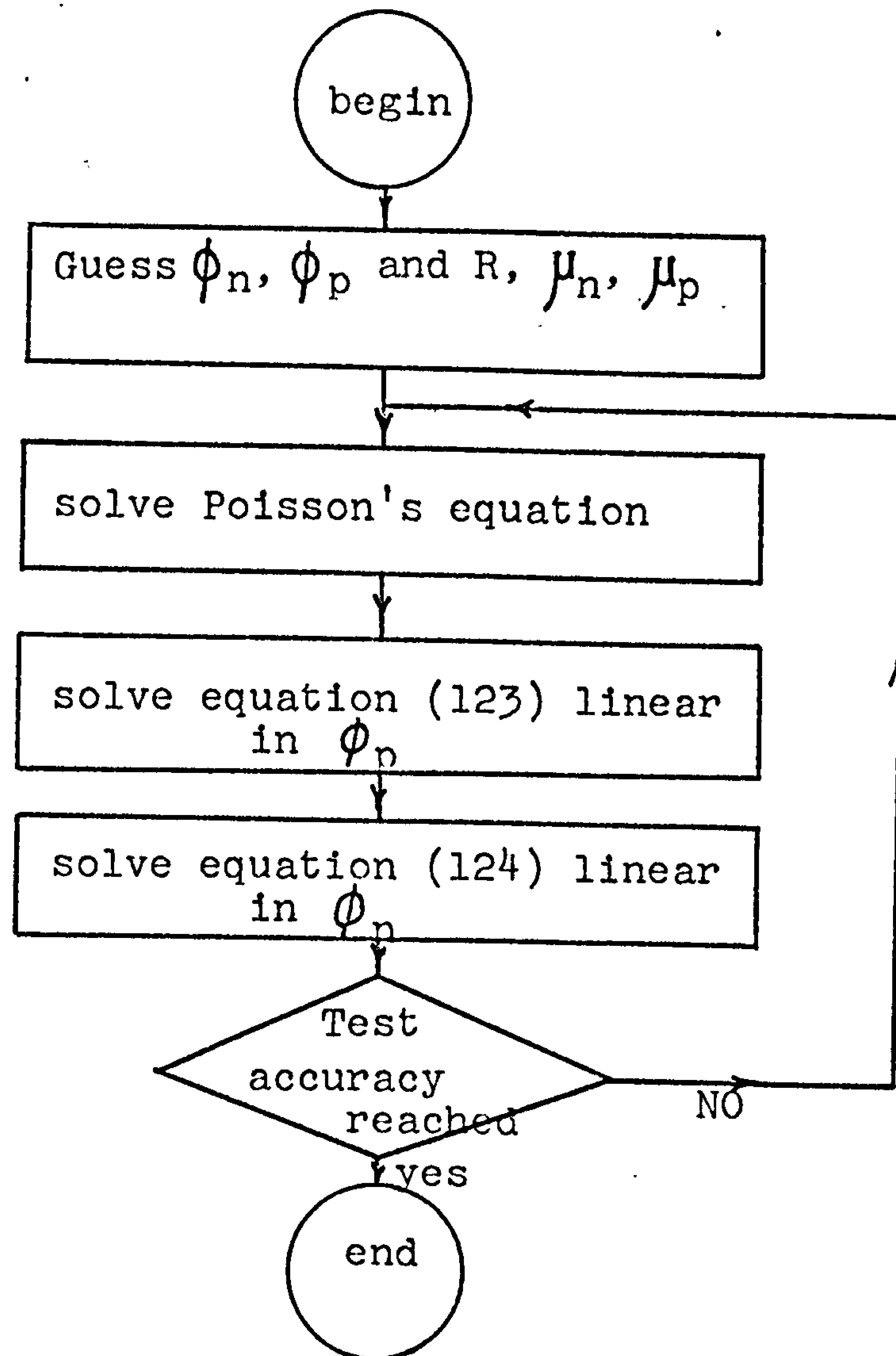


Figure (7-5) Flow chart of the iterative scheme.

Doping Profile.

The doping profile is calculated from the 1D Gaussian diffusion equation:

$$N = N_1 \exp\left[-(X_1-Re)^2/(eK)^2\right] - N_2 \exp(-X_2^2/(bK)^2) + N_3 + N_4 \quad (126)$$

where:

N_1 = surface density donors, concentration.

N_2 = surface density acceptors, concentration.

N_3 = epitaxial layer concentration.

N_4 = fourth layer concentration.

eK = diffusion constants, donors.

bK = diffusion constants, acceptors.

Re = flat top.

Mobility Model.

The carrier mobility variation with doping and electric field have been presented for silicon by D.M. Caughey and R.E. Thomas (1967),:

$$\mu = \left[\frac{\mu_{max} - \mu_{min}}{1 + (N/N_{ref})^{\alpha}} + \mu_{min}\right] \Big/ \left[1 + (E/E_c)^{\beta}\right]^{1/\beta} \quad (127)$$

where μ is mobility and N is doping density. β is constant, and equal to unity for holes and two for electrons.

The value of α and N_{ref} can be obtained from the slope and unity intercept of the straight line of; $\log(\mu_{max} - \mu)/(\mu - \mu_{min})$ versus log N.

$$(N/N_{ref})^{\alpha} = (\mu_{max} - \mu)/(\mu - \mu_{min})$$

Recombination Model.

The rate of recombination for non-equilibrium but steady-state condition is obtained from the Hall-Shockley, and Read model:

$$R = (pn - n_i)^2 / \left[\tau_{no}(p + p_1) + \tau_{po}(n + n_1) \right]$$

where

τ_{no}, τ_{po} = electron and hole lifetimes.

p_1, n_1 = hole and electron concentrations that would exist if the Fermi-levels were at the trap level.

For simplicity we will assume that the recombination centres are near the bandgap so:

$n_1 = p_1 = n_i$

therefore

$$R = n_i \frac{e^{\varphi_p - \varphi_n} - 1}{\tau_{no}(e^{\varphi_p - \psi} + 1) + \tau_{po}(e^{\psi - \varphi_n} + 1)} \qquad (128)$$

Note that, p and n are in units of n_i, the intrinsic carrier concentration, and ψ, φ_p and φ_n are in units of the Bolzmann voltage kT/q.

Boundary conditions.

For the discussion of the boundary conditions we will

treat a thyristor as a "hook transistor" as shown in figure (7-6).

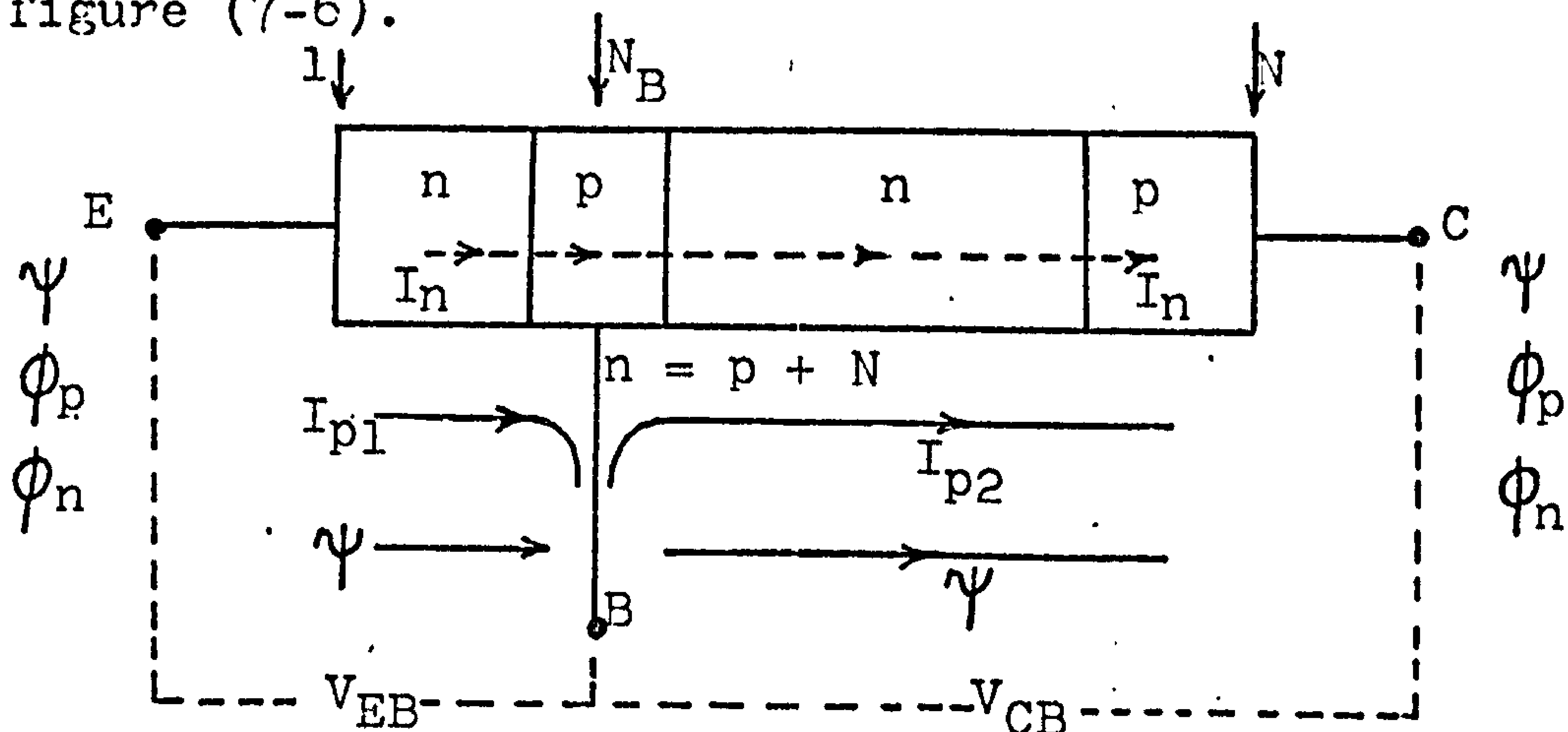


Figure (7-6) Schematic of npnp hook-transistor under consideration.

Boundary conditions are specified at points representing the emitter, base and collector contacts. Along the contacts infinite surface recombination velocities are assumed, or in other words, the carriers are assumed to be in thermodynamic equilibrium. Also it is assumed that the charge neutrality condition is valid along the contacts. Therefore the carrier densities at the emitter and collector are fixed.

$$pn = 1$$
$$n - p - N = 0 \tag{129}$$

It is convenient to take the base as reference point for the electrostatic potential. The potentials at the emitter and collector are then determined from the diffusion and applied potentials. In practice the approximation is

such, that the majority carrier density is equal to the net impurity density.

Emitter contact

$n = N$ $\quad p = 1/N \quad \therefore \quad \psi = \ln N + V_{EB}$

Base contact

$p = p$ $\quad n = p + N \quad \therefore \quad \psi = \ln|p|$

Collector contact

$n = N$ $\quad p = 1/N \quad \therefore \quad \psi = \ln N + V_{CB}$

The electron density may be solved for as a two point boundary value problem between emitter and collector on the assumption that no minority current flows out through the base contact. The hole density at the base is then fixed by the neutrality relationship (129). Electrostatic potential and hole current density are solved for in each region of the device separately, emitter to base $(1 - N_B)$ and base to collector $(N_B - N)$.

Poisson's Equation.

In solving the Poisson's equation we assume that, the quasi-Fermi potentials are known, along with a trial solution for the ψ and we consider how improved values for the ψ can be obtained. The equation to be solved is the second order differential equation:

$$\nabla^2\psi = \phi_n \exp(\psi) - \phi_p \exp(\psi) - N$$

The right-hand side represents the net space charge. To linearize such a non-linear equation we introduce the difference $\delta(x)$ between the available trial solution and the exact solution.

$$\psi_{exact} = \psi_0 + \delta \tag{130}$$

Then,

$$\delta'' - \delta\left[\phi_n \exp(\psi_0) + \phi_p \exp(-\psi_0)\right] = \left[-\psi_0'' + \phi_n \exp(\psi_0) - \phi_p \exp(-\psi_0) - N\right] \tag{131}$$

which can be written:

$$\nabla^2 \delta - A\delta = b$$

where

$$A = \phi_n \exp(\psi_0) + \phi_p \exp(-\psi_0) = n + p$$

$$b = -\nabla^2 \psi_0 + \phi_n \exp(\psi_0) - \phi_p \exp(-\psi_0) - N$$

$$= -\nabla^2 \psi_0 + n - p - N$$

ψ_0 = the ψ values of the former iteration.

The resulting linear equation for the correction $\delta(x)$ can be replaced by a set of difference equations. In this process, the left hand side forms a matrix M having non-zero elements in the main diagonal. Then we can write as:

$$M\delta = b \tag{132}$$

where δ and b are considered as column vectors. The solution δ is given by:

$$\delta = M^{-1}b \tag{133}$$

Therefore

$$\psi_{new} = \psi_0 + M^{-1}b \tag{134}$$

The linearized Poisson equation can be solved directly by a Gaussian elimination method. The coefficient matrices of the continuity difference equations depend upon the electric potential, which changes with each "outer" iteration. Therefore, it is necessary that independent of the values of the electric potential in each point, the difference equations are numerically stable, and that the iterative solution method of the individual equations is always convergent. These conditions will be satisfied by iteration solution methods, such as the method of successive over-relaxation (SOR), R.S. Varga (1962), superior to the method of direct matrix inversion technique, which exhibits slow convergence.

The difference equation at the point (i), figure (7-8) is

$$\left[4 + h^2\left\{\phi_{n_i}\exp(\psi_i) + \phi_{p_i}\exp(-\psi_i)\right\}\right]\delta_i = \delta_{i+1} + \delta_{i-1} + 2\delta_i - b_i \tag{135}$$

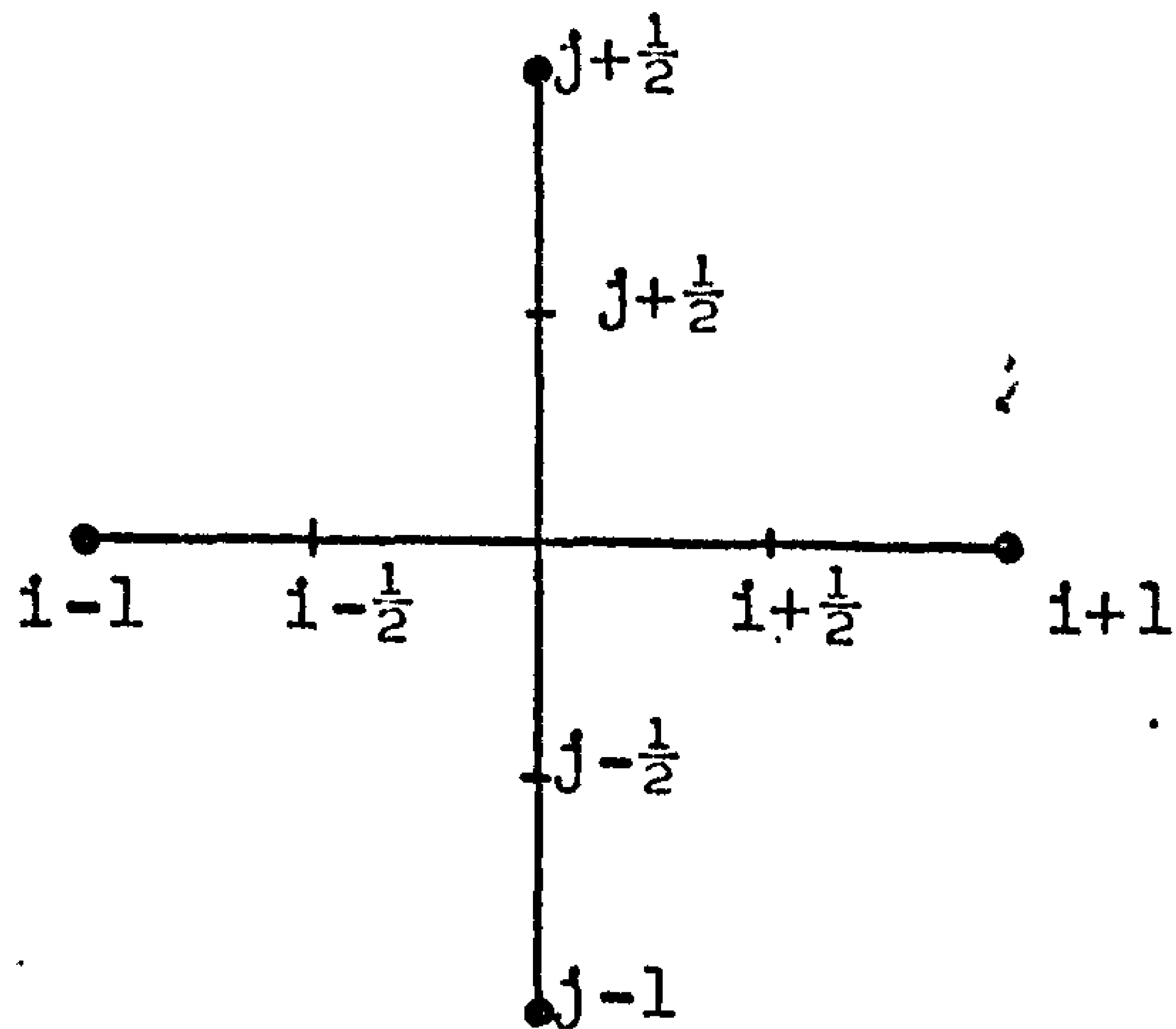


Figure (7-8) Mesh points.

where b is a known function of ψ, ϕ_n, ϕ_p and N, and h is the step length. Convergence of the SOR is always guaranteed by the diagonal dominance criterion. This method can be readily extend to two-dimensional solution (Slotboom, 1969). Therefore equation (135) can be written in the form of 2D as:

$$\left[4 + h^2\left\{\phi_{n_{i,j}}\exp(\psi_{i,j}) + \phi_{p_{i,j}}\exp(-\psi_{i,j})\right\}\right]\delta_{i,j} = \delta_{i+1,j} + \delta_{i-1,j} + \delta_{i,j+1} + \delta_{i,j-1} - b_{i,j}. \tag{136}$$

Continuity Equations.

We assume that the electric potential ψ is a known value as well as R, μ_p, μ_n and consider equations (123), (124). These sets of equations can be solved by direct integration, but the process will be very slow. The method is capable of extension to two dimensions but needs careful consideration since diagonal dominance is not guaranteed.

However these sets of difference equations can also be solved by method of SOR. At the point (i), figure (7-8), the difference equation for equation (123) is:

$$(a_{i+\frac{1}{2}} + a_{i-\frac{1}{2}} + 2a_i)\,\phi_{p_i} = a_{i+\frac{1}{2}}\,\phi_{p_{i+1}} + a_{i-\frac{1}{2}}\,\phi_{p_{i-1}} + 2a_i\,\phi_{p_i} - h^2 R_i \tag{137}$$

where $a = \mu_p \exp(-\psi)$

The difference equation for (124) is similar to (137) except that $a = \mu_n \exp(\psi)$. In extending to 2D equation (137) will be replaced by:

$$(a_{i+\frac{1}{2},j} + a_{i-\frac{1}{2},j} + a_{i,j+\frac{1}{2}} + a_{i,j-\frac{1}{2}})\,\phi_{p_{i,j}} = a_{i+\frac{1}{2},j}\,\phi_{p_{i+1,j}} + a_{i-\frac{1}{2},j}\,\phi_{p_{i-1,j}} + a_{i,j+\frac{1}{2}}\,\phi_{p_{i,j+1}} + a_{i,j-\frac{1}{2}}\,\phi_{p_{i,j-1}} - h^2 R_{i,j} \tag{138}$$

With the new value for ψ, and available quasi-Fermi potentials φ_p and φ_n one calculates the recombination rate R, and μ_n, μ_p at that point in the iteration cycle, therefore with values which all are known we return to the beginning for computing new ψ values and etc.

Example.

A procedure is adopted to use the Cranfield Institute of Technology programs (W. Love) to solve a numerical example

of a thyristor (hook-transistor) with a Gaussian doping profile, non-linear mobility variation and Shockley-Read recombination. Figure (7-9) shows the impurity profile of the device under consideration.

Figure (7-10) shows a plot of potential under zero bias condition. One recognizes the built-in junction voltages. Because of the impurity gradients in the base and emitter bulk regions, the potential also has a gradient to guarantee zero current flow.

Figure (7-11) shows a potential distribution for a specified bias conditions. One observes the corresponding changes of the junction voltages from those shown in figure (7-10).

The plot of electron density for the same bias conditions is shown in figure (7-12). Comparing the different bias conditions shows that the density of electrons in the active base region is increased, and also it is seen that electrons spread relatively widely into the second base. For higher value of V_{EB} the high injection of carriers has taken place and it seems that the p-base has been swamped by injected carriers.

Figure (7-13) shows the plot of hole densities. The viewing point has been shifted to the collector side of the device.

The lateral variations in current densities such as lateral current spreading, and potentials and their relationship with base current can not be taken into account in the 1D thyristor structurs. Two dimensional (2D) models are made to include these effects, which is under consideration.

The cut-off frequency is calculated in accordance with the charge control principle from a perturbation of the charge concentration and the resulting change in collector current:

$$f_T = (1/2\pi)\Delta I_C/\Delta Q_p$$

where ΔQ_p is the change in total stored hole charge. For example for the structure under consideration with the values:

$V_{EB} = -0.75$ V, $V_{CB} = 0.97$ V, $I_C = -1.15*10^7$ A/m^2

the value of cut-off frequency is equal to:

$$f_T = 1.92 \text{ GHZ}$$

8. Conclusion.

The results of individual experiments and theory are described throughout the work, but the main conclusions can be summarized as follows:

(i) It was shown that the method of three terminal current gain measurement by means of Fulop's method for small thyristors can also be used to measure current gains of the transistor components of high power thyristors. The method showed that the centre junction was reverse-biased and the two other junctions were forward biased, so that device is in the high impedance region. Calculating the dc component of currents from repeated measurements of small signal current gain factors of two transistor sections of the thyristor at several fixed current levels will yield the dc current gain of two transistor sections. It was then found that switching occurs when sum of small signal alpha's becomes unity rather than sum of dc alphas and agrees with Fulop's results. However with the known values for α_{npn0} and α_{pnp0} with their respective cut-off frequencies one gets some quantitative information on the dimensions and material properties of the thyristor.

(ii) The small signal current gains of two transistor sections were measured as a function of temperature from room temperature up to 140°C, the normal limit of operation. It was shown that from the curve of sum alpha versus temperature at a number of fixed anode currents, one can estimate qualitatively the variation of latching current, I_{BO} with temperature. This can be done by moving along a line of constant α_{t0}, as close to unity as possible and noting the interception with curves plotted for constant I_A. Measurement showed predictably the effect of gold-doping on the pnp current gain. This value was considerably lower because of reduced lifetime in the ungated base region.

In analysis of instability of pnpn devices the various conditions were investigated and it appears, that I_{c0}, the saturation current of centre junction plays a dominant role in the instability of pnpn devices with temperature. This has a large effect on the partial derivative of sum alphas with current which is always positive. The corresponding partial derivative with temperature, which is sometimes negative has much less influence.

(iii) The current gain measurements of sample thyristors

with and without shorted emitters from the same silicon resistivity showed almost similar variation with frequency. In the investigation of temperature dependence of alpha's, it appeared that α_{npn0} has almost the same variation for the devices with and without shorting dots and they were very close even at high temperatures (100°C). The break-over voltage V_{BO} of devices with no shorting dots showed an expected decrease with increasing temperature, while for the shorted emitter devices this value was found to be constant or even to slightly increase with increasing temperature. Aldrich and Holonyak result's confirms our results. Then it was thought that the shorted emitter device is conducting in the area of the gate between gate contact and the nearest shorting dot. Alternatively, the current gain of the npn transistor section may have been controlled by adjustment of silicon resistivity and the thickness by means of introducing some acceptable impurity (gold) to the basic silicon, in order to improve dV/dt performance of the device.

(iv) The theory of the influence of shorting dots in pnpn devices is outlined in a report by W. Fulop and was further developed. Firstly with a resistance R placed between the cathode

and gate to which a shorting dot could be likened, it was shown that anode dc current I_A will decrease for decreasing R. Another point of interest was that, anode current for the value of R = 0 seems entirely independent of α_{NPN} and α_{INPN}. An attempt was made to investigate the current flow in direct manner without using the thyristor equations. It was shown that the α_{eff} of npn transistor depends on A_S, the shorted area and I_L, the hole current out of the shorting dot. Analysing I_L, showed that this current varies with A_S and W, the p-base width and decreases with increasing A_S as well as W. It seems that the effect of A_S term dominates and decrease in I_L is mostly governed by A_S rather than W.

(v) The problem of voltage distribution in the two central base regions just after the device has switched on but before the plasma has had time to spread is investigated. It is shown that in the "OFF" portion of the thyristor all three junctions become reverse biased, just after turn-on but before spreading taken place. Since the cathode junction has a very low break-down voltage, probably less than 10 V, this junction breaks-down and majority carriers will flow into the centre junction. Finally the junctions

J_1 and J_2 will share the reverse voltage, and calculation shows that for a very large V_{OFF}, these two voltages are equal, i.e. $V_C = V_{PIV}$.

In order to have a better understanding of internal thyristor behaviour, the carrier transport equations for 1D thyristor structure are solved numerically in a way similar manner to that used by Gummel for a 1D continuity equations. The Boltzman statistics is used rather than Fermi statistics. Also boundary conditions are applied to the point of contacts. Then the potential distribution under zero and specified bias conditions was plotted. Also the electron current density as well as hole current density was plotted for a set of bias conditions.

It would be of interest to extend this technique to 2D model and also consider the time transient problems of pnpn devices in such a way.

R e f e r e n c e s

1. Moll, J.L., M. Tanenbaum, J.M. Goldey and N. Holonyak. "PNPN transistor switches", proc. IRE, vol. 44, pp. 1174-1182, 1956.

2. I.M. Mackintosh, "Three-terminal P-N-P-N transistor switches", IRE trans. on Electron devices, vol.5 pp. 10-12, 1958.

3. A.K. Jonscher, "P-N-P-N switching diodes", J. Electronics control, vol.3, pp. 573-586, 1957.

4. D.R. Muss, C. Goldberg, "Switching Mechanism in the N-P-N-P silicon controlled rectifier". IEEE trans on Electron devices. vol. ED-10, No. 2 , pp. 113-120, 1963.

5. W. Fulop, "Three Terminal Measurements of Current Amplification Factors of Controlled Rectifiers", IEEE trans. Electron Devices, vol. ED-10 No. 2 , pp. 120-133, 1963.

6. D.E. Crees, C.A. Hogarth, "Current Gain in PNPN Silicon controlled Rectifiers". J. Electronics and Control, vol. 14, pp. 481-498, 1963.

7. V.A. Kuzmin. "Theory of Voltage-current

characteristics of PNPN Semiconductor Devices". Radio and Elect. Phys., vol.-8, pp. 309-310, 1963.

8. Gibbons, J.F., "Critique of the Theory of PNPN Devices". IEEE. trans. Electron Devices, vol. ED-11, pp. 406-413., 1964.

9. A.K. Jonscher. "Principles of Semiconductor Device Operation". John Willey and sons, Inc., 1960.

10. F.E. Gentry et al, "Semiconductor Controlled Rectifiers", Prentic-Hall., 1964.

11. I.M. Mackintosh, "The Electrical Characteristics of Silicon PNPN Triodes", proc. of the IRE, vol-46, pp. 1229-1235, 1958.

12. S.M. Sze. "Physics of Semiconductor Devices", John Willy & sons, Inc., 1969.

13. J.A. Hoerni and R.N. Noyce. "PNπN Switches", IRE Wescon convention record, vol. 2, pt.3, pp. 172-175, 1958.

14. W. Fulop. "A Theoretical Investigation of the D.C. and Small Signal Characteristics of the Low Impedance Region of pnpn Diods and Triodes", Int. J. Electronics, vol-20, No.5, pp. 399-429, 1966.

15. A. Herlet and K. Raithal, "Forward Characteristics of Thyristors in the Fired State", Solid-state Electronics, vol-9, pp. 1089-1105, 1966.

16. R.A. Kokosa. "The Potential and Carrier Distributions of a pnpn Device in the ON State". Proc. IEEE., vol-55, No. 8, pp. 1389-1400, 1967.

17. G.D. Bergman, "The Gate-triggered Turn-on process in Thyristors". Solid-state Electronics, vol-8, pp. 757-765, 1965.

18. R.L. Longini, J. Melngailis "Gated Turn-On of Four Layer Switch", IEEE. Trans. on Electron Devices, vol.ED-10, pp. 175-185, 1963.

19. W.H. Dodson and R.L. Longini, "Probed Determination of Turn-on Spread of Large Area Thyristor". IEEE. Trans. on Electron Devices, vol. ED-13, No.5, pp. 478-484, 1966.

20. H.J. Ruhl, "Spreading Velocity of the Active Area Boundary in a Thyristor". IEEE. Trans. on Electron Devices, vol. ED-17, No.9, pp. 672-680, 1970.

21. R.W. Aldrich and N. Holonyak, "Two-Terminal Asymmetrical and Symmetrical silicon Negative Resistance Switches", J. Applied Physics, vol-30

No.11, pp. 1819-1825, 1959.

22. C.K. Chu, "Geometry of Thyristor Cathode Shunts", IEEE. Trans on Electron Devices, Vol. ED-17, No.9, pp. 687-693, 1970.

23. P.S. Radcrecht. "A Review of the Shorted Emitter Principle as Applied to PNPN Silicon Controlled Rectifiers"., Int. J. Electronics, vol. 31, No.6, pp.541-564, 1971.

24. I. Somos and D.E. Piccone, "Behaviour of Thyristors Under Transient Conditions", proc. IEEE, vol. 55, No. 8, pp. 1306-1311, 1967.

25. N. Mapham, "Overcoming Turn-On Effects in Silicon Controlled Rectifiers". Electronics, vol. 35, pp. 50-51 August 17, 1962.

26. B.V. Cordingley, "Improving the Turn-On Performance of High-power Thyristors", J. of Science & Technology, vol-38, No. 1, pp. 2-7, 1971.

27. D.I. Gray, "This SCR is not for Burning", Electronics, pp. 96-100, Sept. 30,1968.

28. W.M. Bullis, "Properties of Gold in Silicon", Solid-State Electronics, vol.9, pp. 143-168, 1966.

29. R.L. Pritchard, Proc. Inst. Radio Engrs, vol.40, pp. 1476, 1952.

30. P.S. Raderecht, "The Development of a Gate Assisted Turn-Off Thyristor for use in high Frequency Applications". Int. J. Electronics, Vol-36, No.3, pp. 399-416, 1974.

31. R.E. Smolyanski, Radiotekh. Elektron, No.9, pp. 1615-25, Sept. 1963.

32. P.S. Raderecht and C.A. Hogarth, "The Temperature Variation of the Parameters of Silicon Controlled Rectifiers", J. Electron. control, vol-17, pp. 145 -157, 1964.

33. D. Buhana , "Investigation of Current-Gain Temperature Dependence in Silicon Transistors", IEEE, Trans. on Electron Devices, vol. ED-16, No.1, pp. 117-123, 1969.

34. F.E. Gentry, "Turn-On Criterion for p-n-p-n Devices". IEEE. Trans. Electron Devices, vol. ED-11, pp. 74, 1964.

35. Y. Tokumaru, "Properties of Silicon Doped with Nickel", Japanese J. Applied Physics, vol-2, No.9, pp. 542-547, 1963.

36. P.S. Raderecht, Ph.D. Thesis, 1972, Brunel University.

37. H.K. Gummel, "A Self-Consistent Iterative Scheme for one Dimensional Steady state Transistor Calculations", IEEE Trans. Electron Devices, vol. ED-11, pp.455-465, 1964.

38. D.M. Caughey and R.E. Thomas "Carrier Mobilities in Silicon Empirically Related to Doping and Field", Proc. IEEE. (Corr.), vol-55, pp. 2192--2193, 1967.

39. R.N. Hall, "Electron-Hole Recombination in in Germanium", Phys. Rev. Vol-87, pp.387, 1952.

40. W. Shockley and W.T. Read, "Statistics of the Recombination of Holes and Electrons", Phys. Rev, vol. 87, pp. 835-842, 1952.

41. W. Fulop "Private Communication".

42. J.J. Ebers and J.L. Moll, "Large Signal Behaviour of Junction Transistors" Proc. IRE, vol-42, pp. 1773, 1954.

43. L. Fox, "Numerical Solution of Ordinary and Partial Differential Equations", Pergamon, 1962.

44. D.E. Hirst "Fortran Digital-Analogue Simulator Program", Brunel University, 1971.

45. J.W. Slotboom "Iterative Scheme for 1-and 2-Dimensional D.C. Transistor Simulation", Electronics letters, vol-5, No. 26, pp.677-678, 1969.

46. W.C. Un "M.Phil. Dissertation", Brunel University, 1974.

List of Symbols.

I_1, I_2, I_3	= Current through the junctions.
I_{S1}, I_{S2}, I_{S3}	= Saturation current of junctions when other two junctions are short-circuited.
I_A	= Anode dc current of SCR.
I_{AS}	= Anode switching current of SCR.
I_K	= Cathode dc current of SCR.
I_G	= Gate firing current.
I_{GS}	= Gate switching current.
I_{ns}, I_{ps}	= Saturation currents of collector junction of npn and pnp transistor sections, where $I_{S2} = I_{ns} + I_{ps}$
I_h	= Holding current.
I_t	= Turn-off current.
I_{Dis}	= Displacement current.
I_{BO}	= Breakover current under-two terminal operation.
I_F	= Forward current.
I_{B1}, I_{B2}	= The base current of pnp and npn transistor sections.
I_{C1}, I_{C2}	= The collector current of pnp and npn transistor sections.
I_{COB1}, I_{COB2}	= Saturation current of reverse biase junctions of pnp and npn transistor sections.
i_a	= ac anode current of SCR.
i_k	= ac cathode current of SCR.

I_{c0p}, I_{c00p} = Saturation current of collector junction of pnp transistor section.

I_{c0n}, I_{c00n} = Saturation current of collector junction of npn transistor section.

I_{c0}, I_{c00} = Saturation current of centre junction of SCR.

I_{D0} = Saturation current flowing across collector of npn section opposite shorting dot.

I_L = Hole lateral current out of shorting dot.

I_{CP}, I_{CN} = dc collector current of pnp and npn transistor sections.

V = Applied voltage.

V_{BO} = Breakover voltage under two- terminal operation.

V_B = Breakdown voltage of centre juction.

V_{EB}, V_3 = Cathode junction (J_3) voltage.

V_C, V_2 = Centre junction (J_2) voltage.

V_{PIV}, V_I = Anode junction (J_1) voltage.

α_{1N}, α_{PNP} = dc forward alpha for PNP section.

α_{2N}, α_{NPN} = dc forward alpha for NPN section.

α_{1NI} = dc inverse alpha of PNP section.

α_{2NI} = dc inverse alpha of NPN section.

α_{1N0}, α_{pnp0} = Low-frequency small-signal current gain factor of pnp transistor section.

α_{2N0}, α_{npn0} = Low-frequency small-signal current gain factor of npn transistor section.

α_{pnp}, α_{npn}	= Small-signal current gain factors of pnp and npn transistor sections.
α_{dc}	= dc current gain of SCR.
α_e	= Small-signal effective alpha of SCR.
α^0_{pnp0}	= Low-voltage value of α_{pnp0}.
α^0_{npn0}	= Low-voltage value of α_{npn0}.
α_{t0}	= The sum of small signal alphas.
α_{t00}	= Low voltage value of α_{t0}.
β	= Minority carrier transport factor.
γ	= Emitter efficiency.
f_p, f_{pnp}	= Cut-off frequency for pnp transistor.
f_n, f_{npn}	= Cut-off frequency for npn transistor.
$f_{(pnp)t}$	= Theoratical value of cut-off frequency for pnp transistor section.
V_S	= Spreading velocity.
E_g	= Band-gap energy.
N_B	= Backround doping.
W_{sc}	= Depletion layer width.
W_{B1}	= Base width of pnp transistor.
W_{B2}	= Base width of npn transistor.
W	= Base width of appropriate transistor.
D_p, D_n	= Diffusion constants for holes and electrons.
D_{pe}	= Diffusion constant of holes in emitter.
D_{nb}	= Diffusion constant of electrons in base.
τ_p, τ_{p0}	= Hole life-time.
τ_n, τ_{n0}	= Electron life-time.
t_r	= Rise-time.

a	= The thickness of each base.
L_p, L_n	= Diffusion length for holes and electrons.
L_{pe}	= Diffusion length for holes in emitter region.
L_{nb}	= Diffusion length for electrons in base region.
M_n, M_p	= Multiplication factors for electrons and holes.
A_S	= Ratio of shorting dot area to total emitter area.
ρ	= The resistivity of p-base region.
C_2	= Depletion layer capacitance.
J_0	= Emitter junction reverse saturation current density.
J_e	= Active area emitter current density.
$\psi(x)$	= Electrostatic potential.
$n(x)$, $p(x)$	= Electron, hole density.
$N(x)$	= Net concentration of the ionised impurity atoms.
$J_n(x)$, $J_p(x)$	= Electron, hole current density.
$R(x)$	= Generation-recombination rate.
$\mu_n(x)$, $\mu_p(x)$	= Electron, hole mobility.
φ_p, φ_n	= Hole, electron quasi-Fermi potentials.
N_1	= Surface density donors, concentration.
N_2	= Surface density acceptors, concentration.
N_3	= Epitaxial layer concentration.
N_4	= Fourth layer concentration.
eK	= Diffusion constants, donors.

bK	= Diffusion constants, acceptors.
Re	= Flat top.
p_1, n_1	= Hole and electron concentrations that would exist if the Fermi-levels were at the trap level.
n_i	= Intransic carrier concentration.
kT/q	= Boltzman voltage.
ΔQ_p	= The change in total stored hole charge.
T	= Absolute temperature.

GRAPHS.

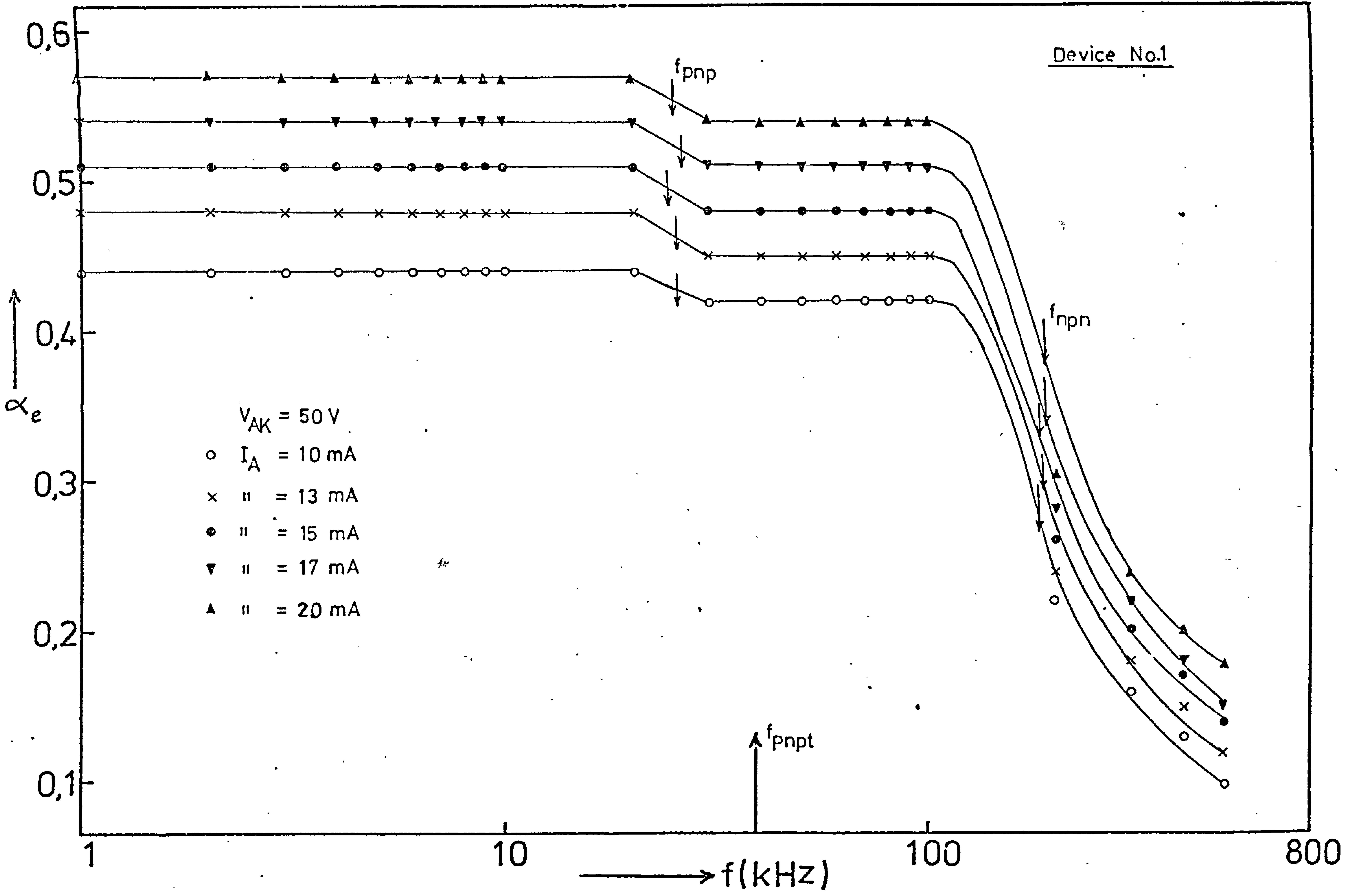


Figure (3-6) Frequency-response of current gain of a medium-power thyristor.

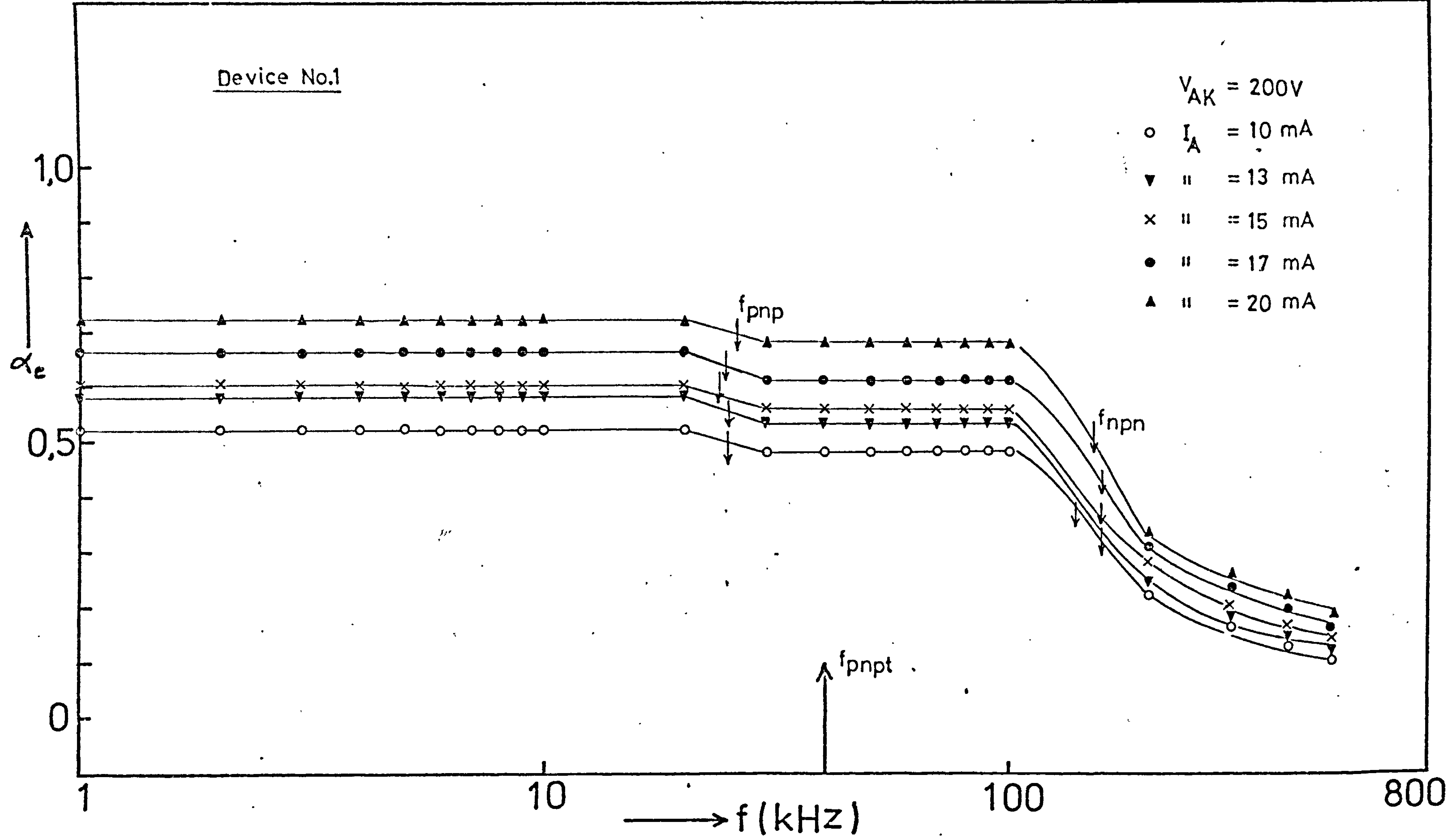


Figure (3-7) Frequency-response of current gain of a medium-power thyristor.

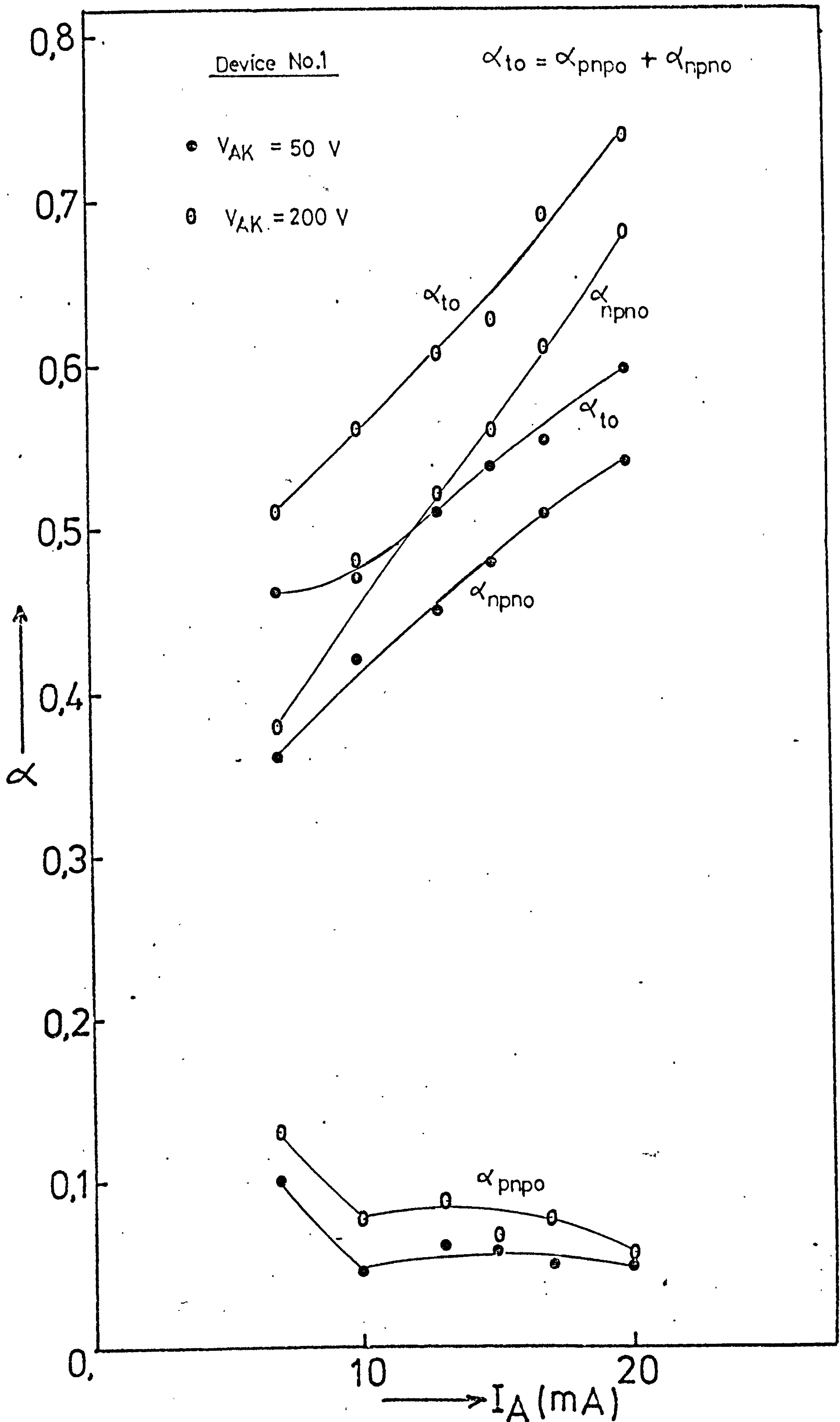


Figure (3-8) Current gain as a function of anode current for a medium-power thyristor.

Figure (3-9) The anode-cathode dc-current characteristics of medium-power thyristor.

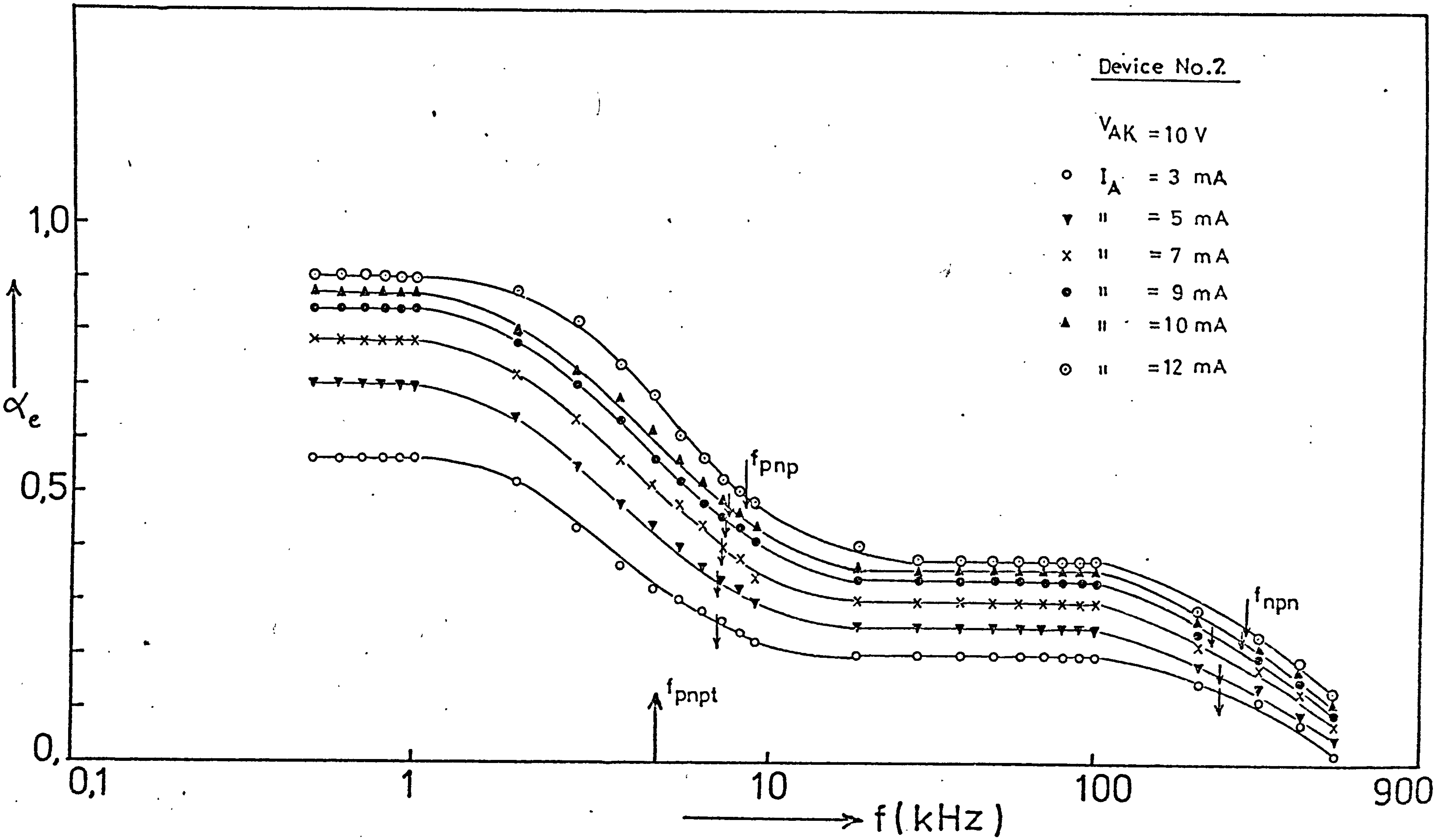


Figure (3-10) Frequency-responce of current gain of a high-power thyristor.

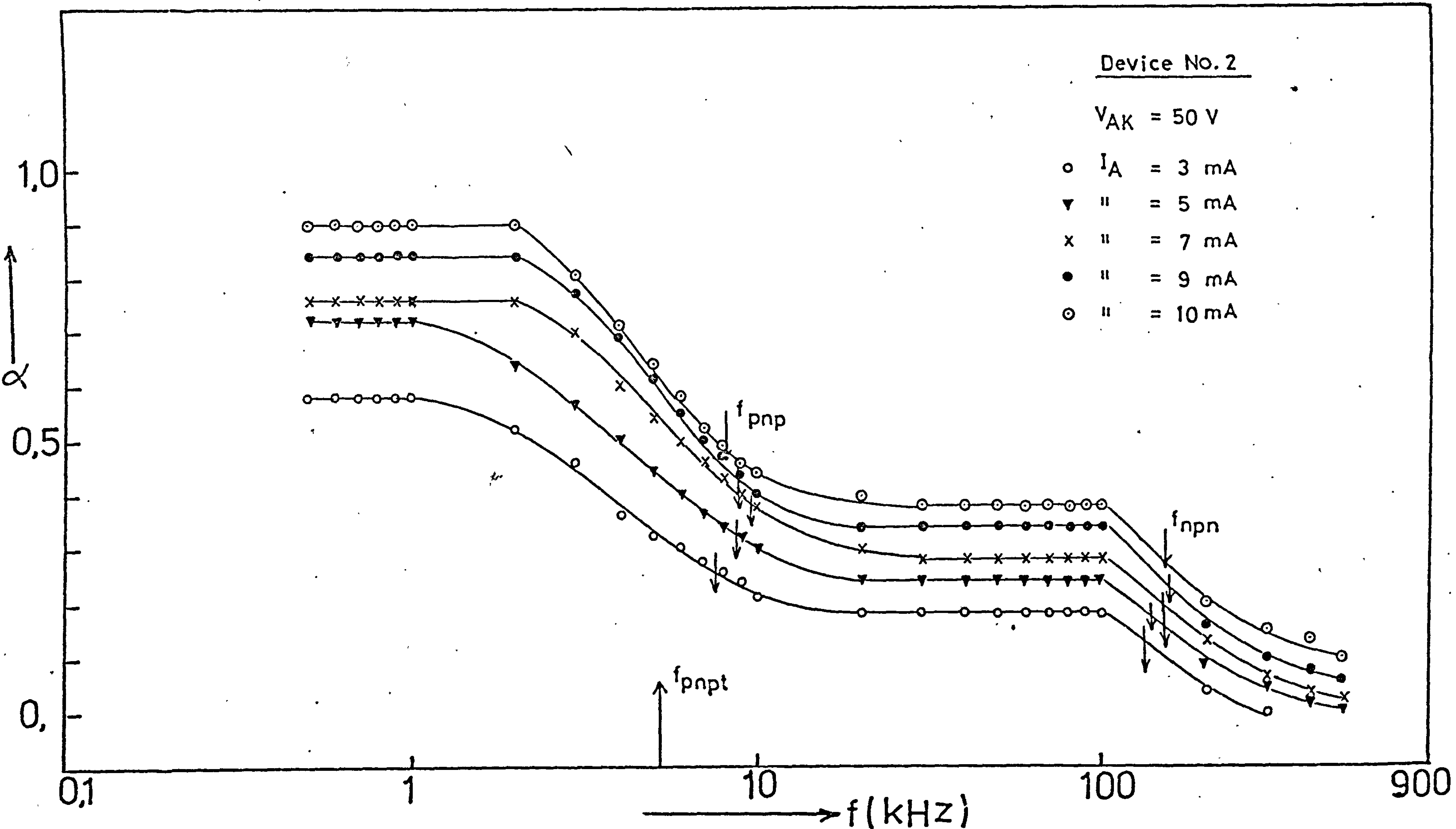


Figure (3-11) Frequency-response of current gain of a high-power thyristor.

Figure (3-12) Current gain as afunction of anode current for a high-power thyristor.

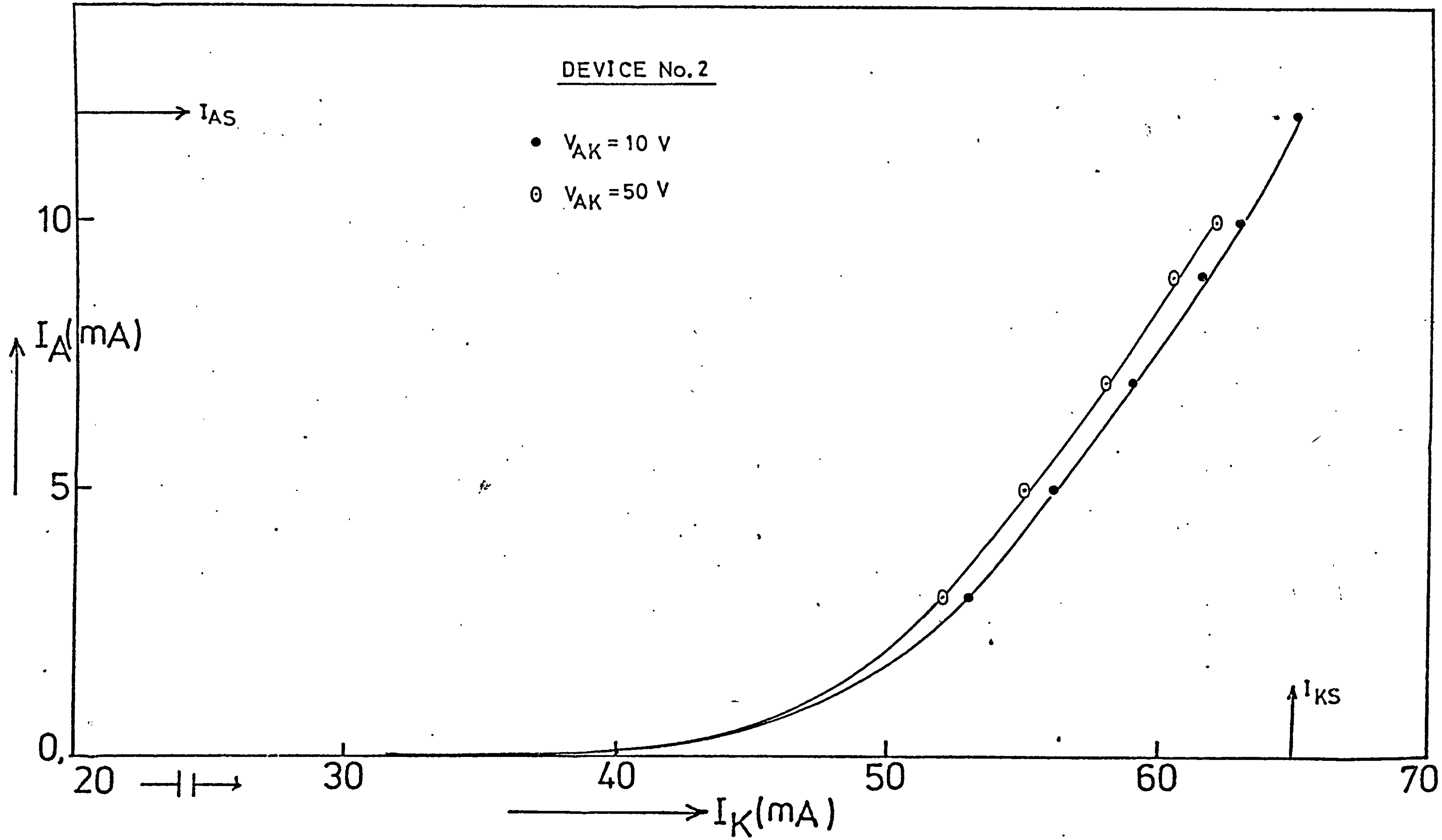


Figure (3-13) The anode-cathode dc-current charcteristics of high-power thyristor.

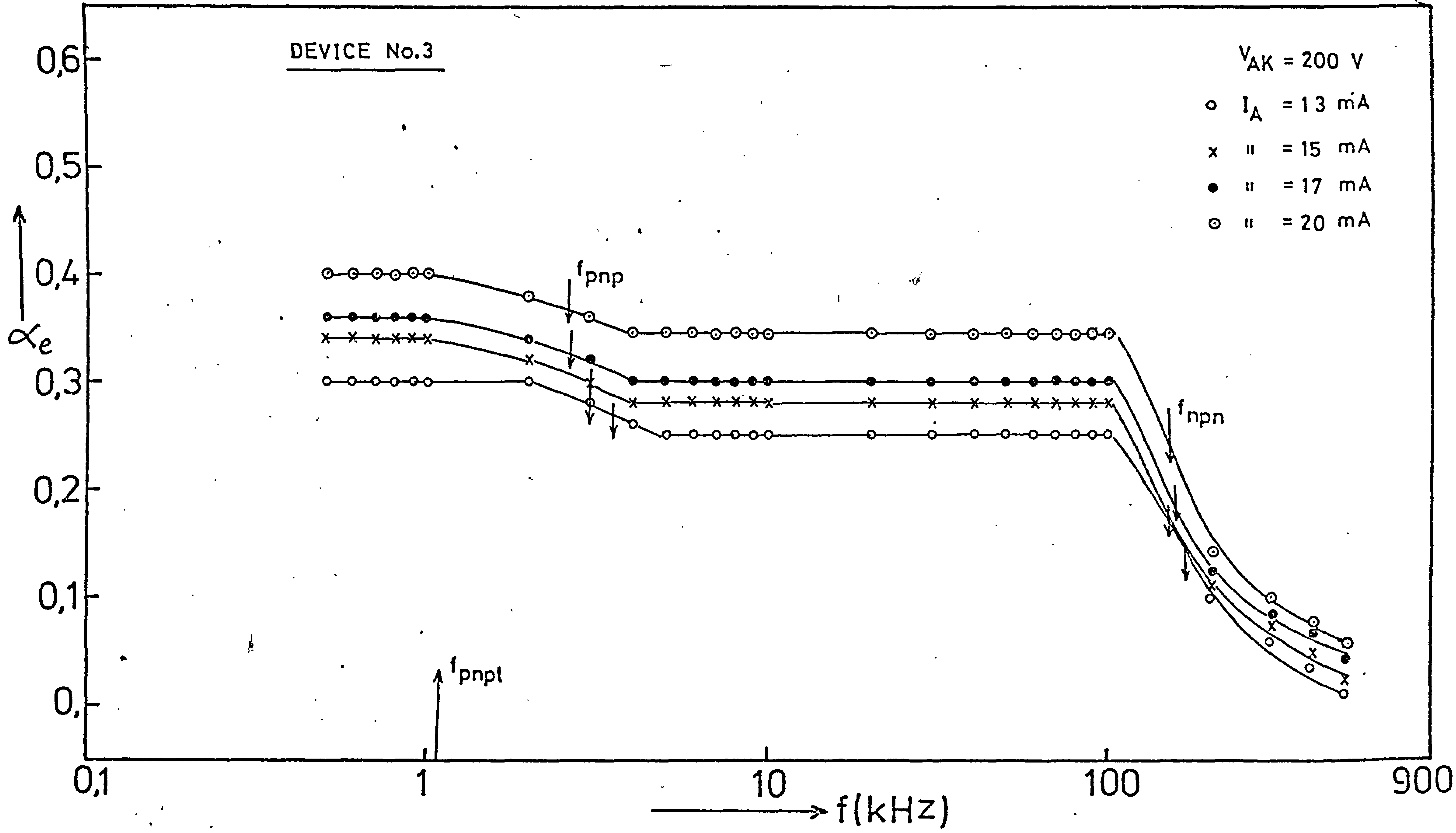


Figure (3-15) Frequency-response of current gain of a high-power thyristor.

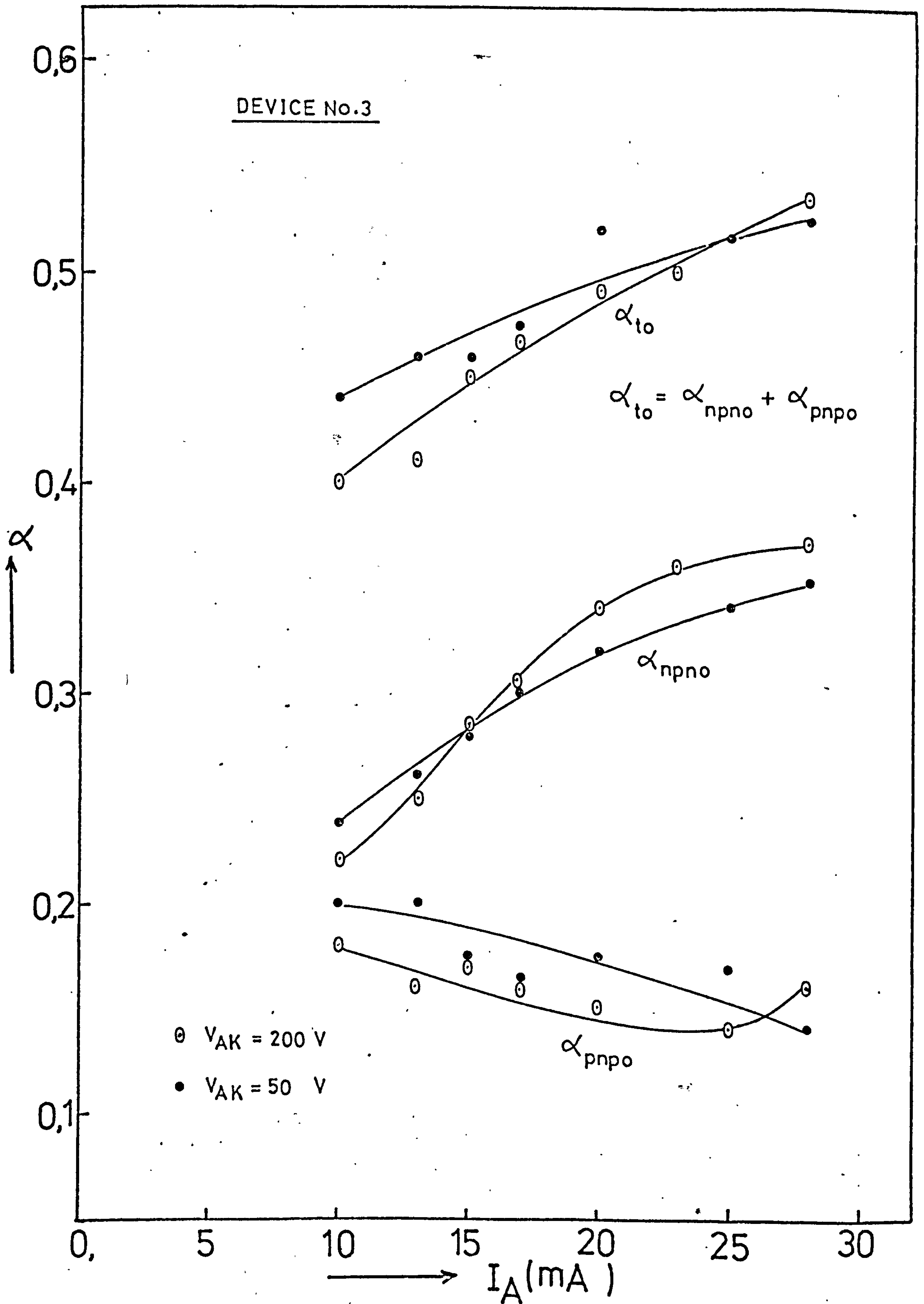


Figure (3-16) Current gain as a function of anode current of a high-power thyristor.

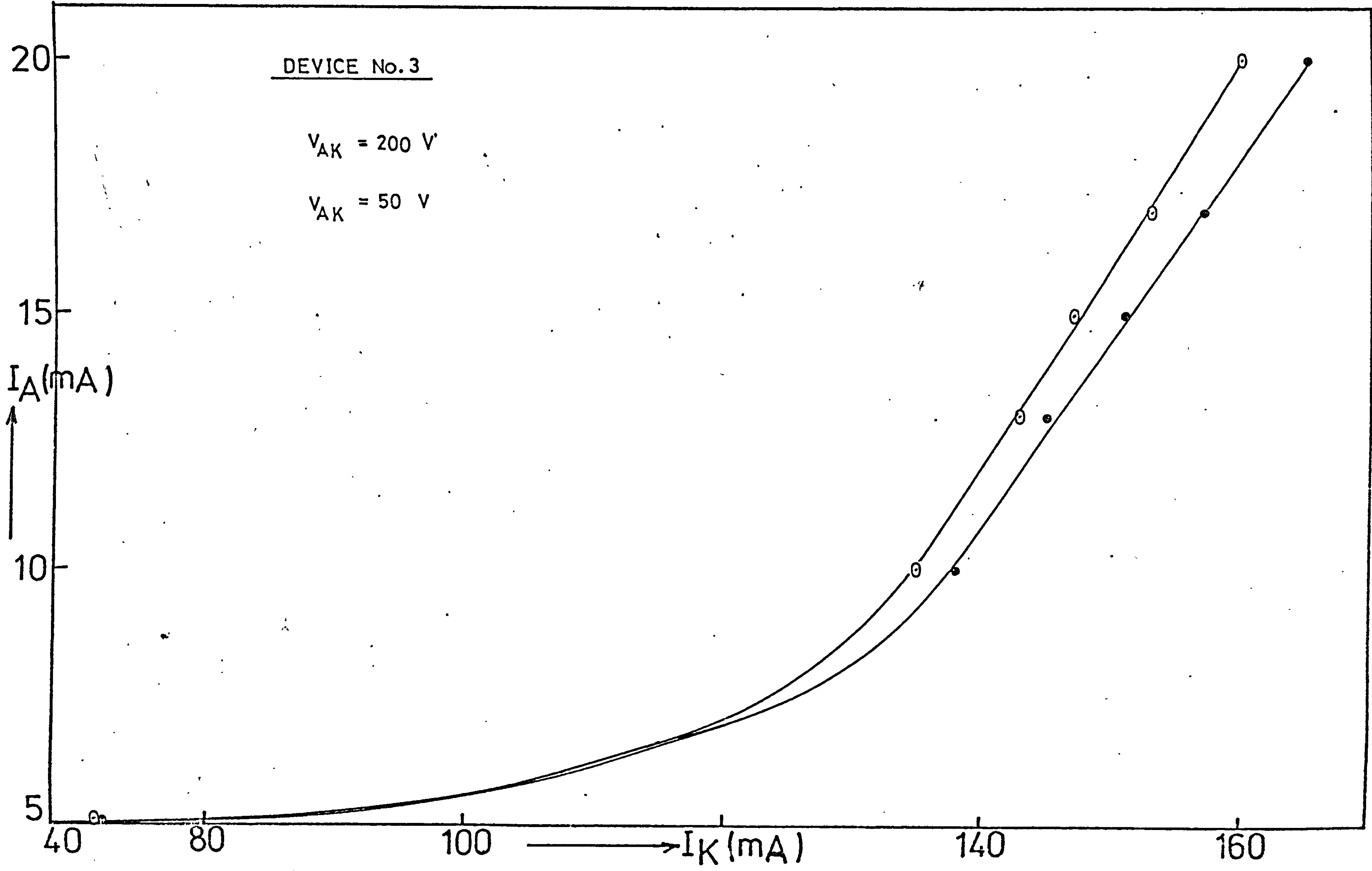


Figure (3-17) [illegible]

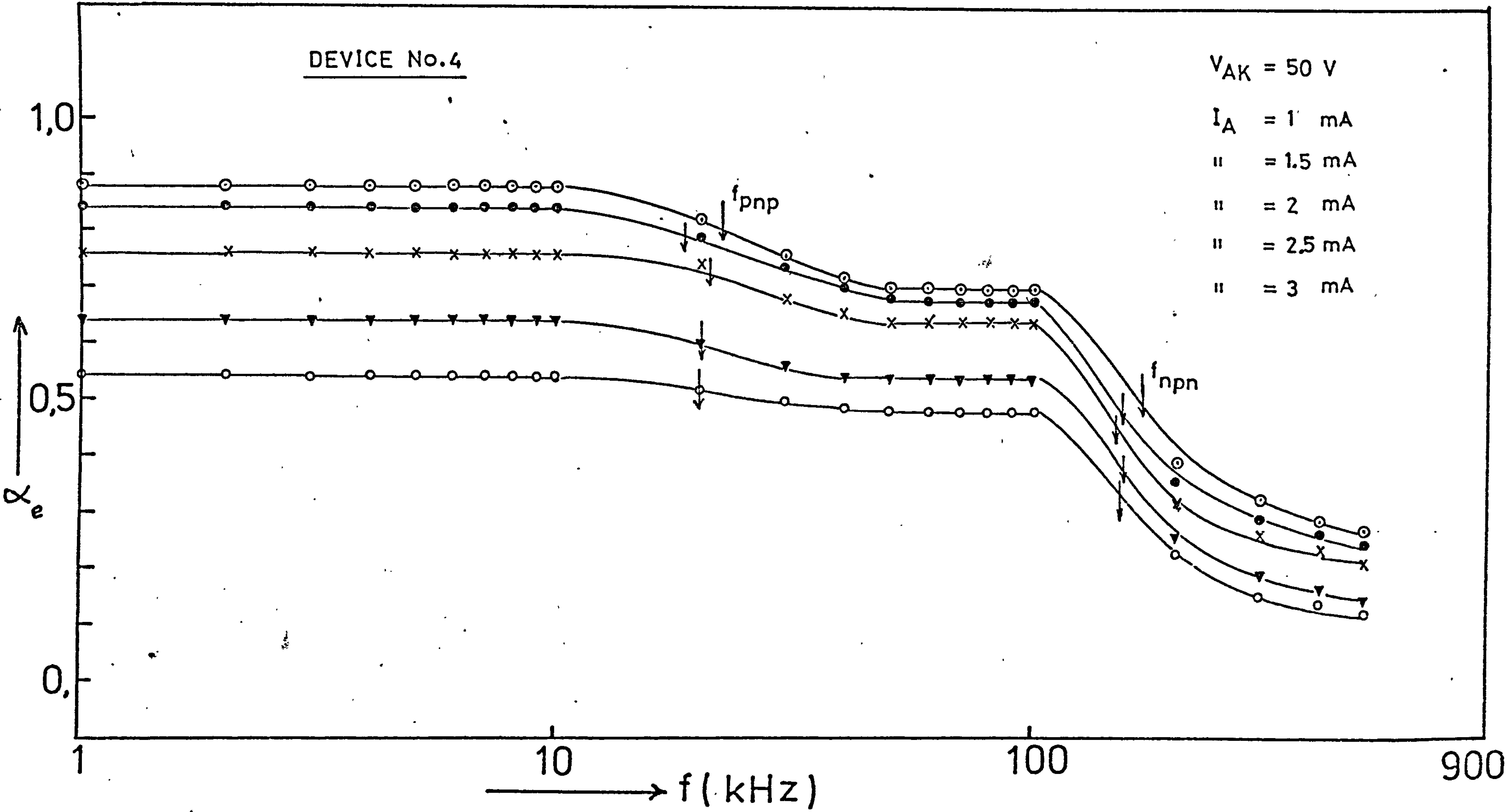


Figure (3-18) Frequency response of current gain of a 10A thyristor (not gold-doped).

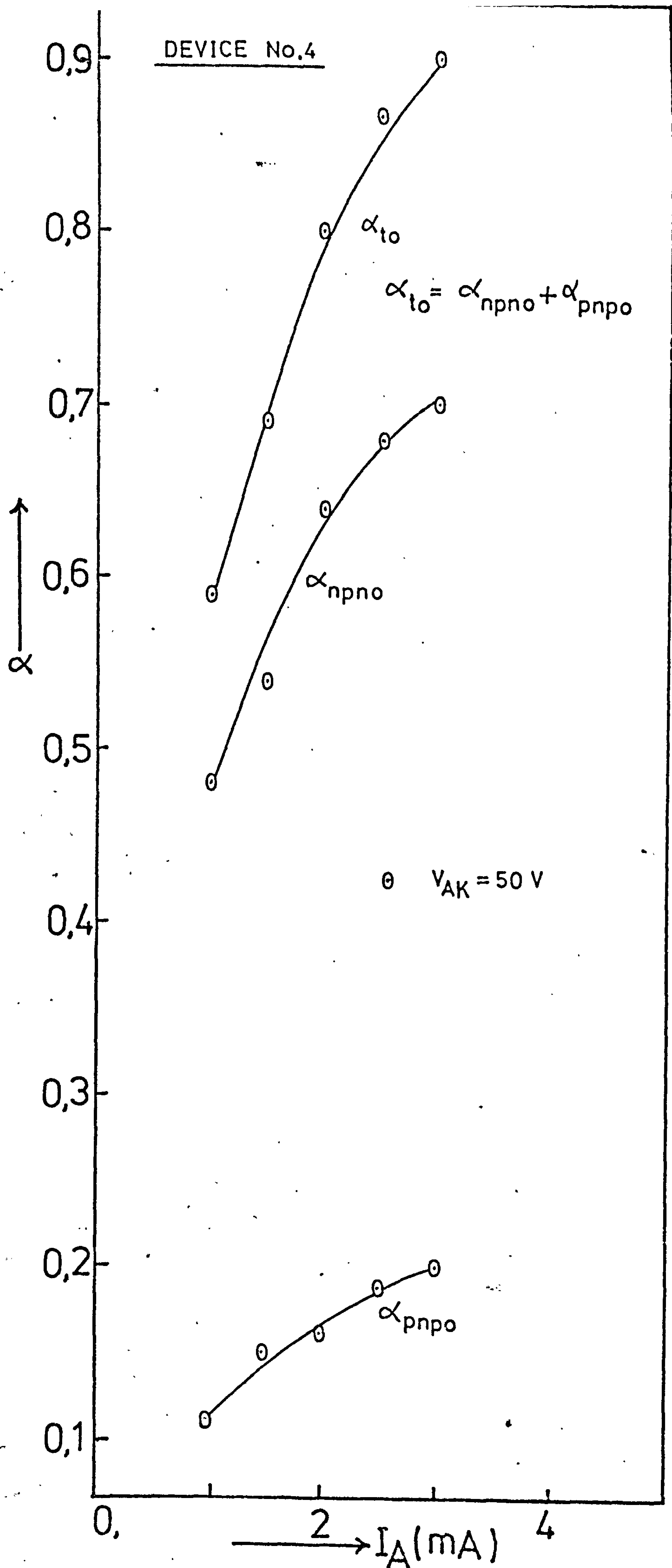


Figure (3-19) Current gain as a function of anode current for a 10A thyristor (not gold-doped).

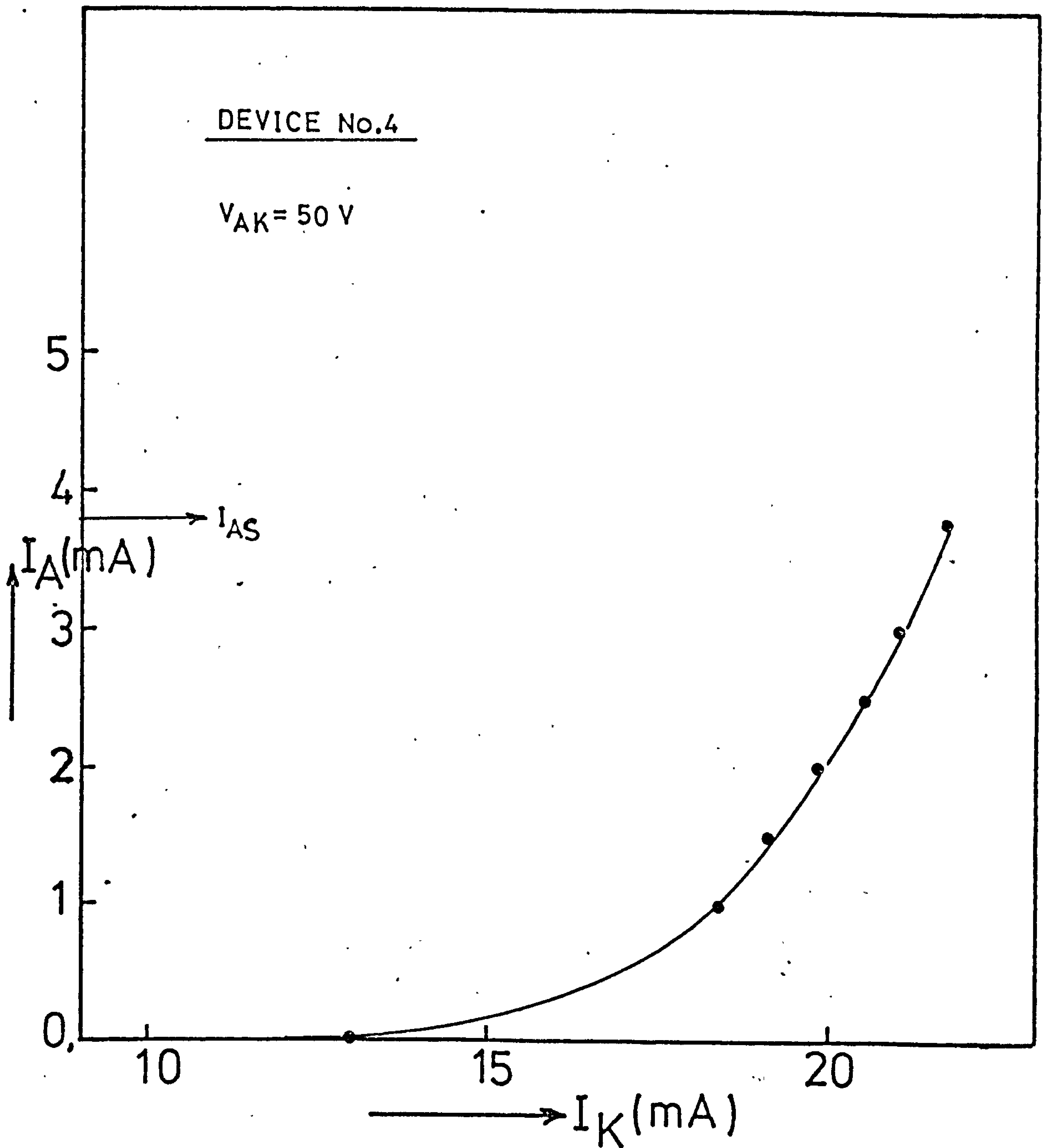


Figure (3-20) The anode-cathode dc-current characteristics of a 10A thyristor (not gold-doped).

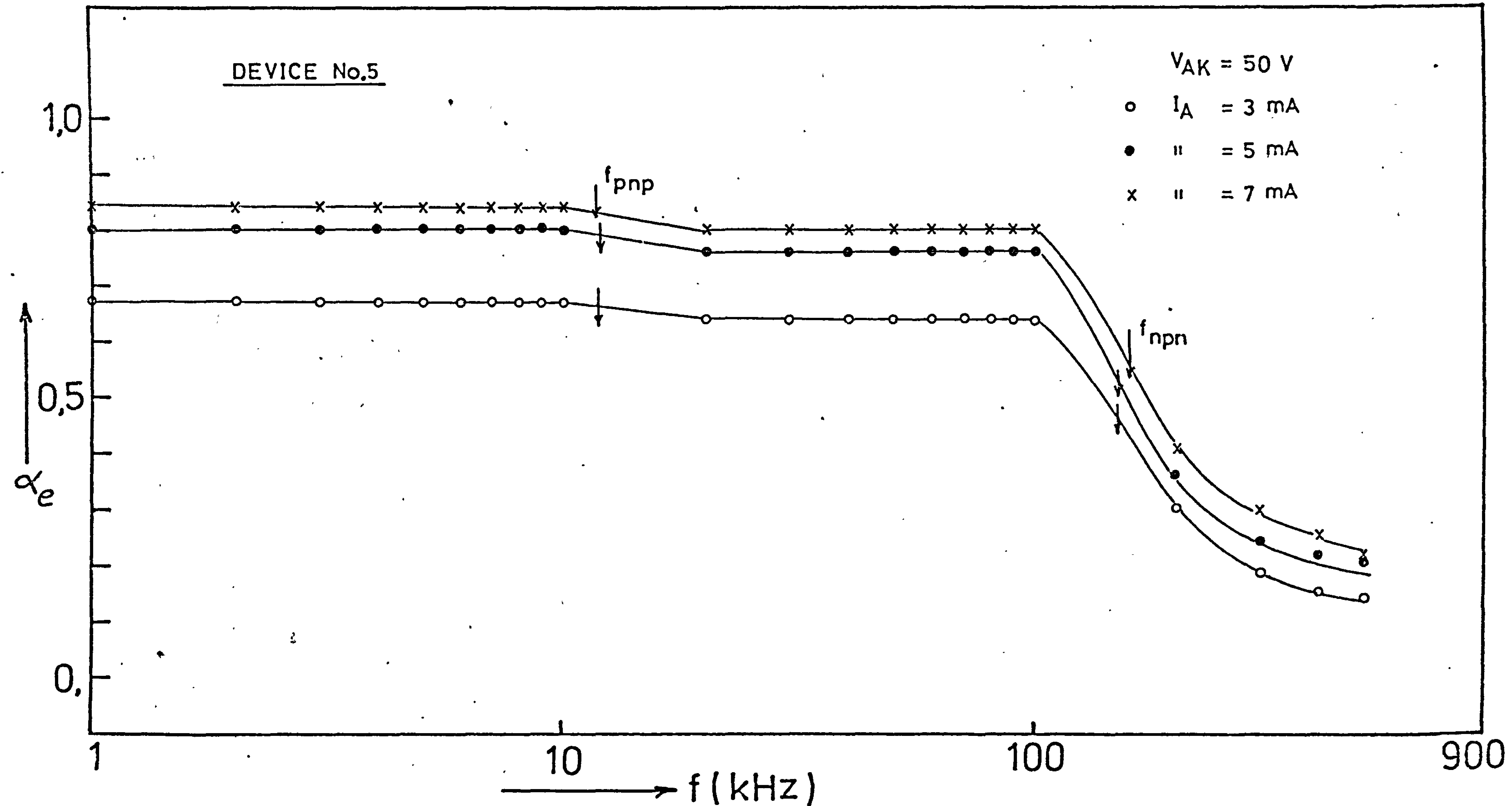


Figure (3-21) Frequency-response of current gain of a 10A thyristor (gold-doped).

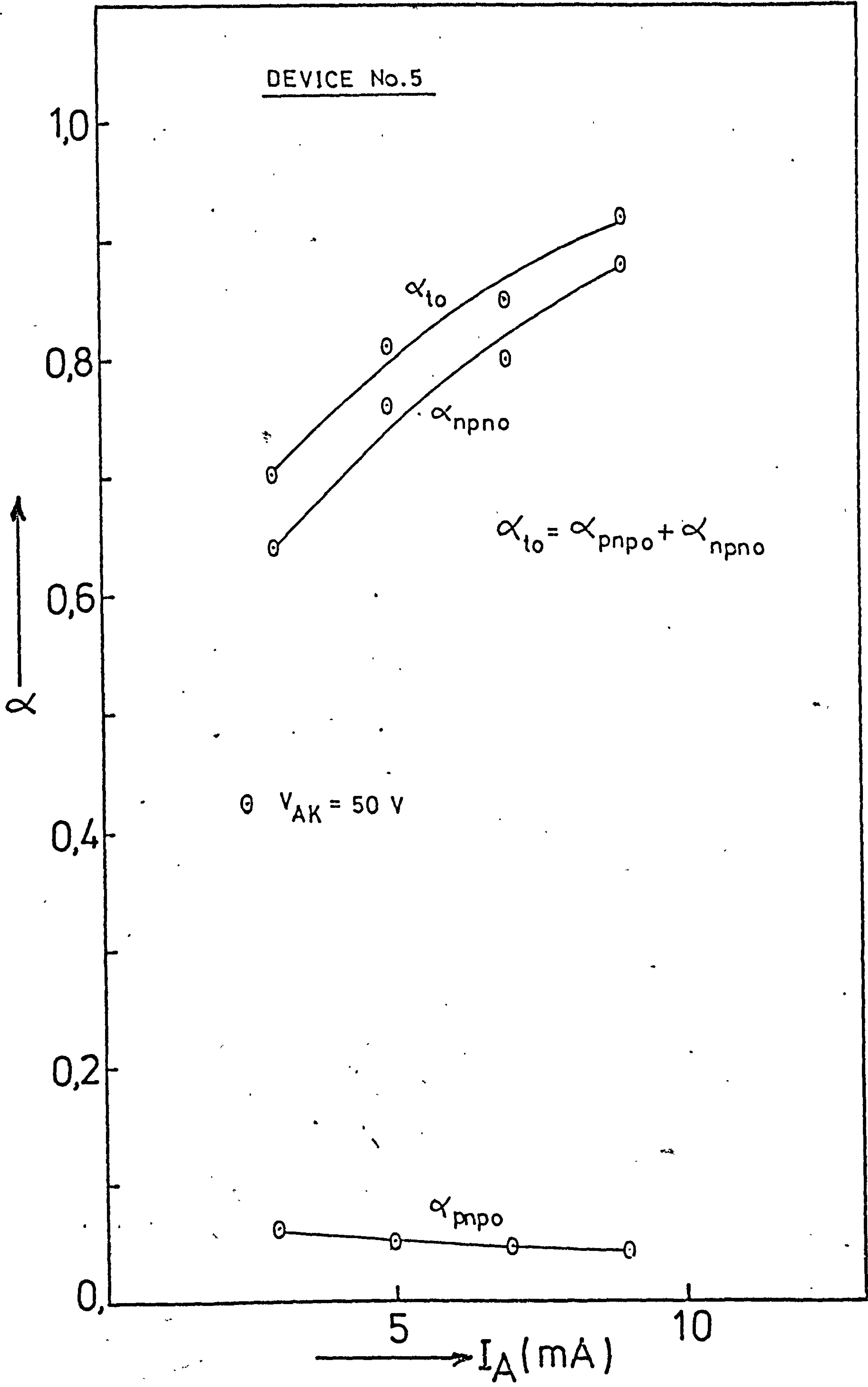


Figure (3-22) Current gain as a function of anode current for a 10A thyristor (gold-doped).

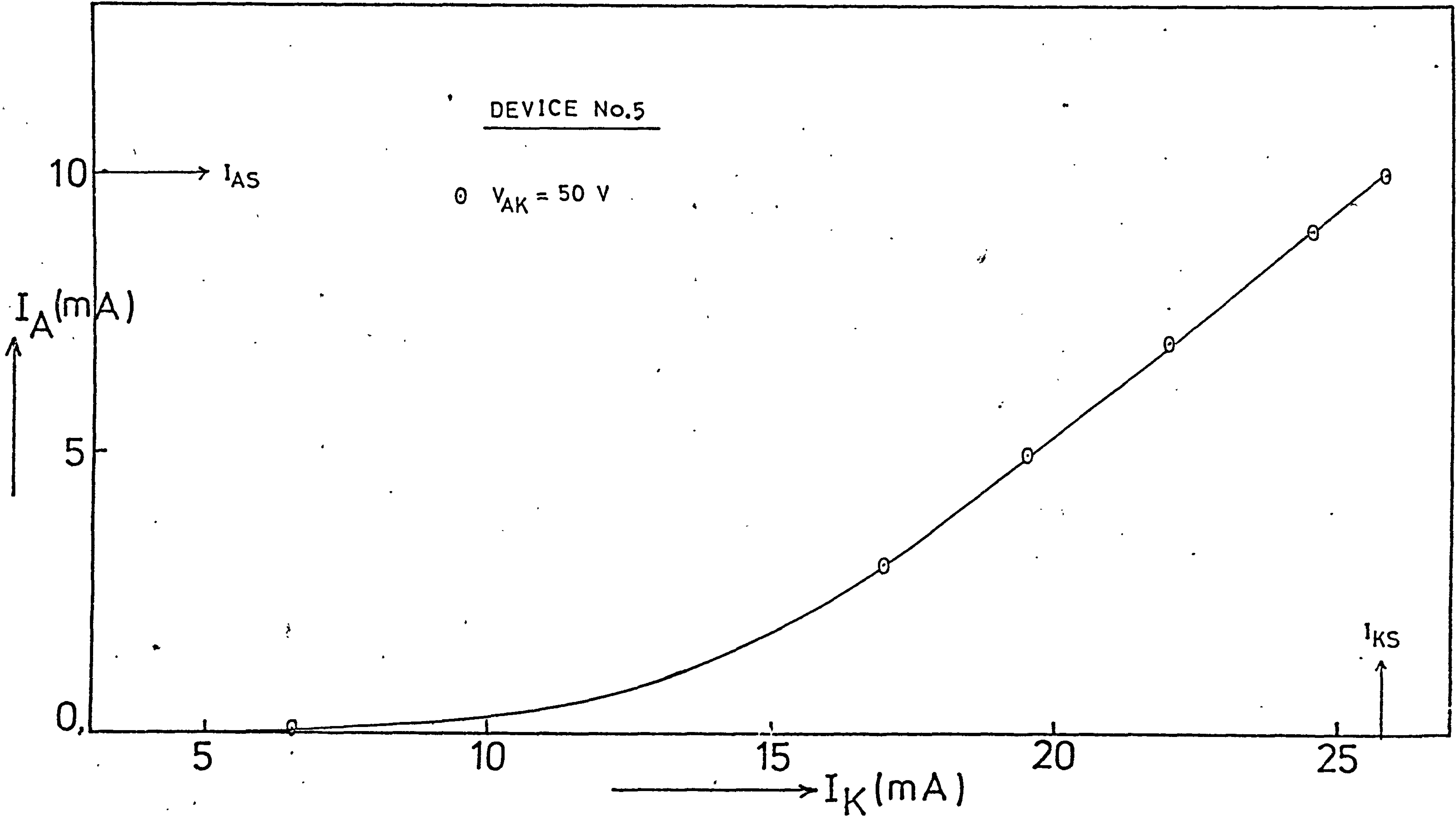


Figure (3-23) The anode-cathode dc-current characteristics of a [illegible] thyristor (gold-doped).

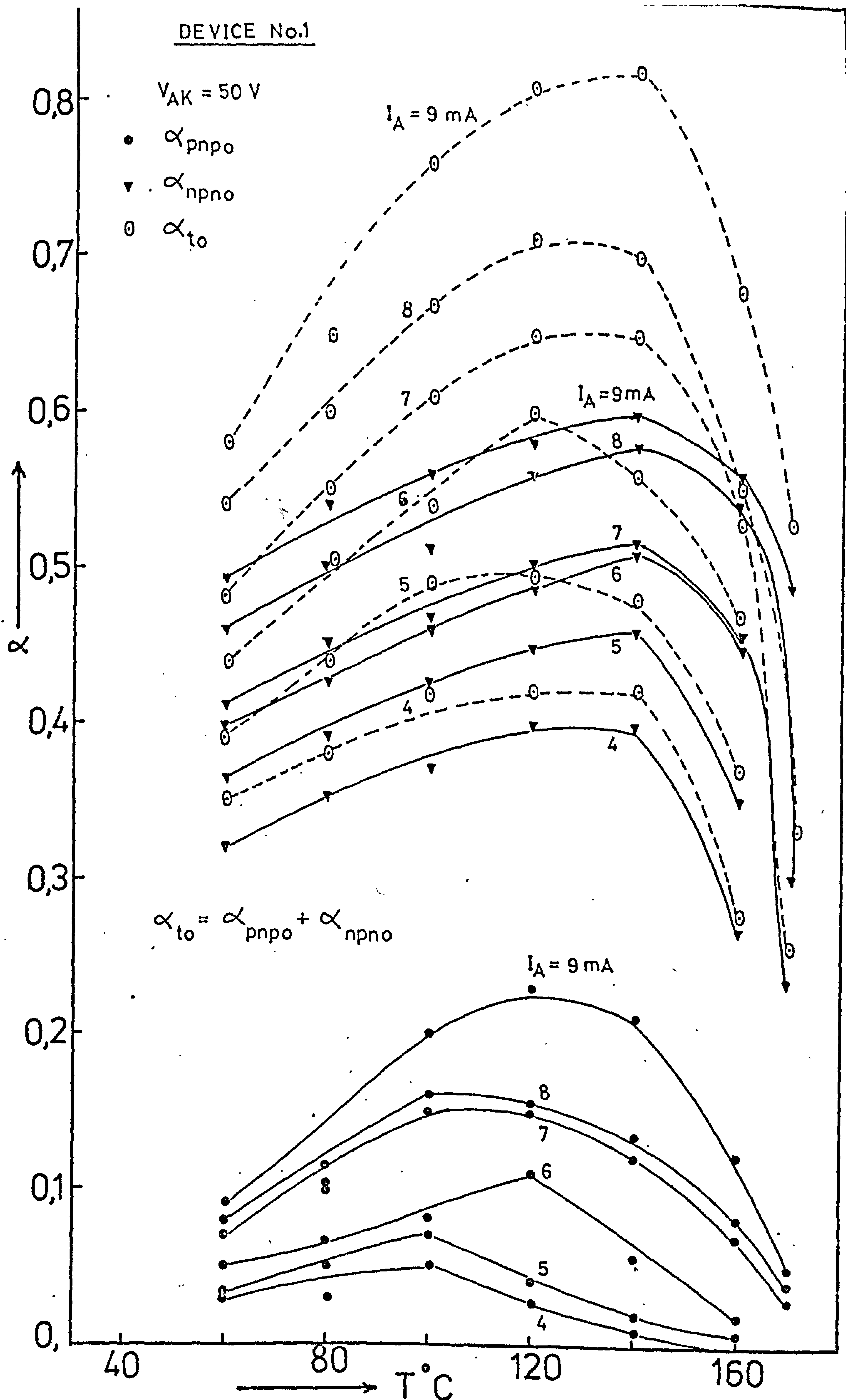


Figure (4-1) Current gain as a function of temperature for a medium-power thyristor.

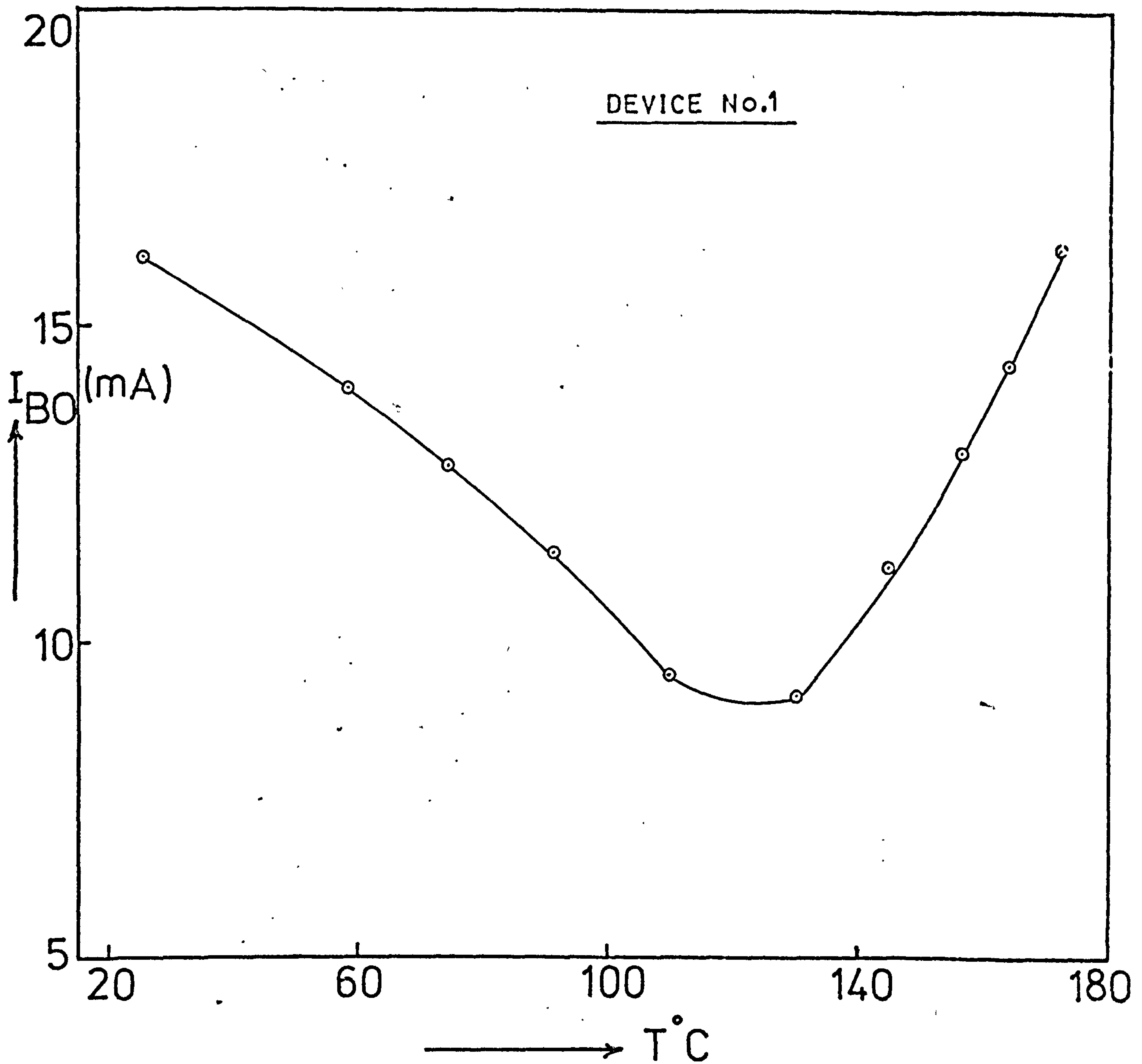


Figure (4-2) Breakover current as a function of temperature for a medium-power thyristor.

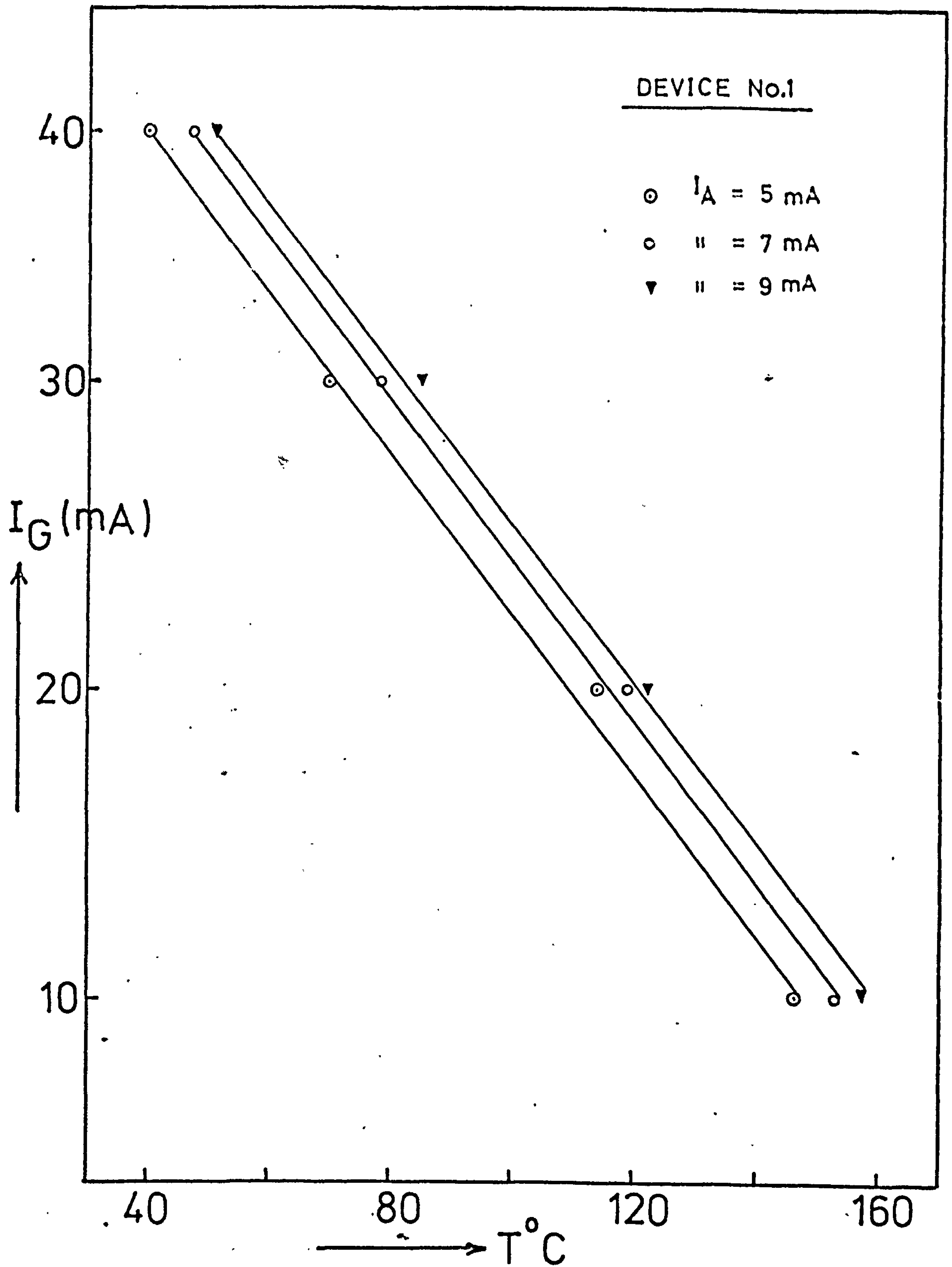


Figure (4-3) Gate firing current as a function of temperature for a medium-power thyristor.

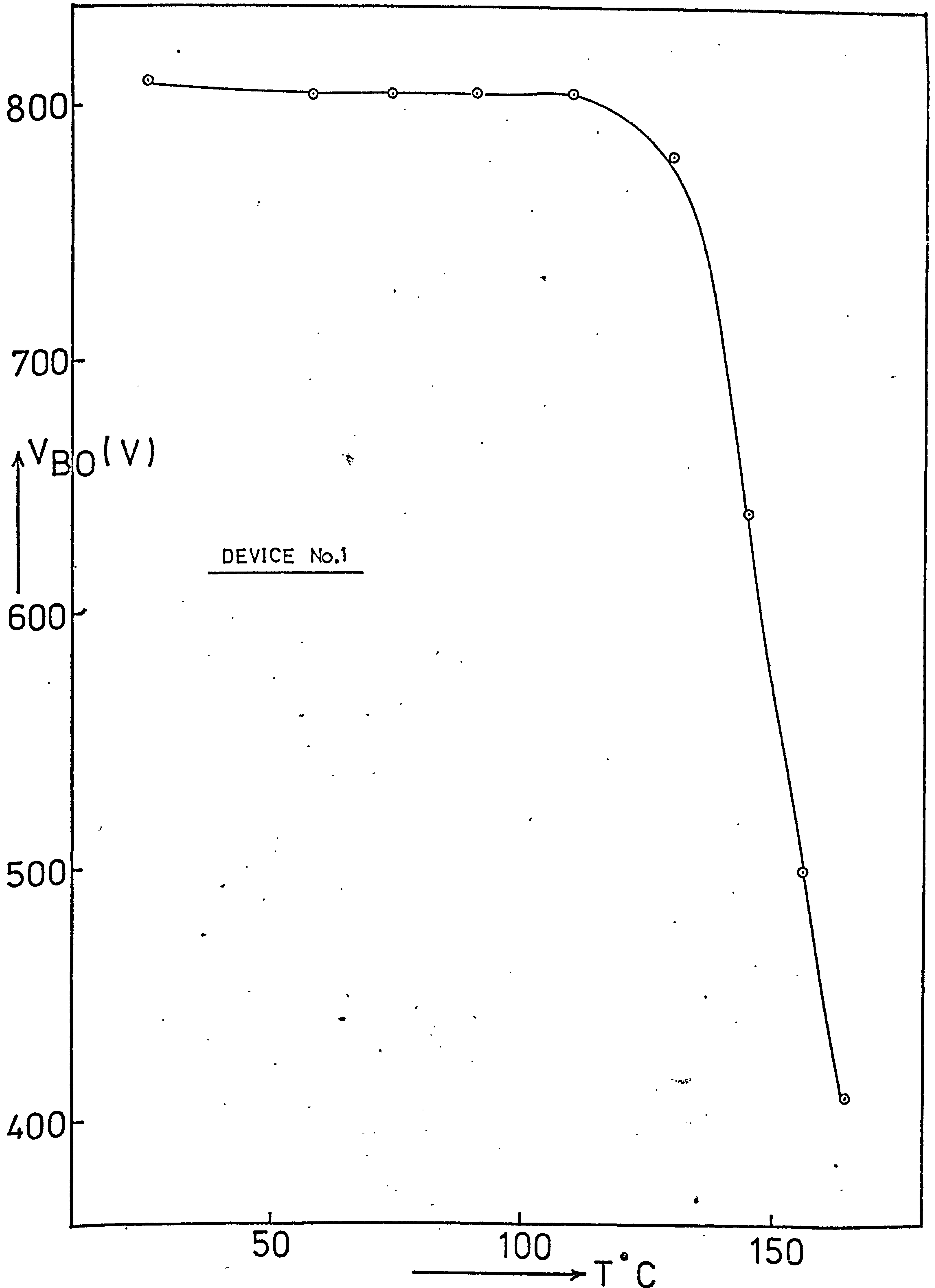


Figure (4-4) Breakover voltage as a function of temperature for a medium-power thyristor.

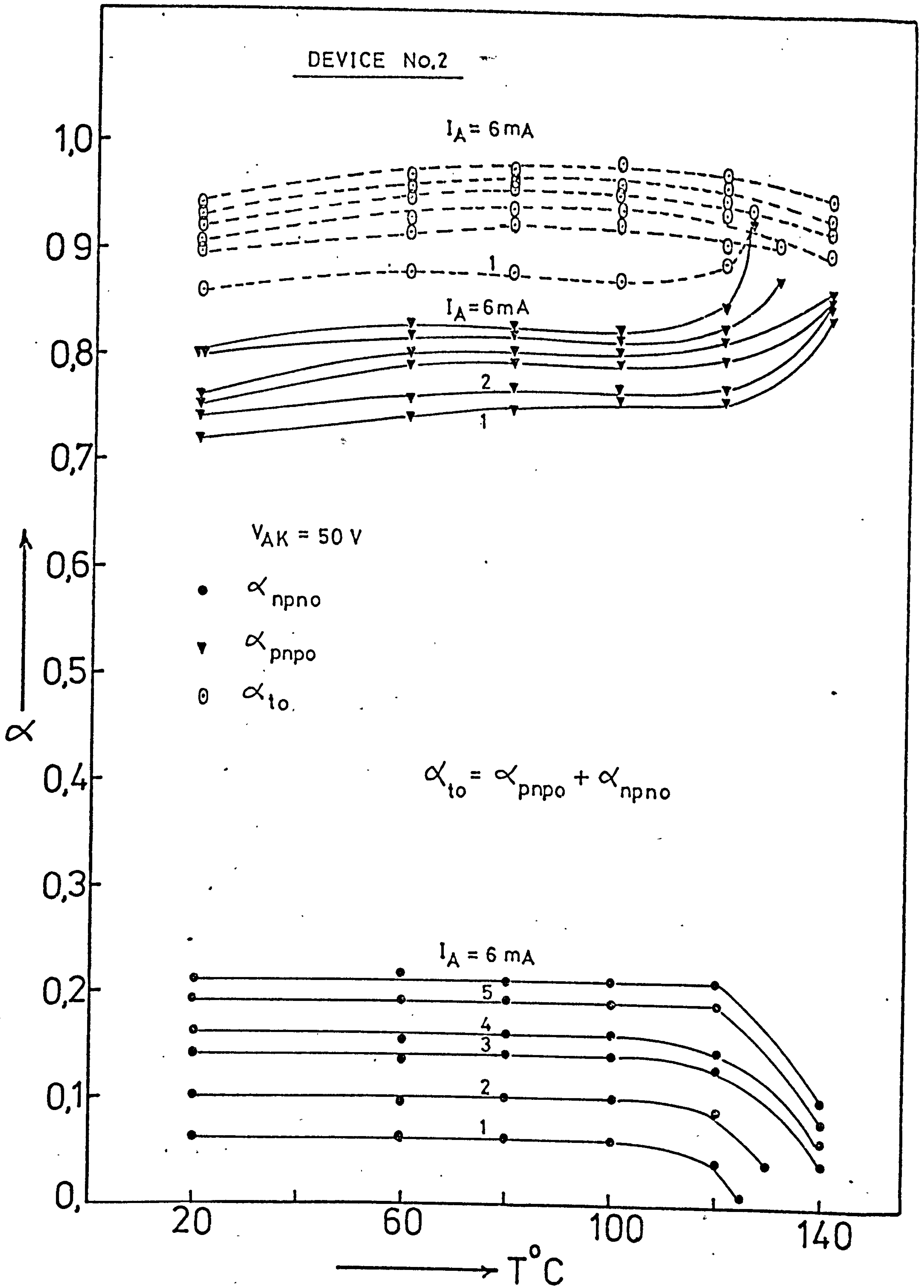


Figure (4-5) Current gain as a function of temperature for a high-power thyristor.

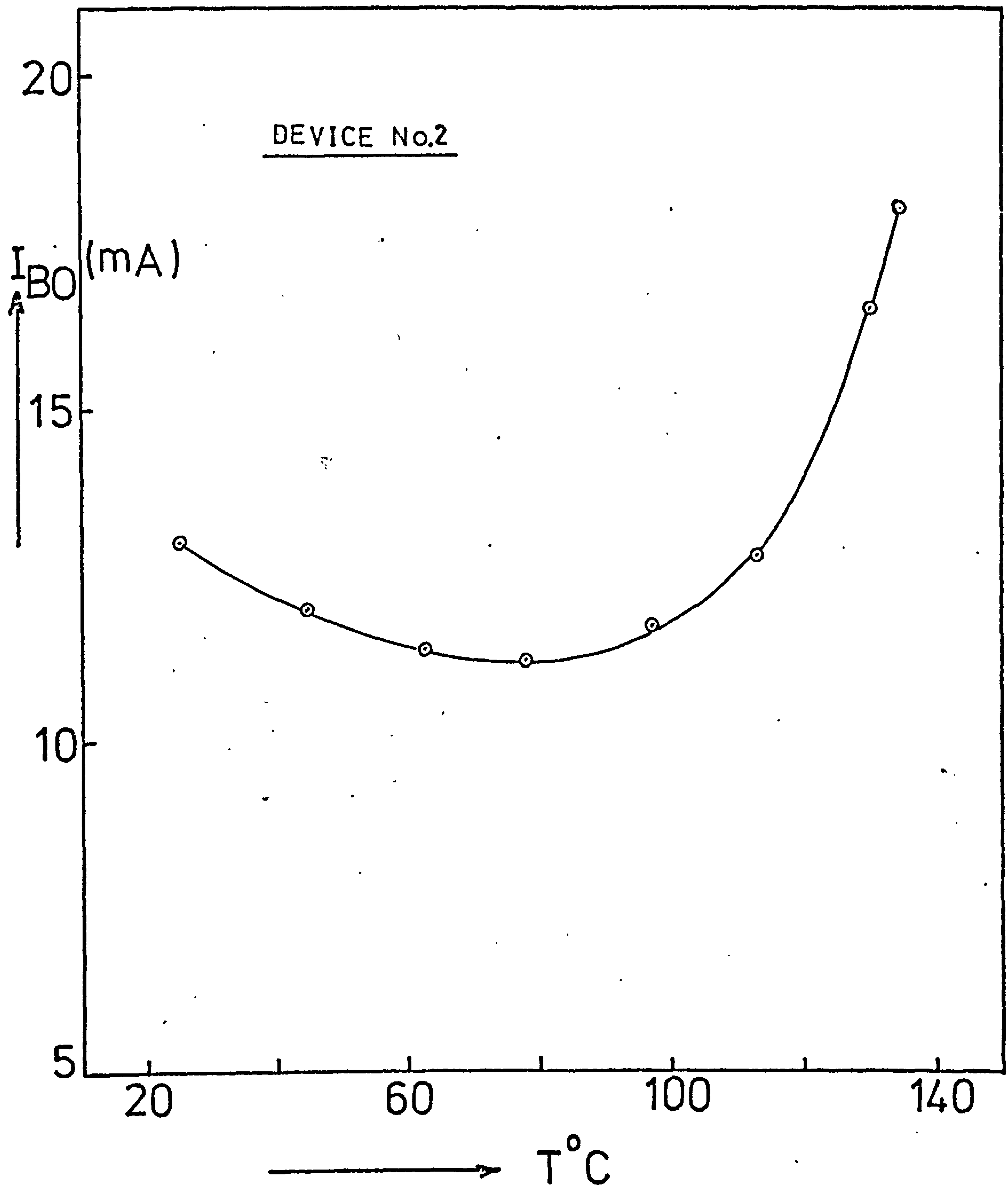


Figure (4-6) Breakover current as a function of temperature for a high-power thyristor.

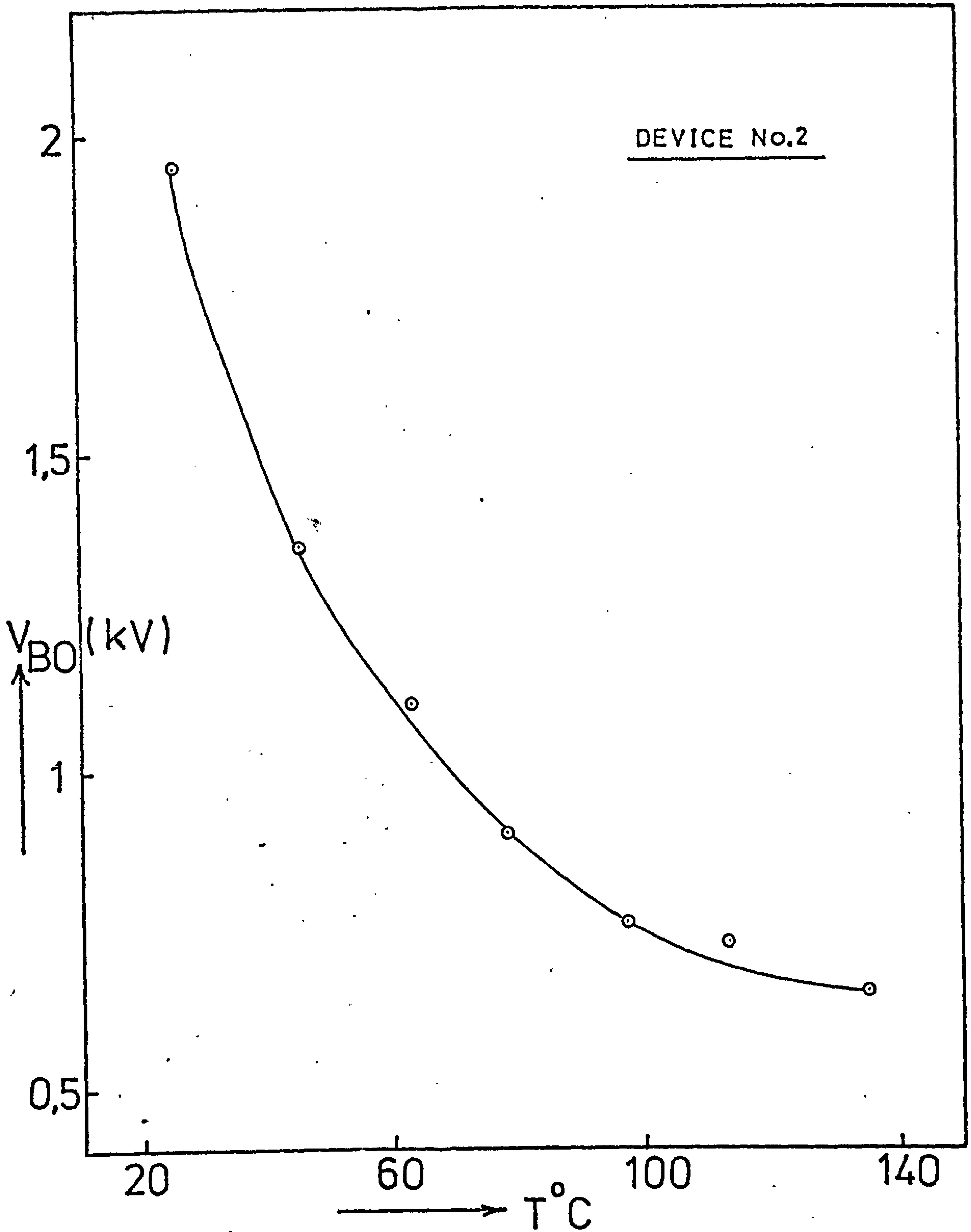


Figure (4-7) Breakover voltage as a function of temperature for a high-power thyristor.

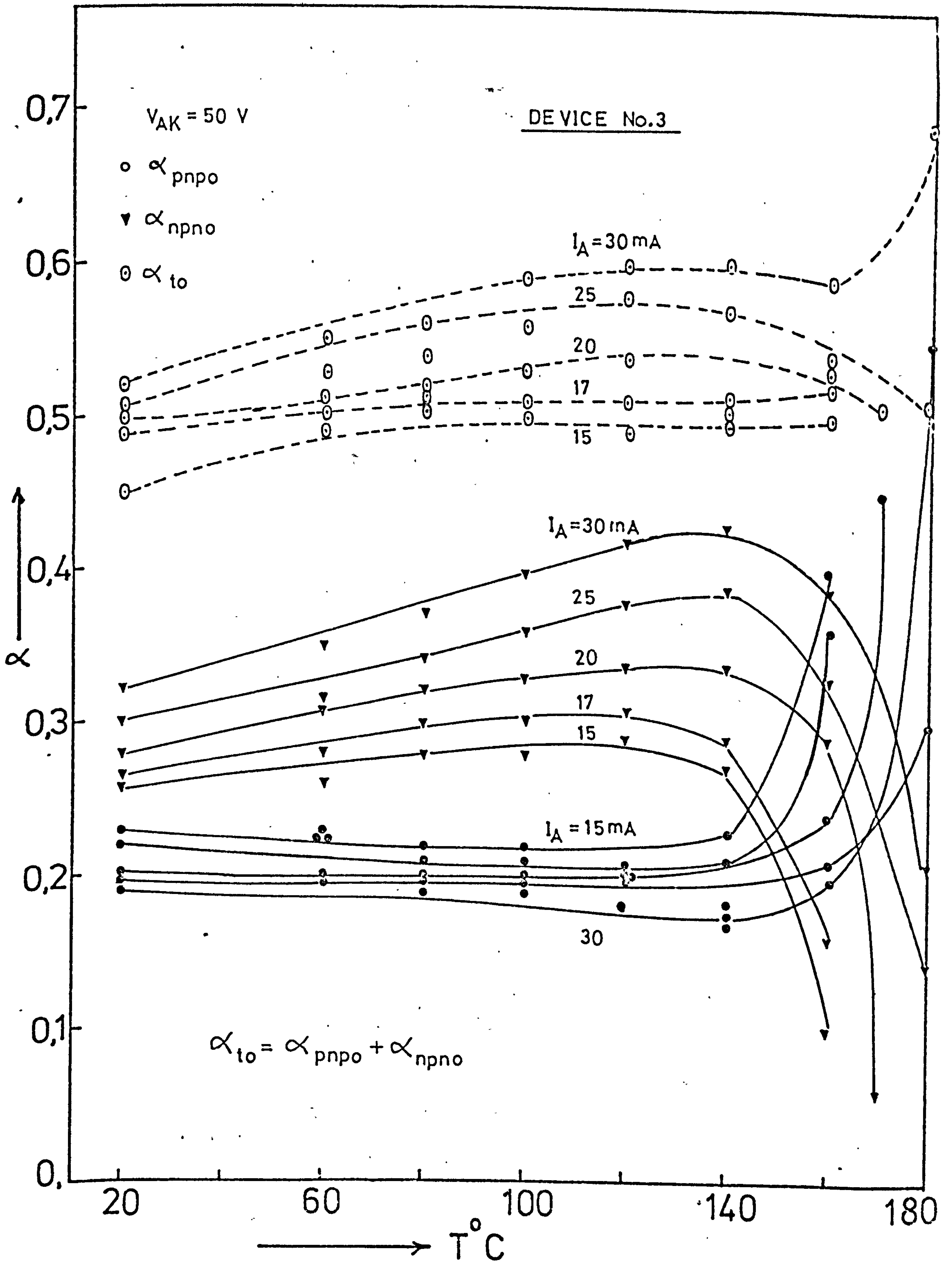


Figure (4-8) Current gain as a function of temperature for a high-power thyristor.

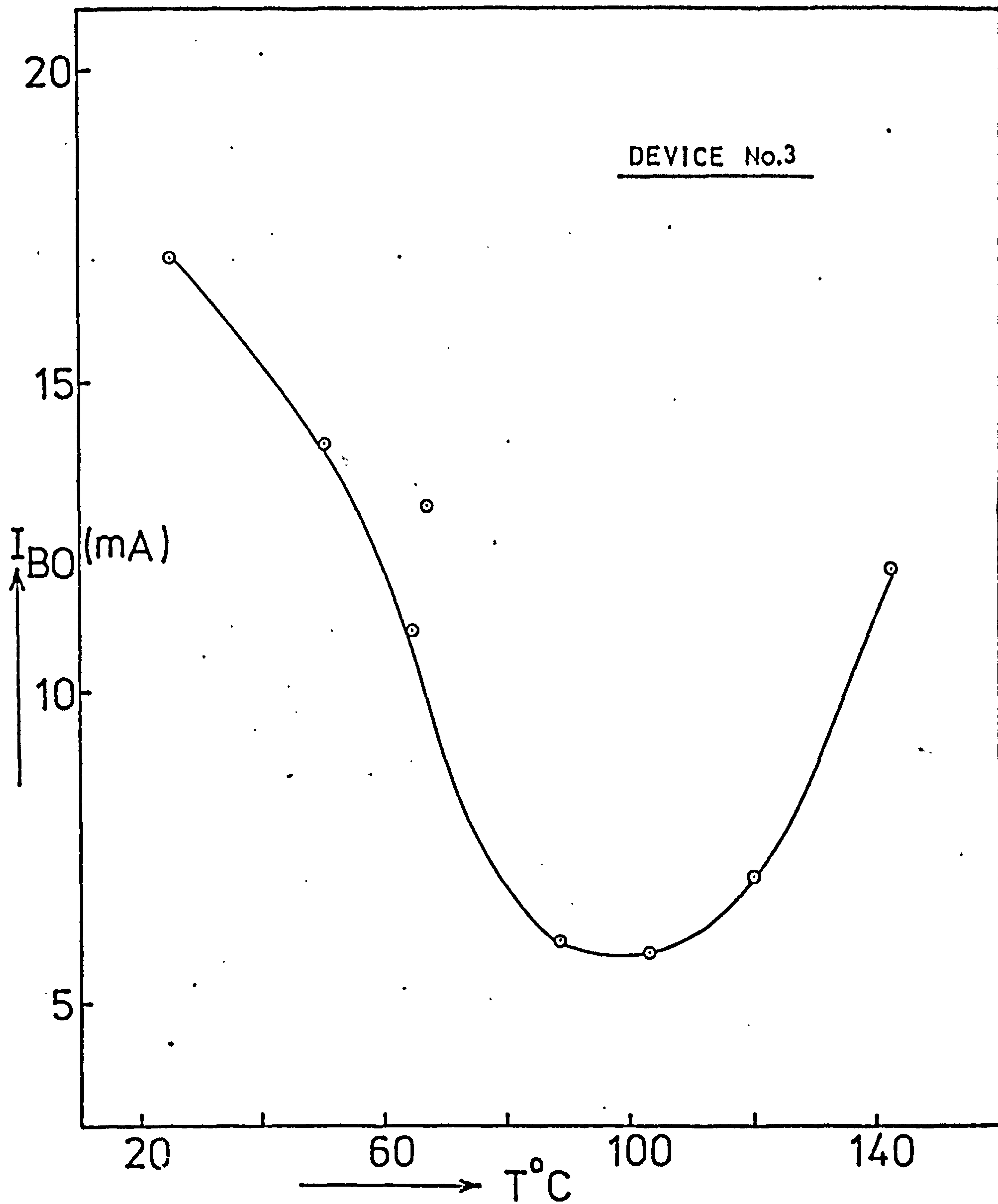


Figure (4-9) Breakover current as a function of temperature of a high-power thyristor.

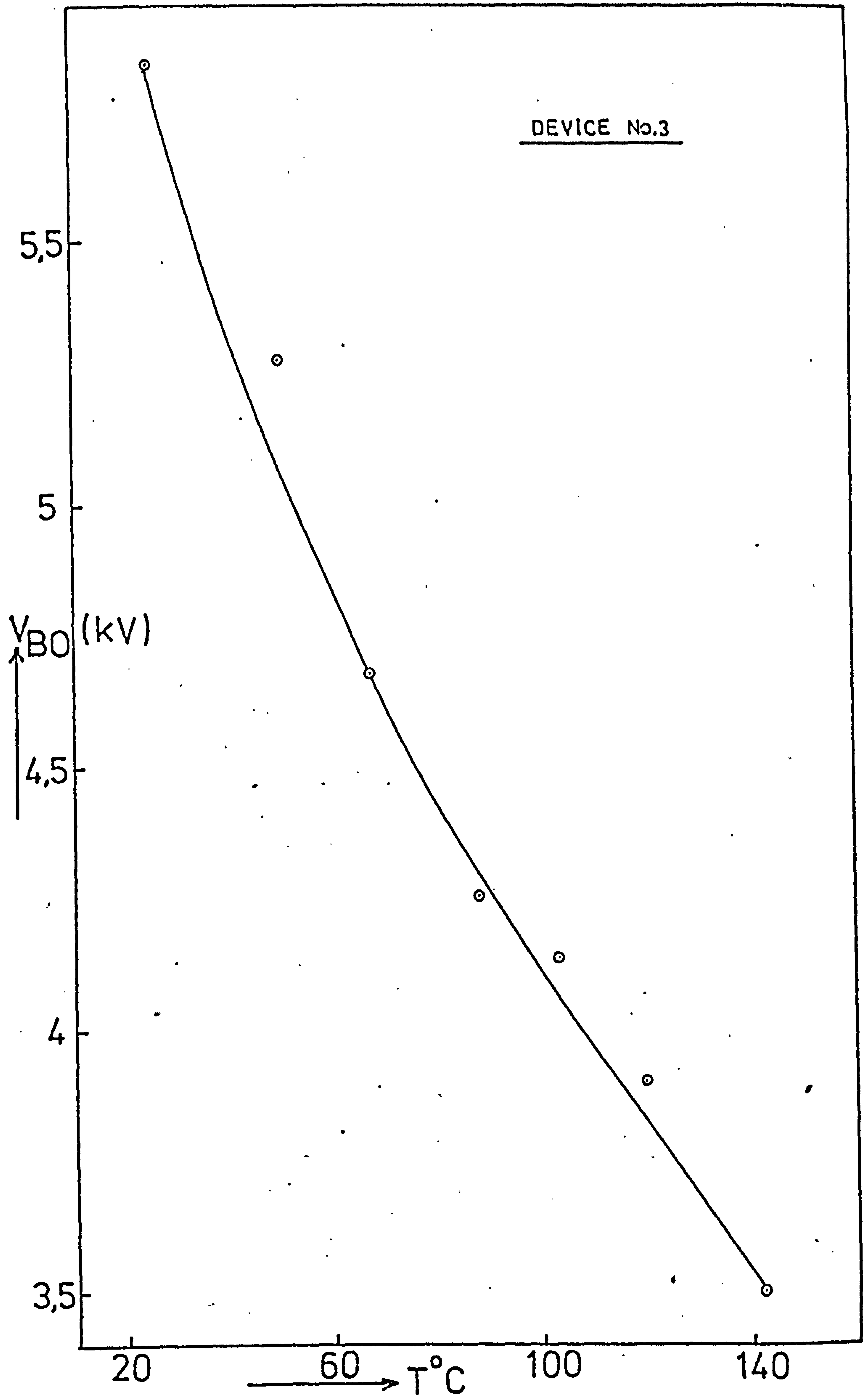


Figure (4-10) Breakover voltage as a function of temperature of high-power thyristor.

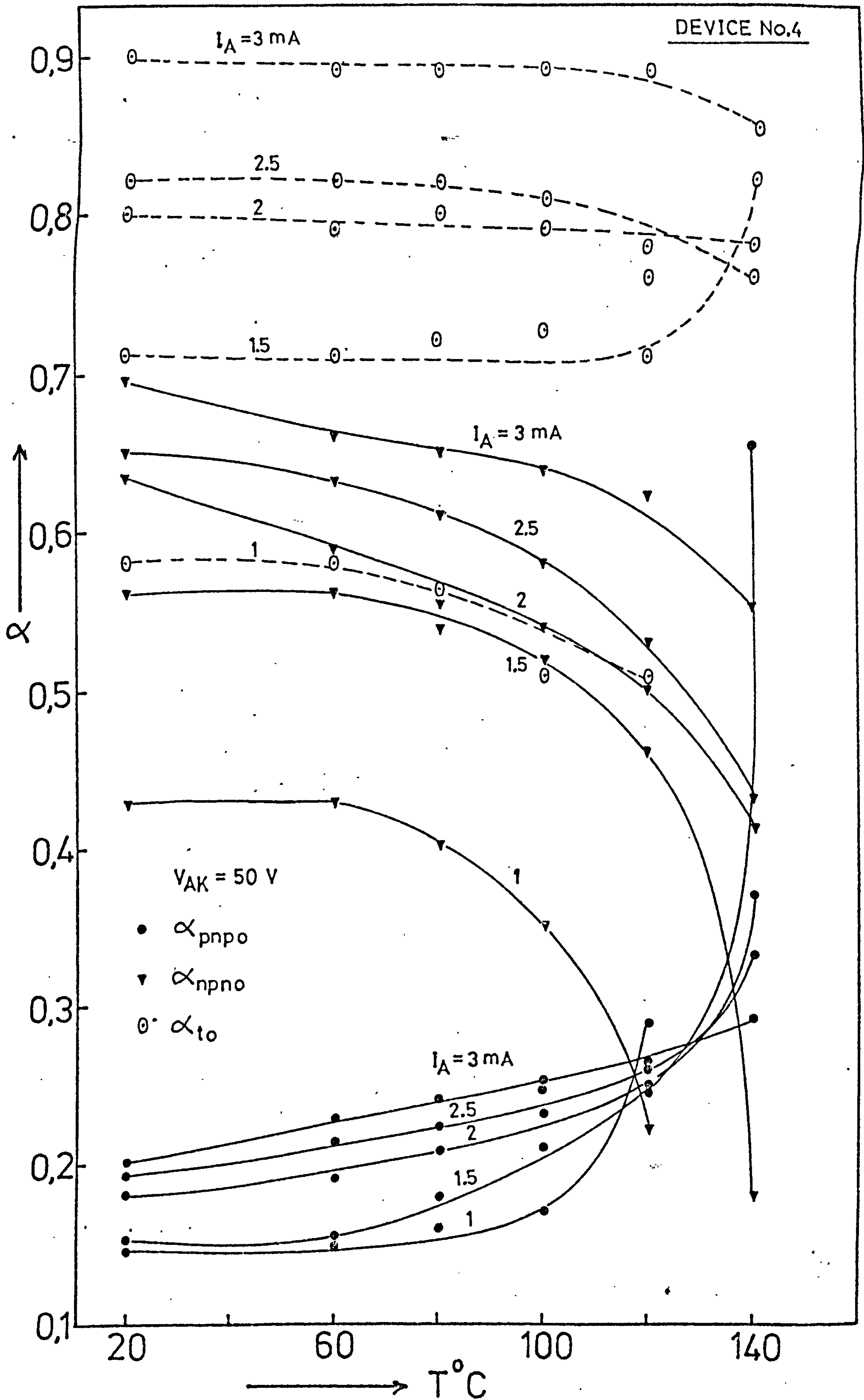


Figure (4-11) Current gain as a function of temperature for a 10A thyristor (not gold-doped).

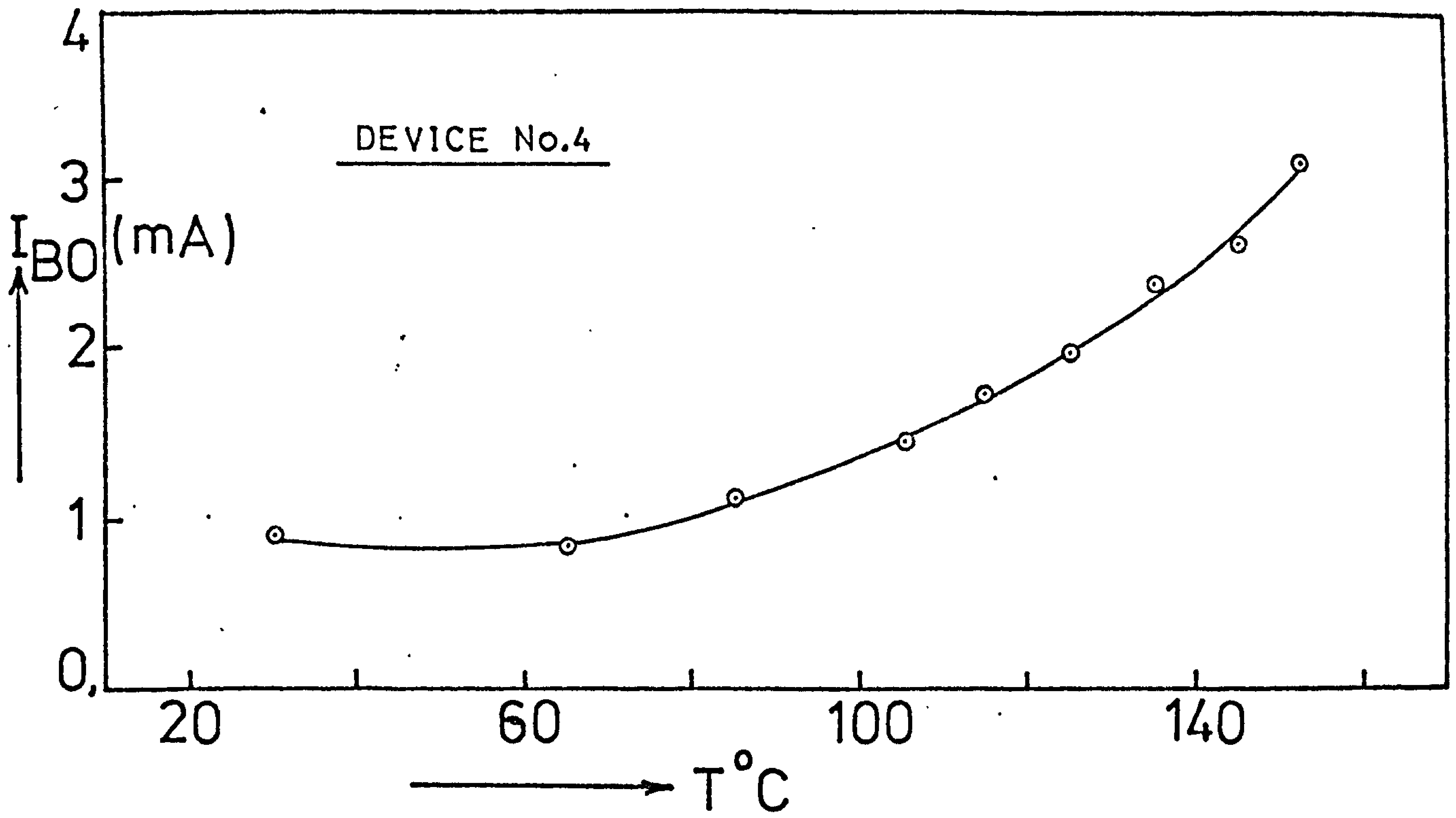


Figure (4-12) Breakover current as a function of temperature for a lCA thyristor (not gold-doped).

DEVICE No 4
V_{BO} (mA)
500
450
400
20
60
100
140
T°C

Figure (4-13) Breakover voltage as a function of temperature for a lOA thyristor (not gold-doped).

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Figure (4.14) Current gain as a function of temperature for a 10A

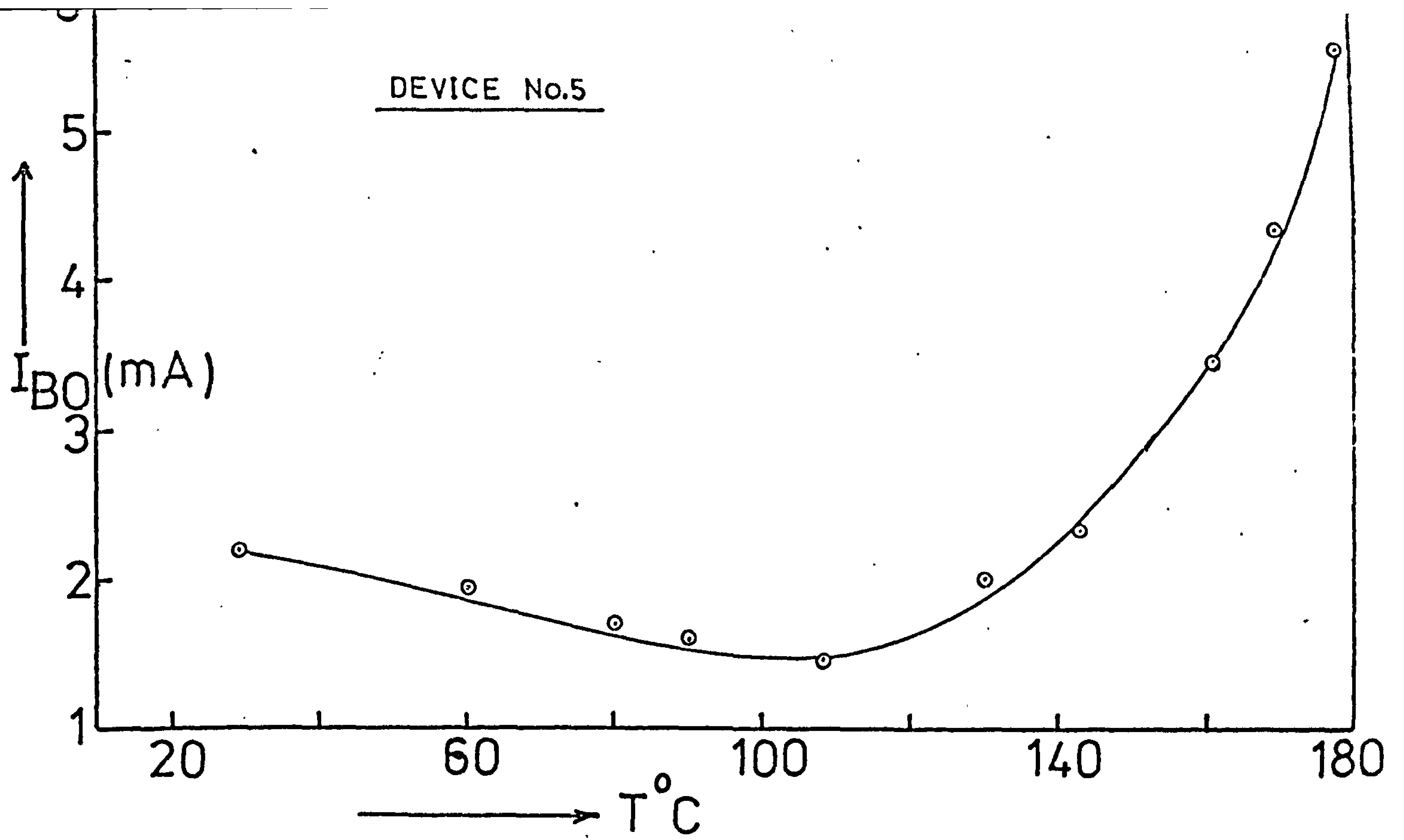


Figure (4-15) Breakover current as a function of temperature for a 10A thyristor (gold-doped).

Figure (4-16) Breakover voltage as a function of temperature for a 10A thyristor (gold-doped).

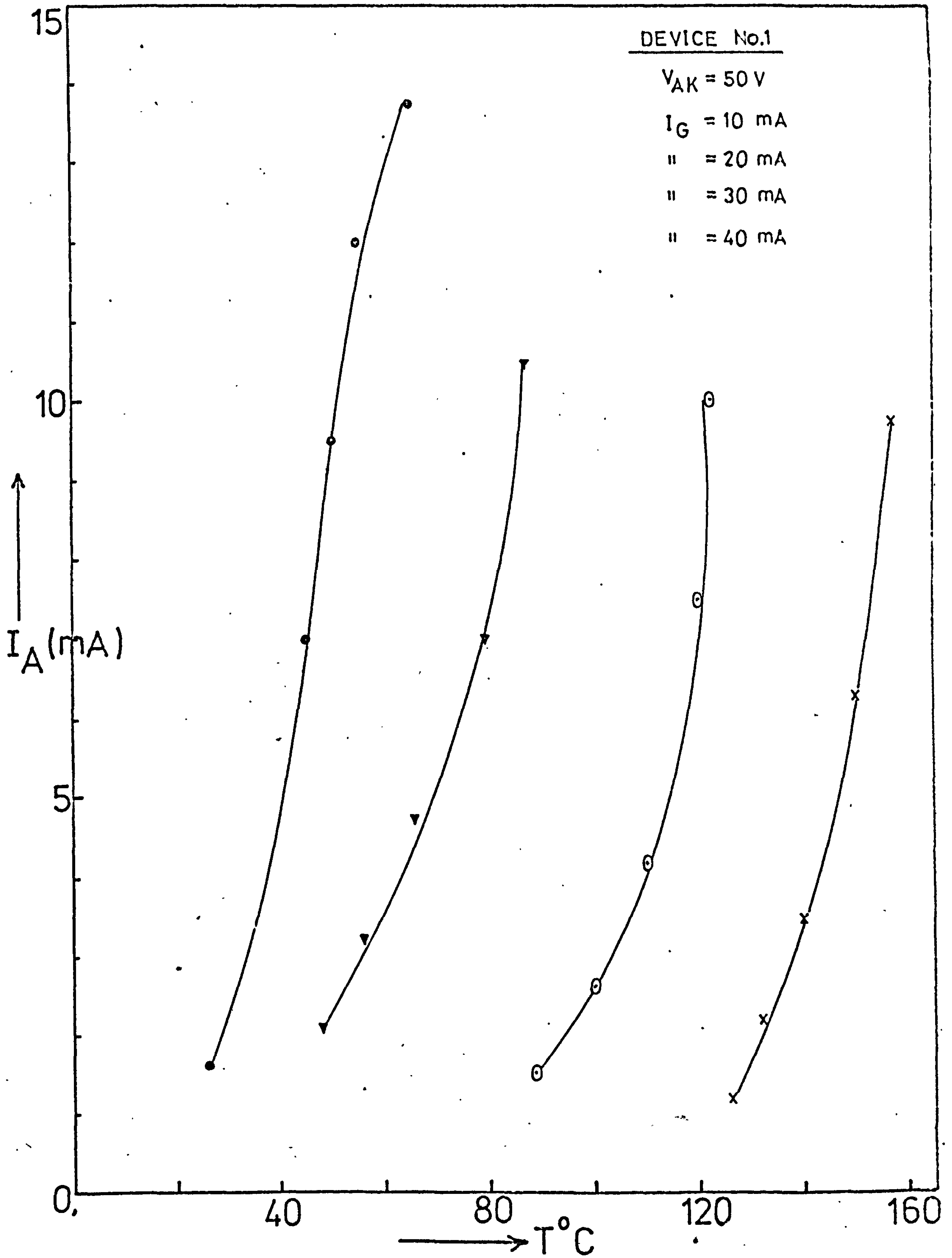


Figure (4-17) Anode current as a function of temperature for a medium-power thyristor.

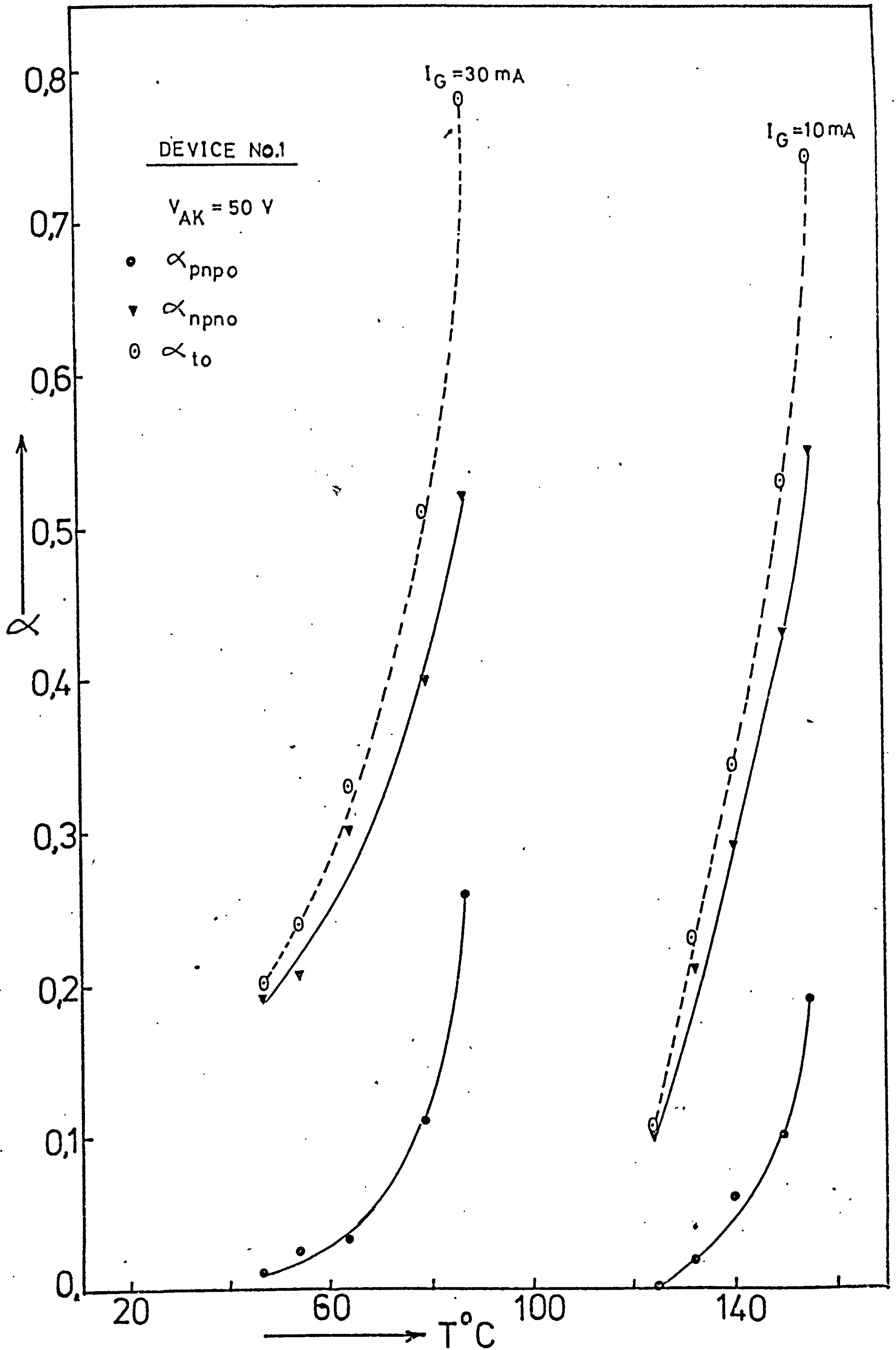


Figure (4-18) Current gain as a function of temperature for a medium-power thyristor (at fixed I_G).

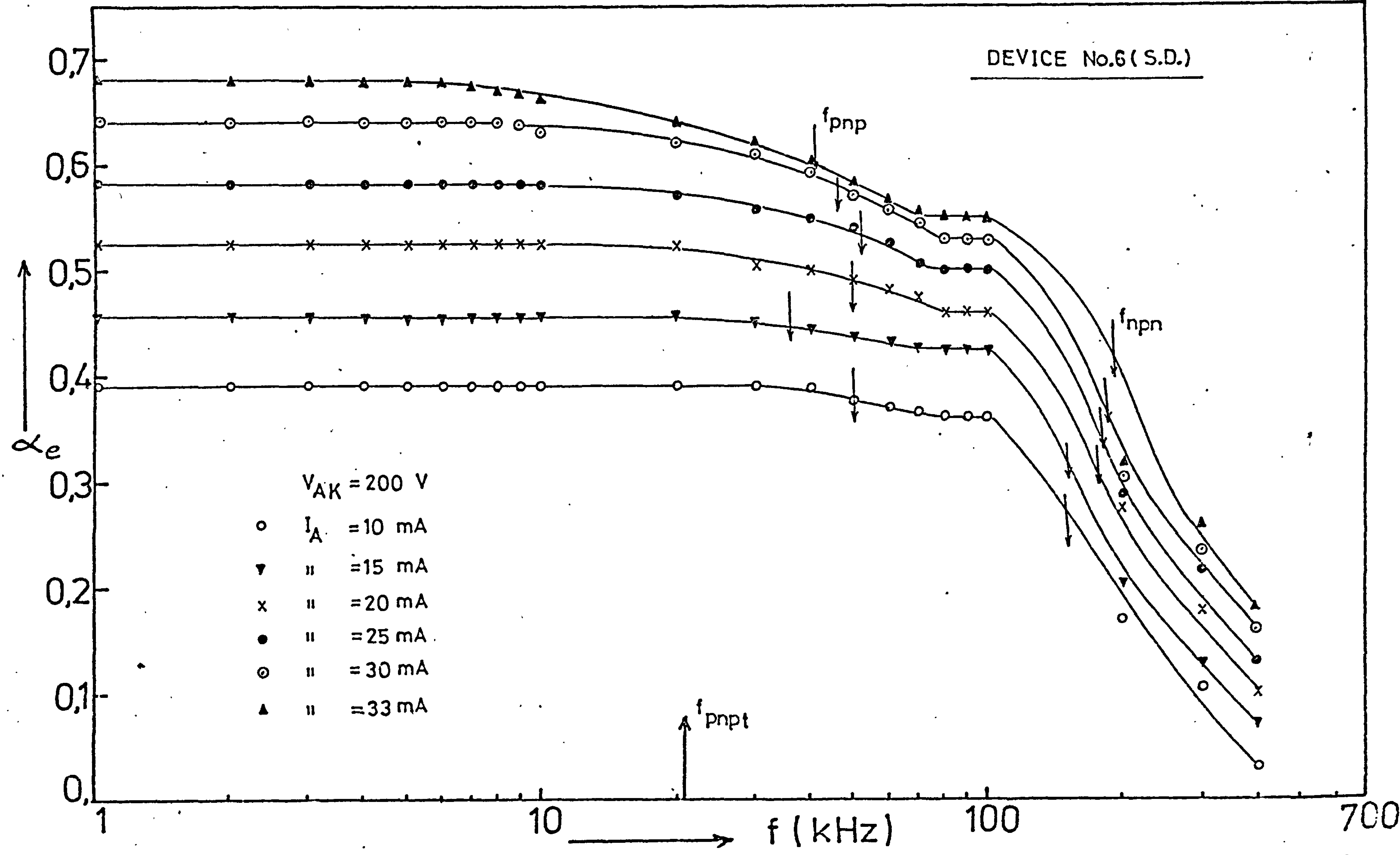


Figure (5-1) Frequency-response of current gain of a medium-power thyristor (shorted-emitter).

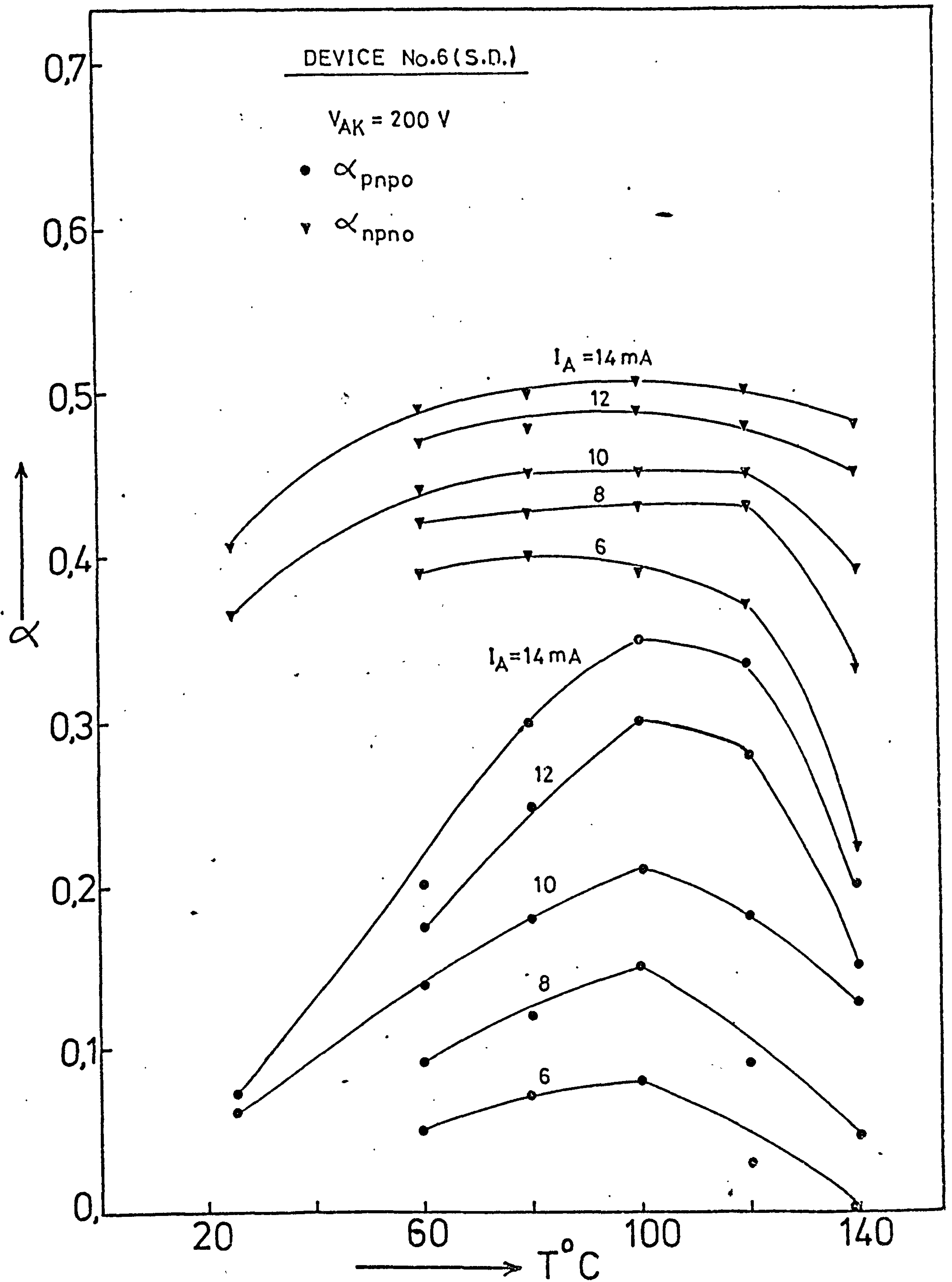


Figure (5-2) Current gain as a function of temperature for a medium-power thyristor (shorted-emitter).

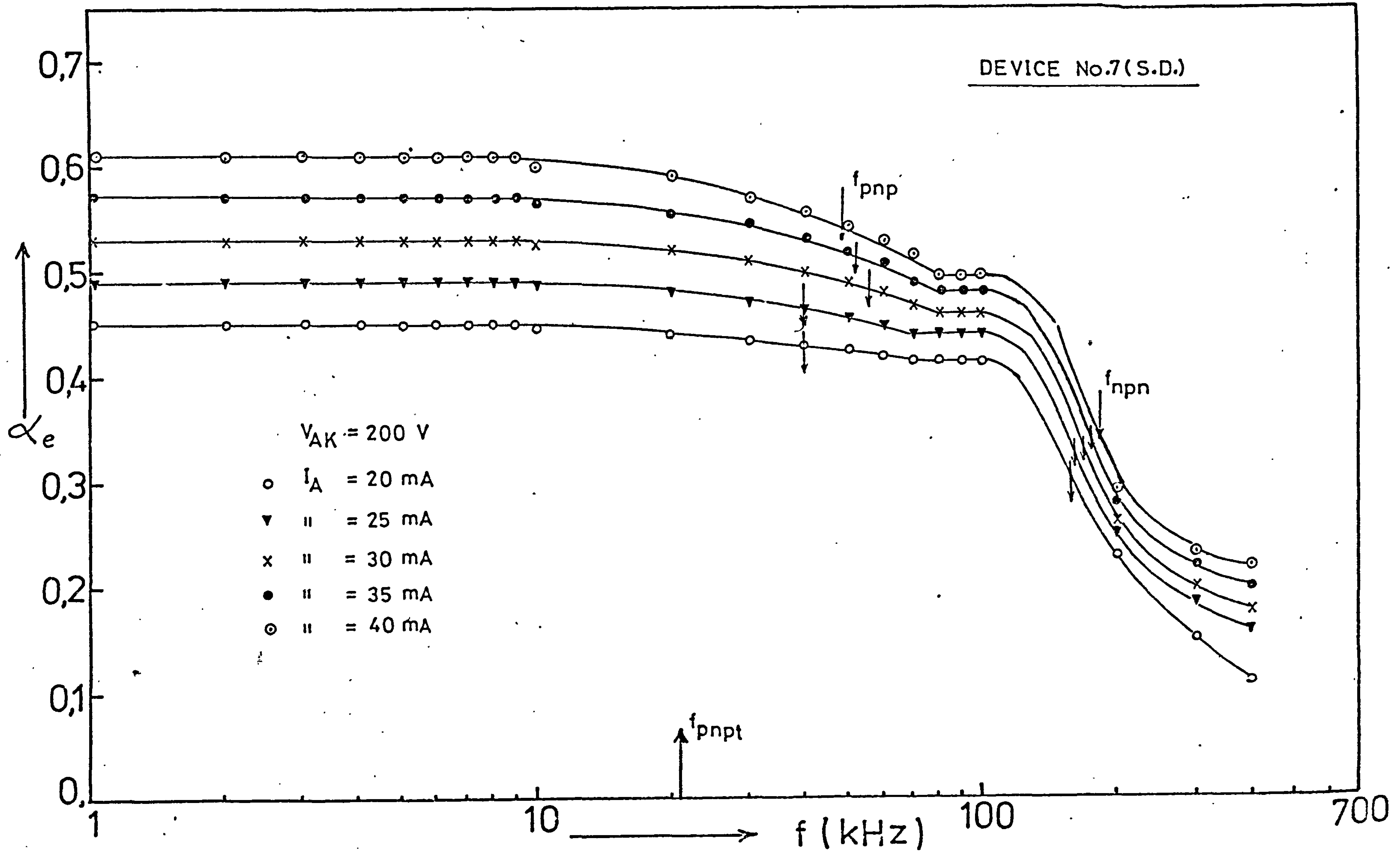


Figure (5-3) Frequency-response of current gain of a medium-power thyristor (shorted-emitter).

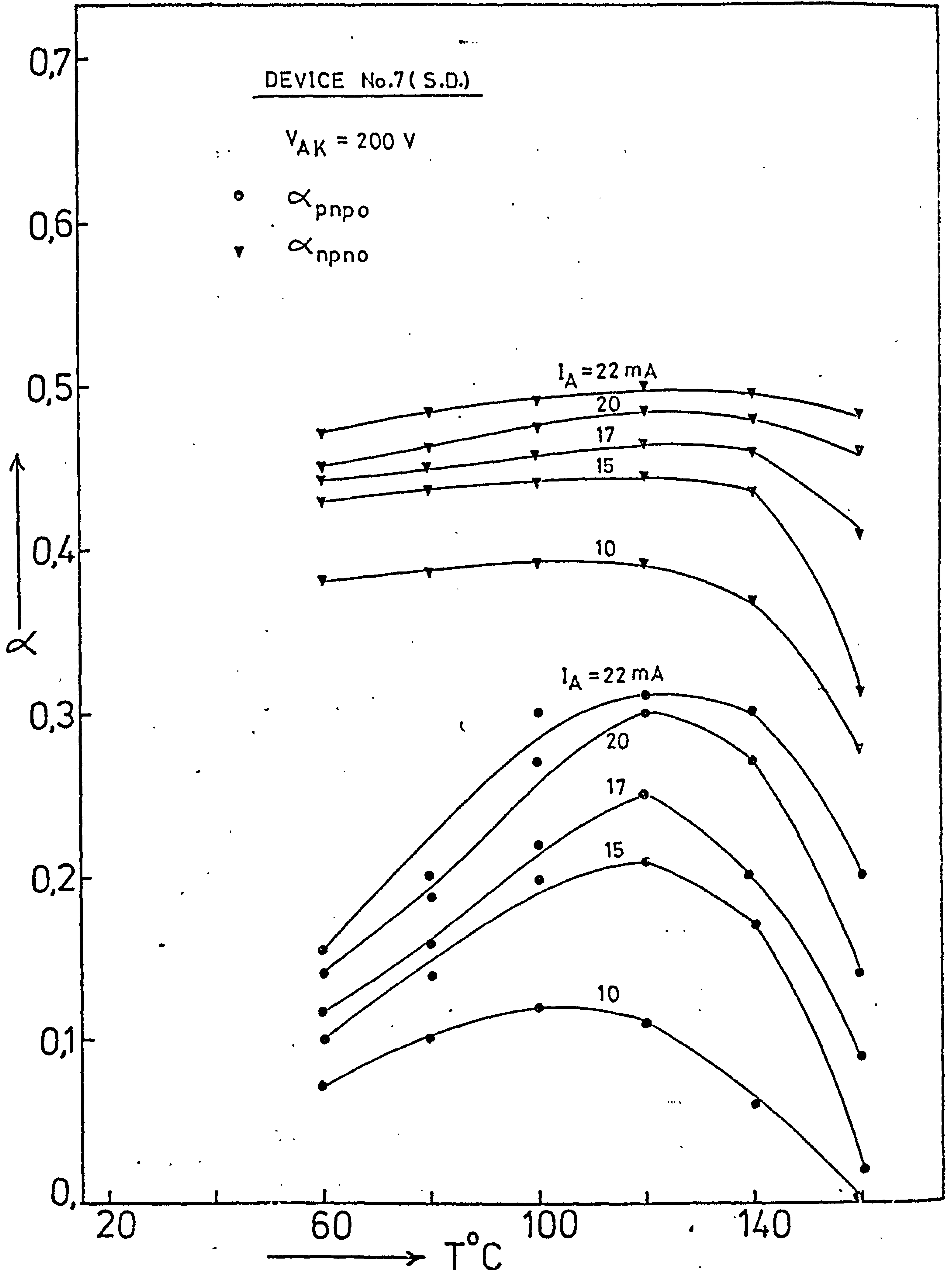


Figure (5-4) Current gain as a function of temperature for a medium-power thyristor (shorted-emitter).

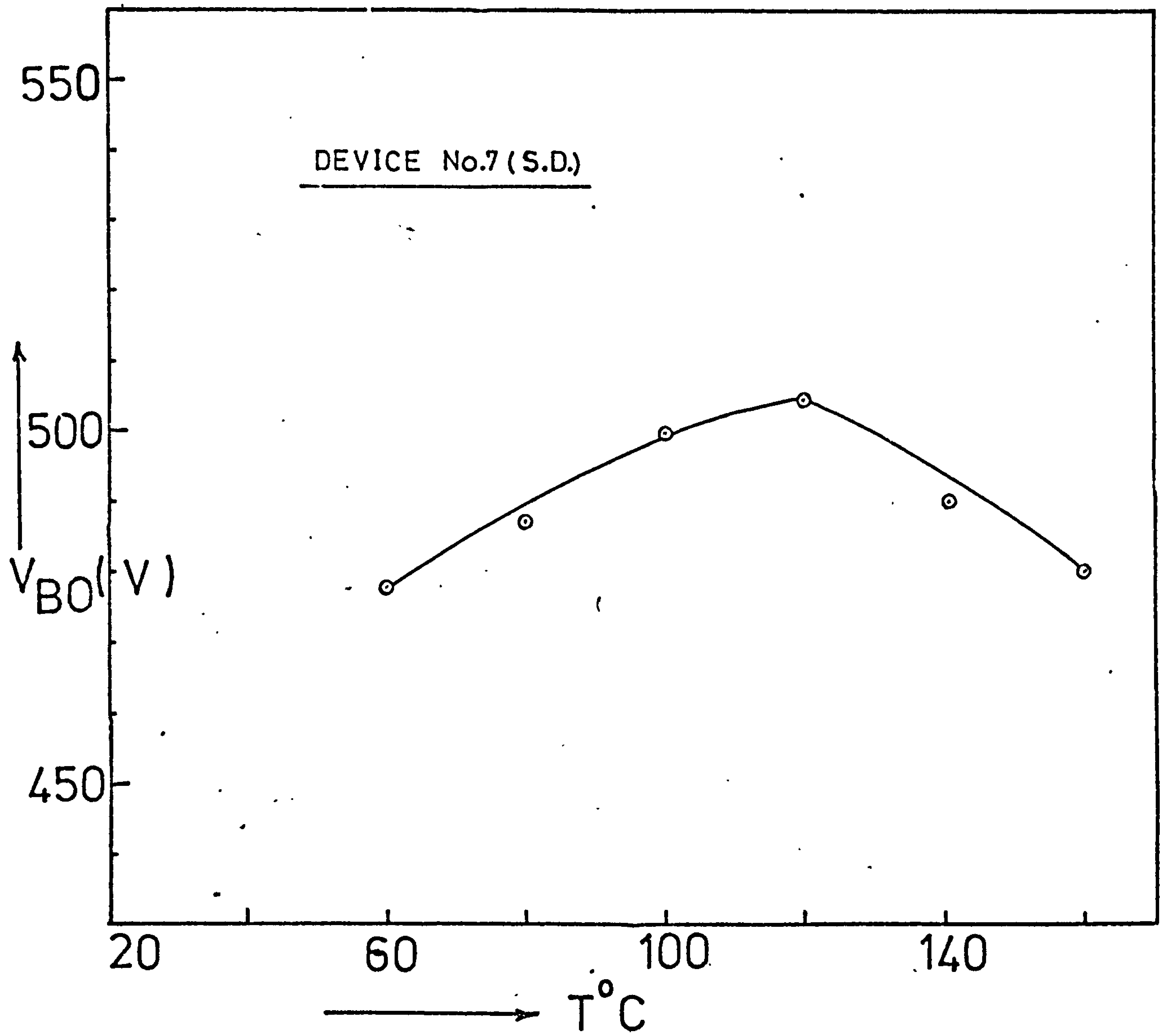


Figure (5-5) Breakover voltage as a function of temperature for a medium-power thyristor (shorted-emitter).

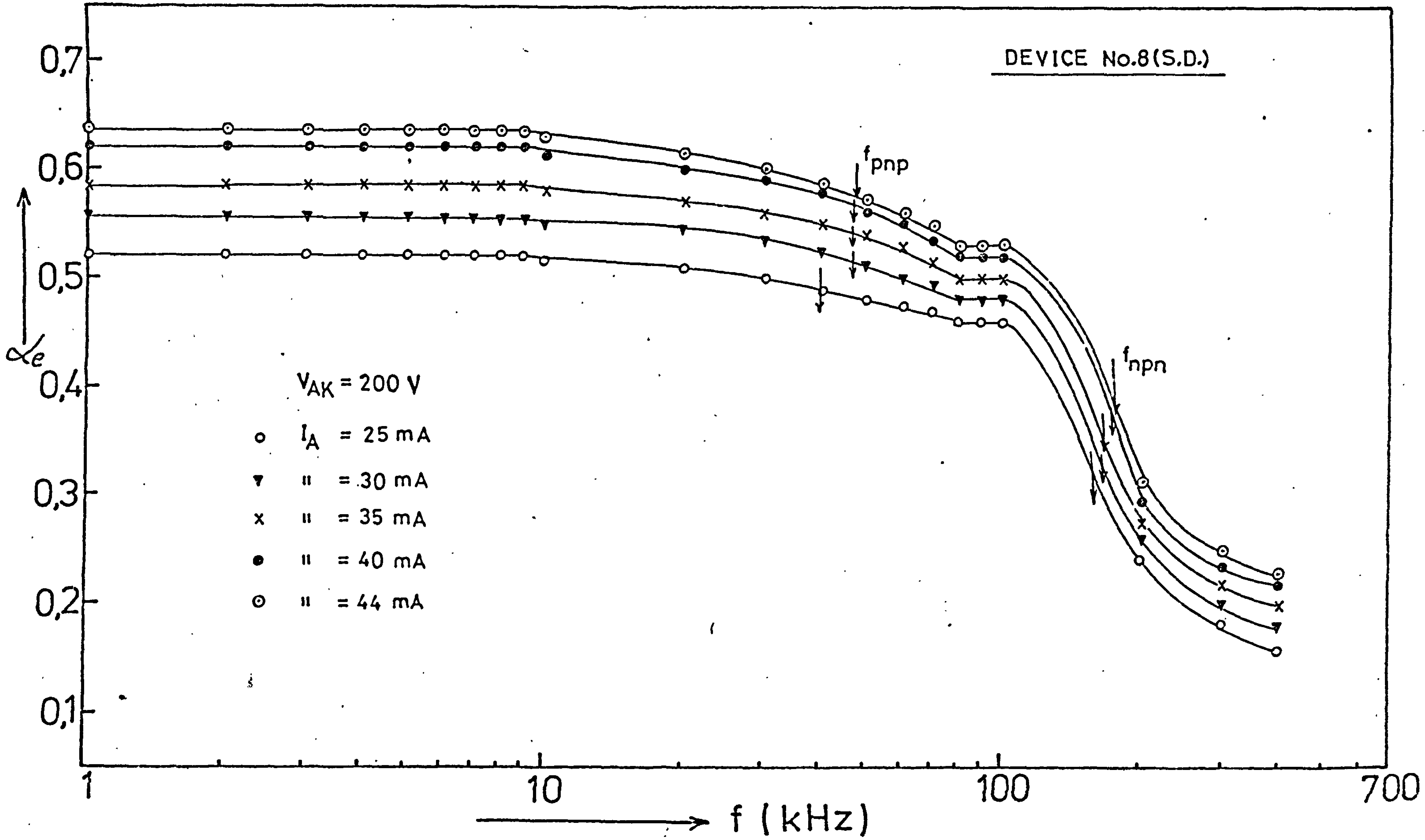


Figure (5-6) Frequency-response of current gain of a medium-power thyristor (shorted-emitter).

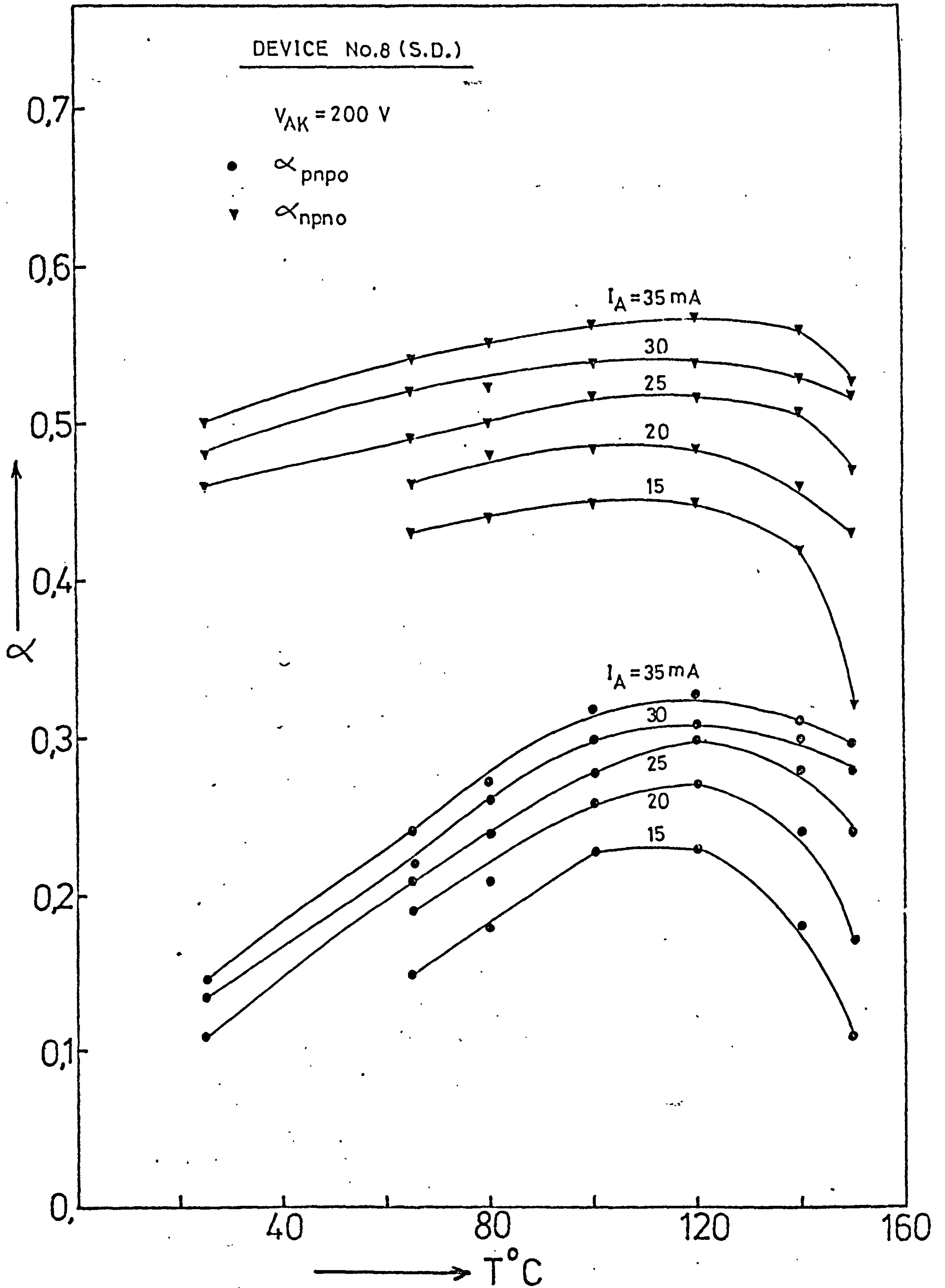


Figure (5-7) Current gain as a function of temperature for a medium-power thyristor (shorted-emitter).

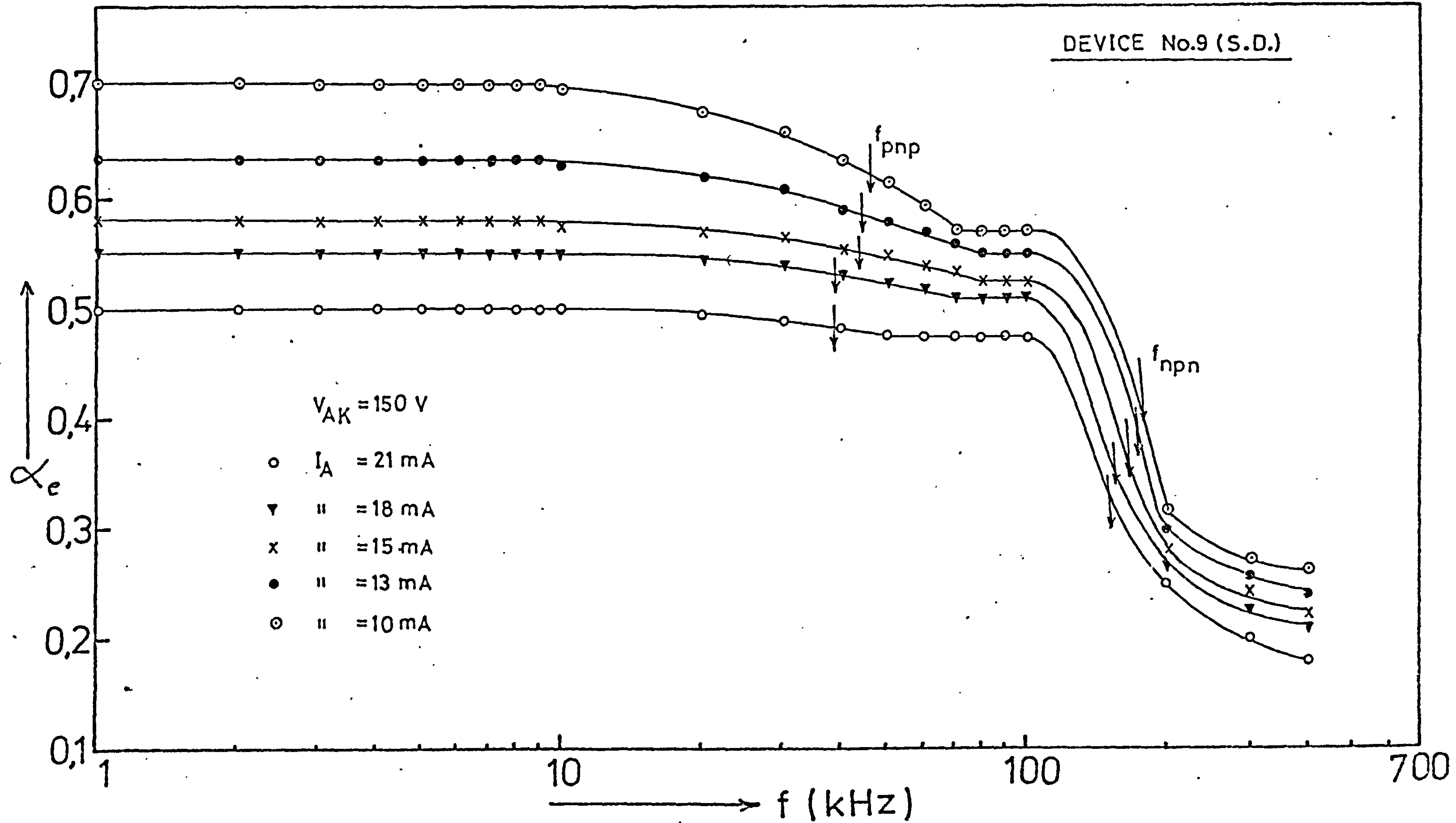


Figure (5-8) Frequency-response of current gain of a medium-power thyristor (shorted-emitter).

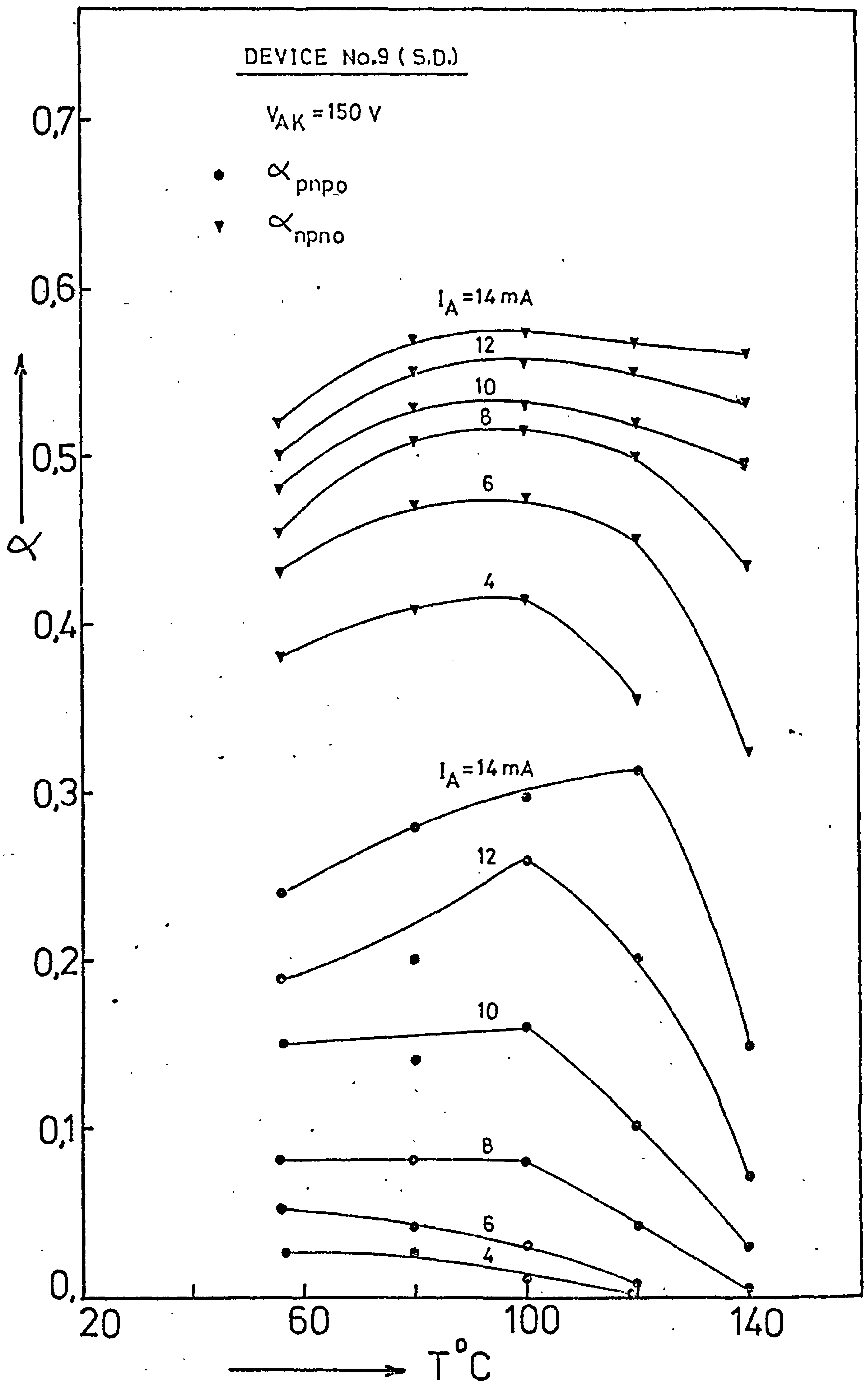


Figure (5-9) Current gain as a function of temperature for a medium-power thyristor (shorted-emitter).

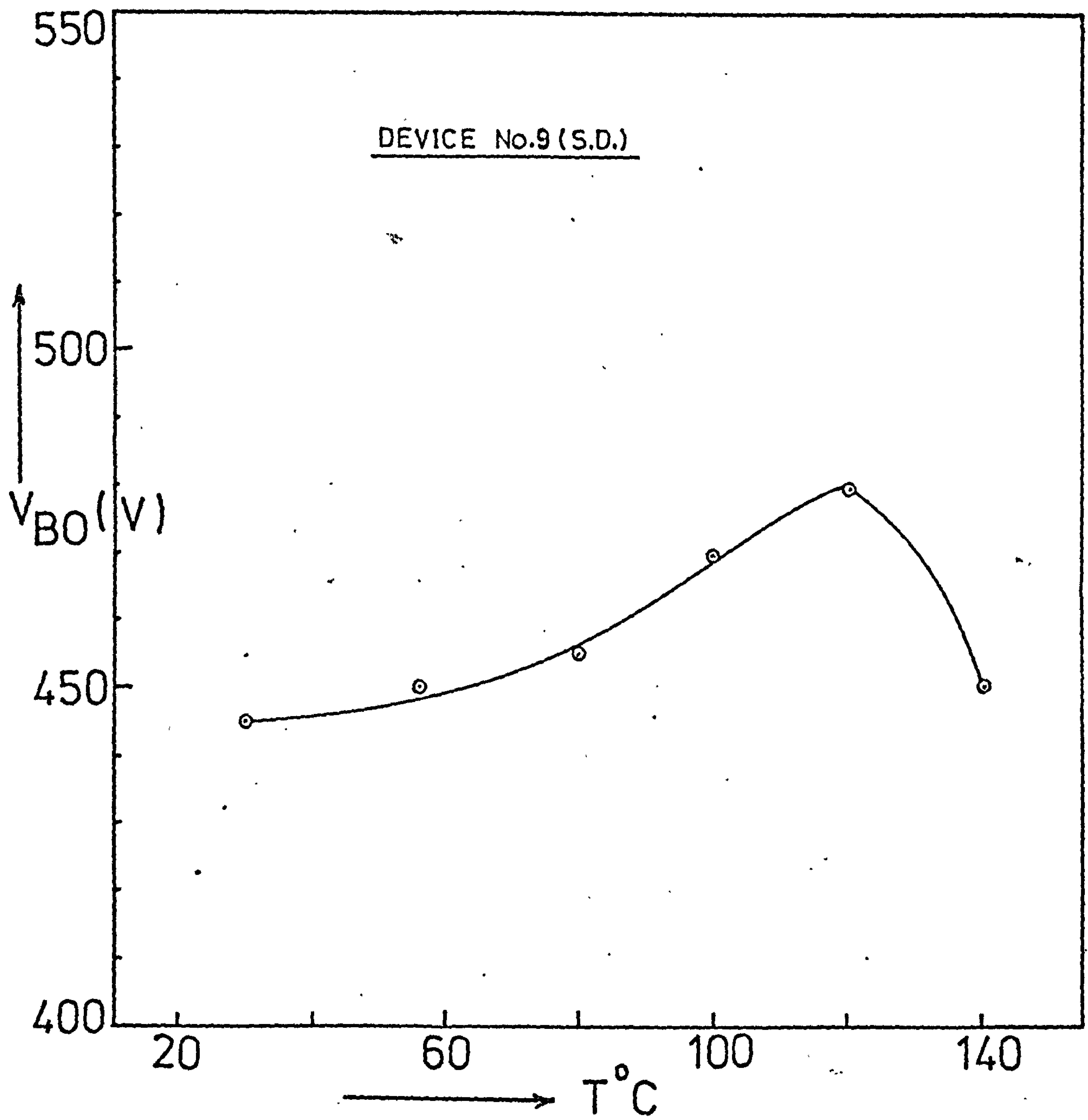


Figure (5-10) Breakover voltage as a function of temperature for a medium-power thyristor (shorted-emitter).

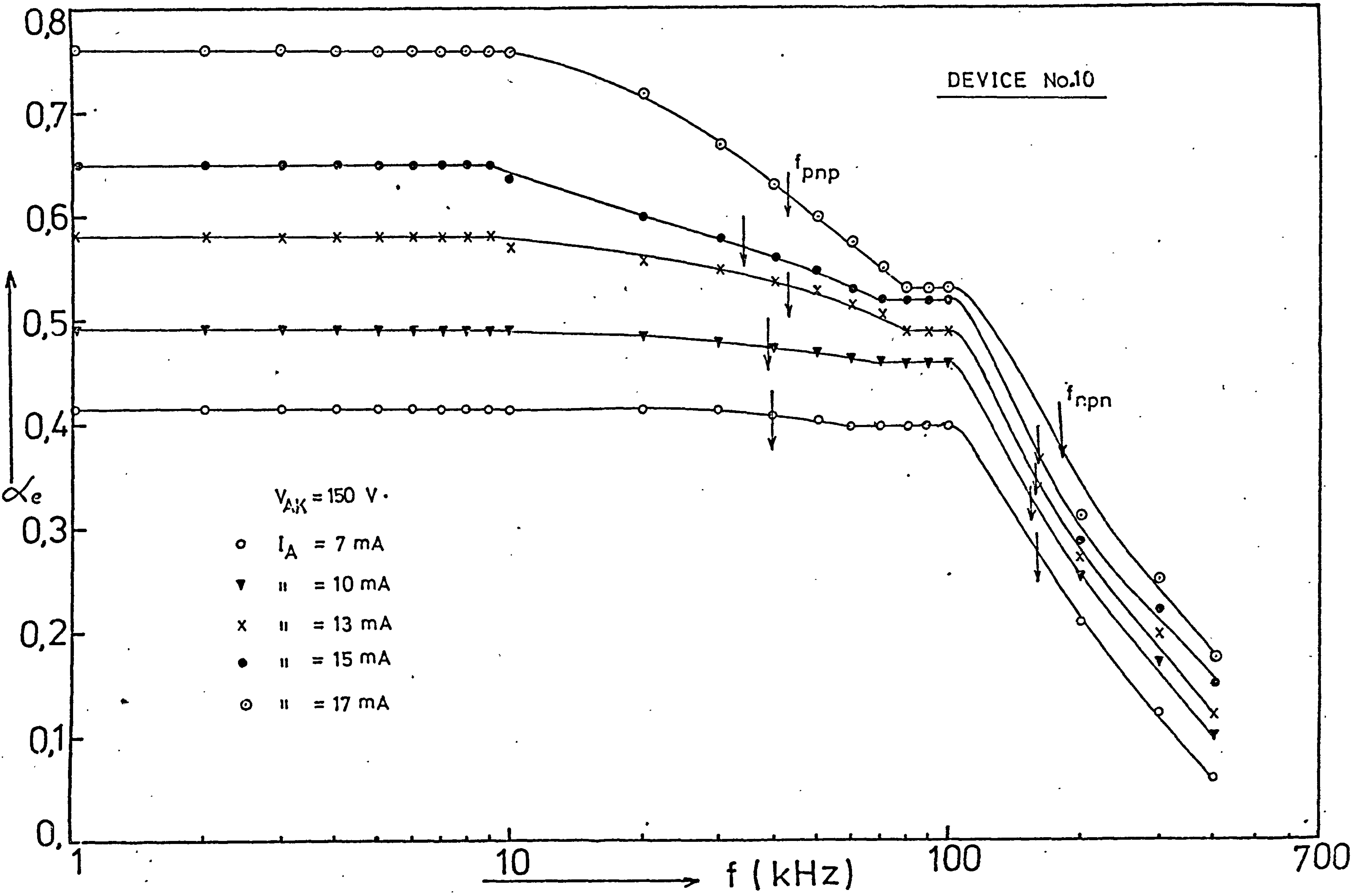


Figure (5-11) Frequency-response of current gain of a medium-power thyristor (not shorted-emitter).

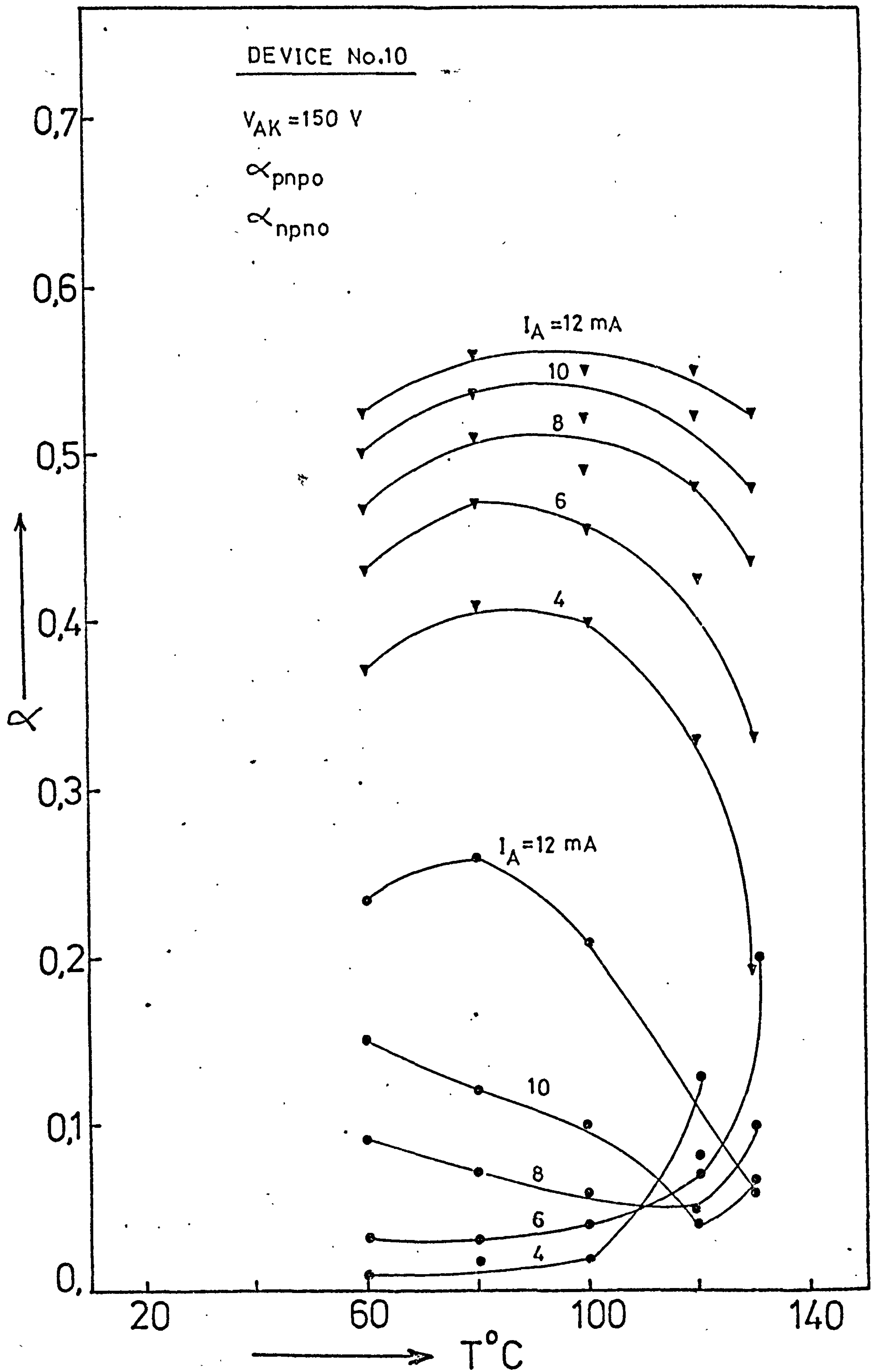


Figure (5-12) Current gain as a function of temperature for a medium-power thyristor (not shorted-emitter).

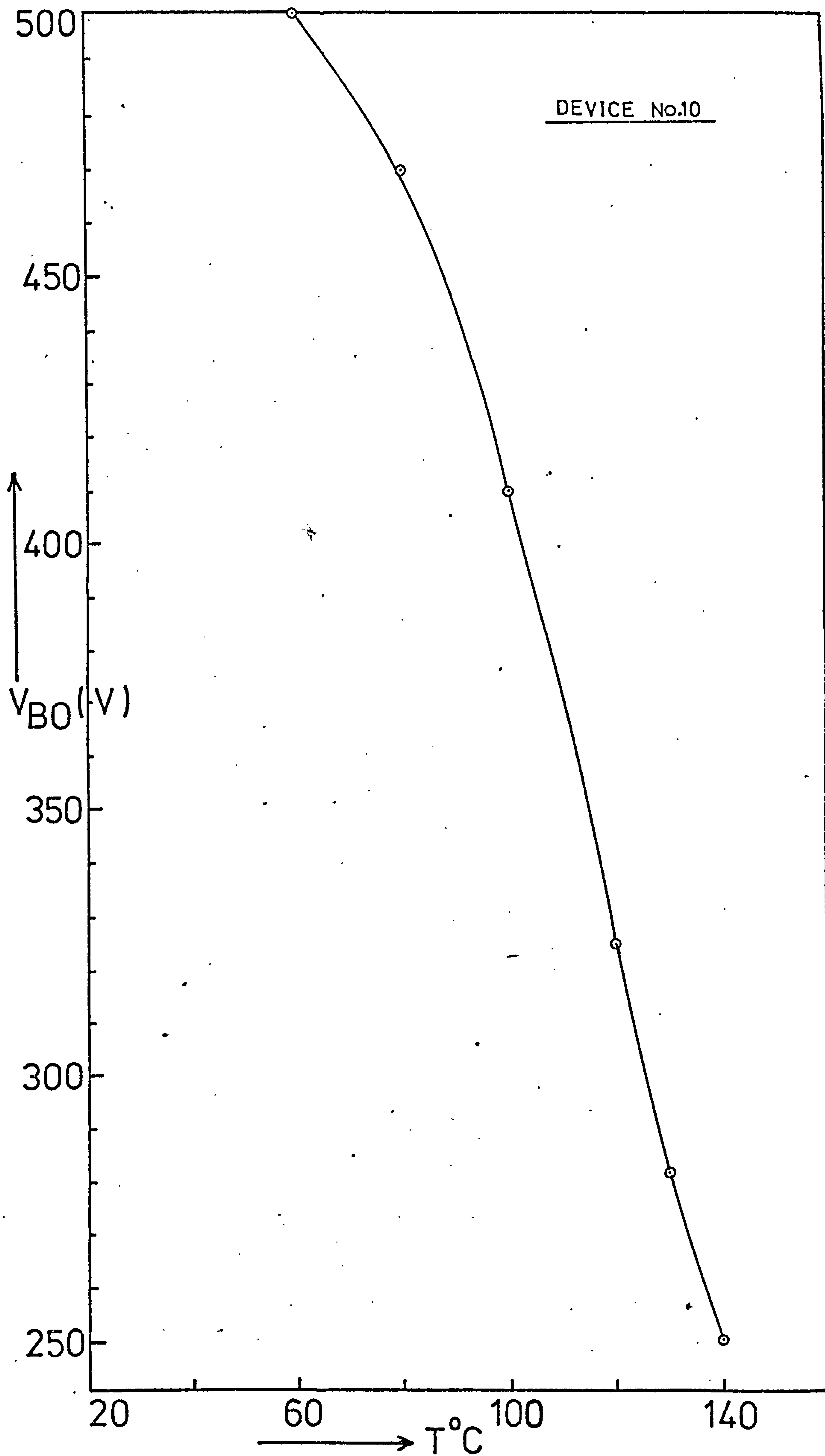


Figure (5-13) Breakover voltage as a function of temperature for a medium-power thyristor (not shorted-emitter).

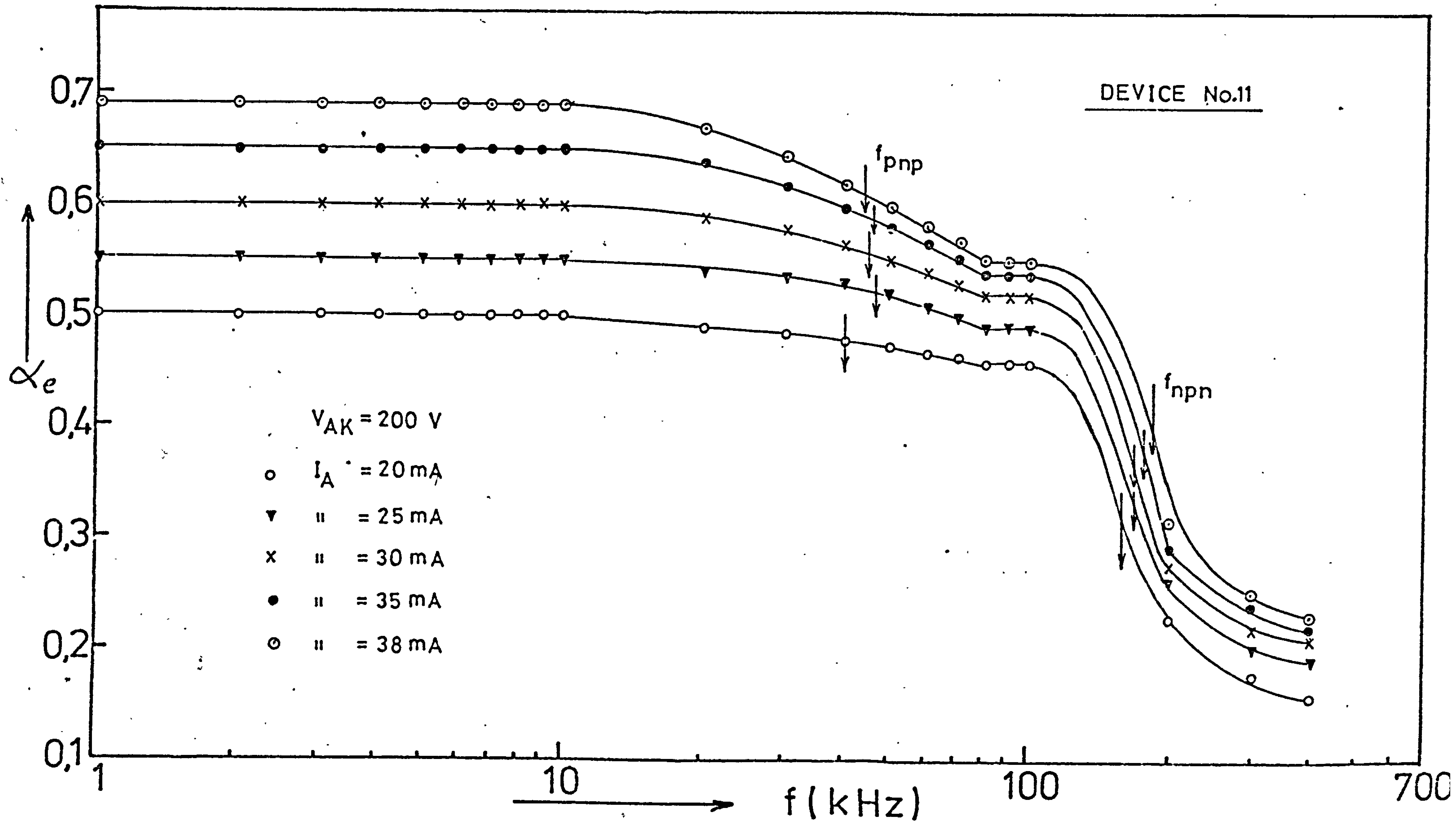


Figure (5-14) Frequency-response of current gain of a medium-power thyristor (not shorted-emitter).

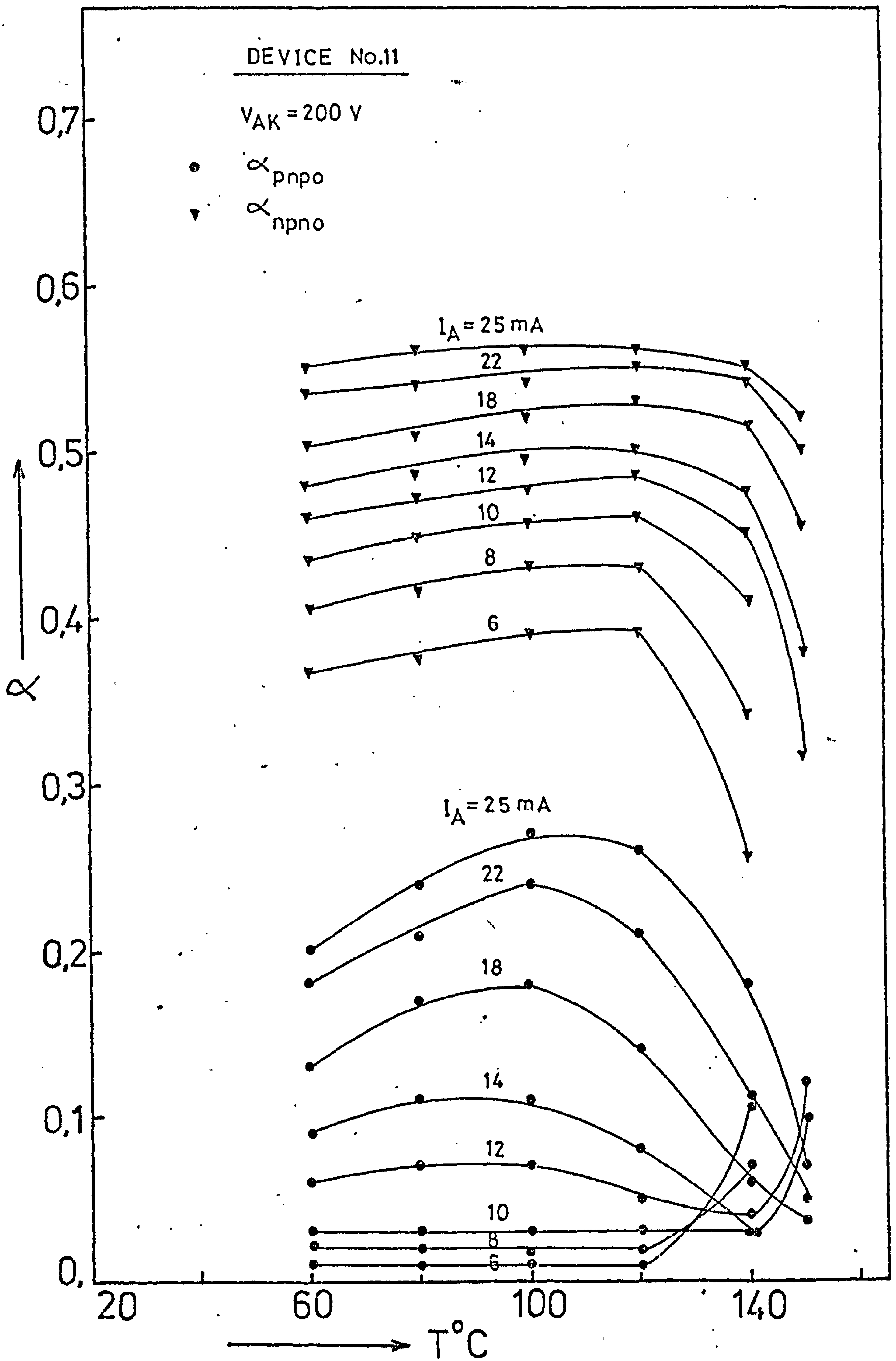


Figure (5-15) Current gain as a function of temperature for a medium-power thyristor (not shorted-emitter).

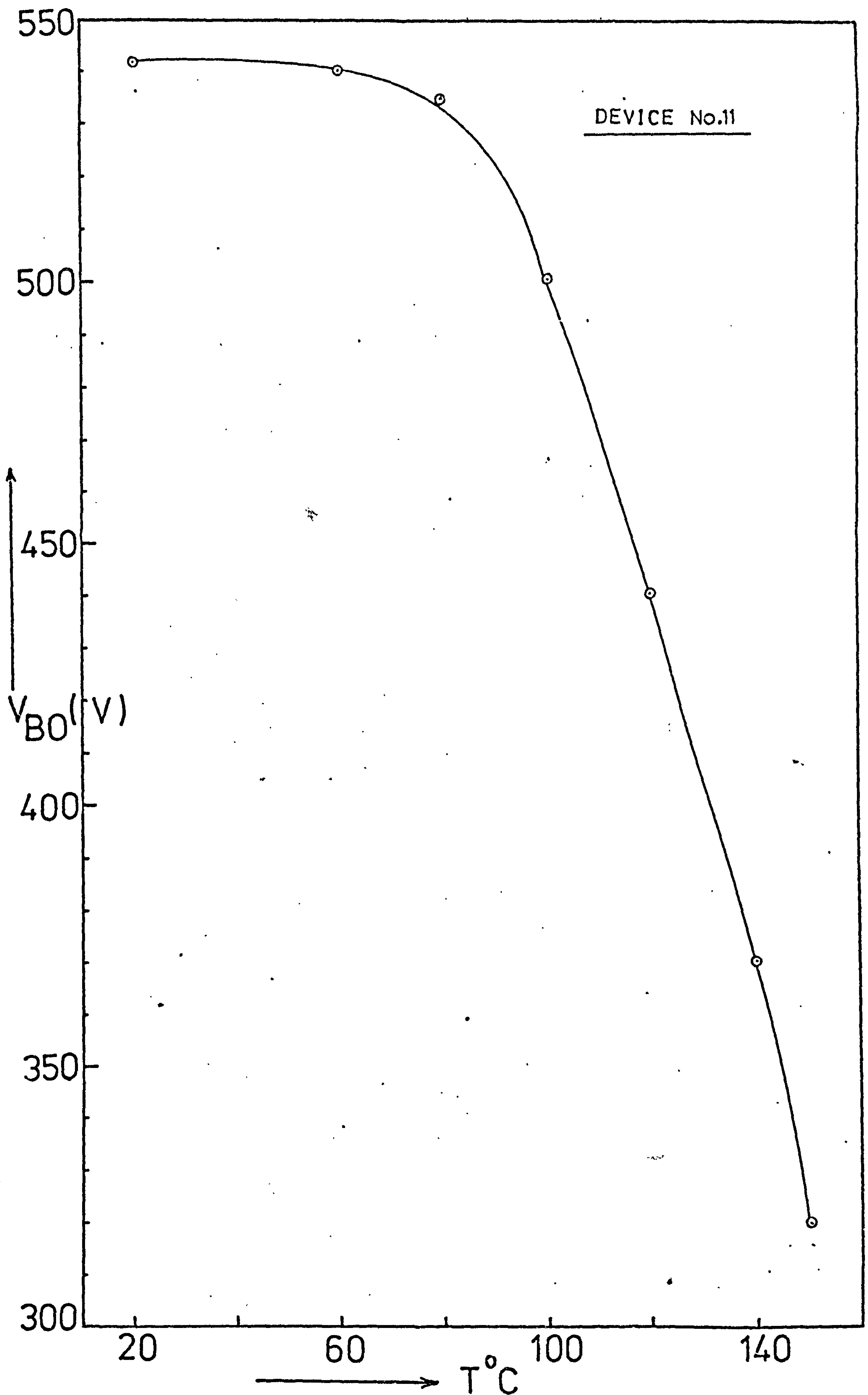


Figure (5-16) Breakover voltage as a function of temperature for a medium-power thyristor (not shorted-emitter).

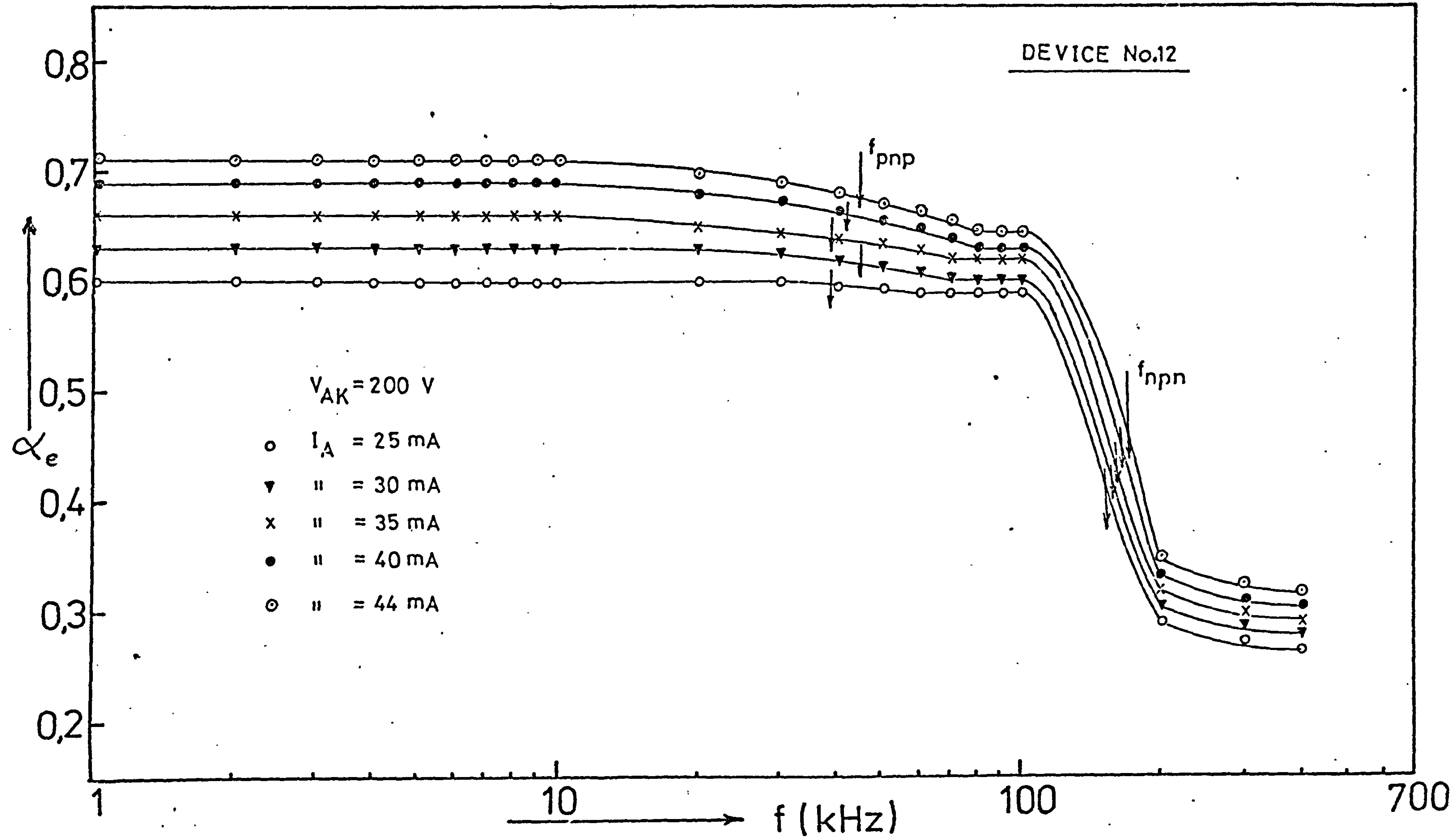


Figure (5-17) Frequency-response of current gain of a medium-power thyristor (not shorted-emitter).

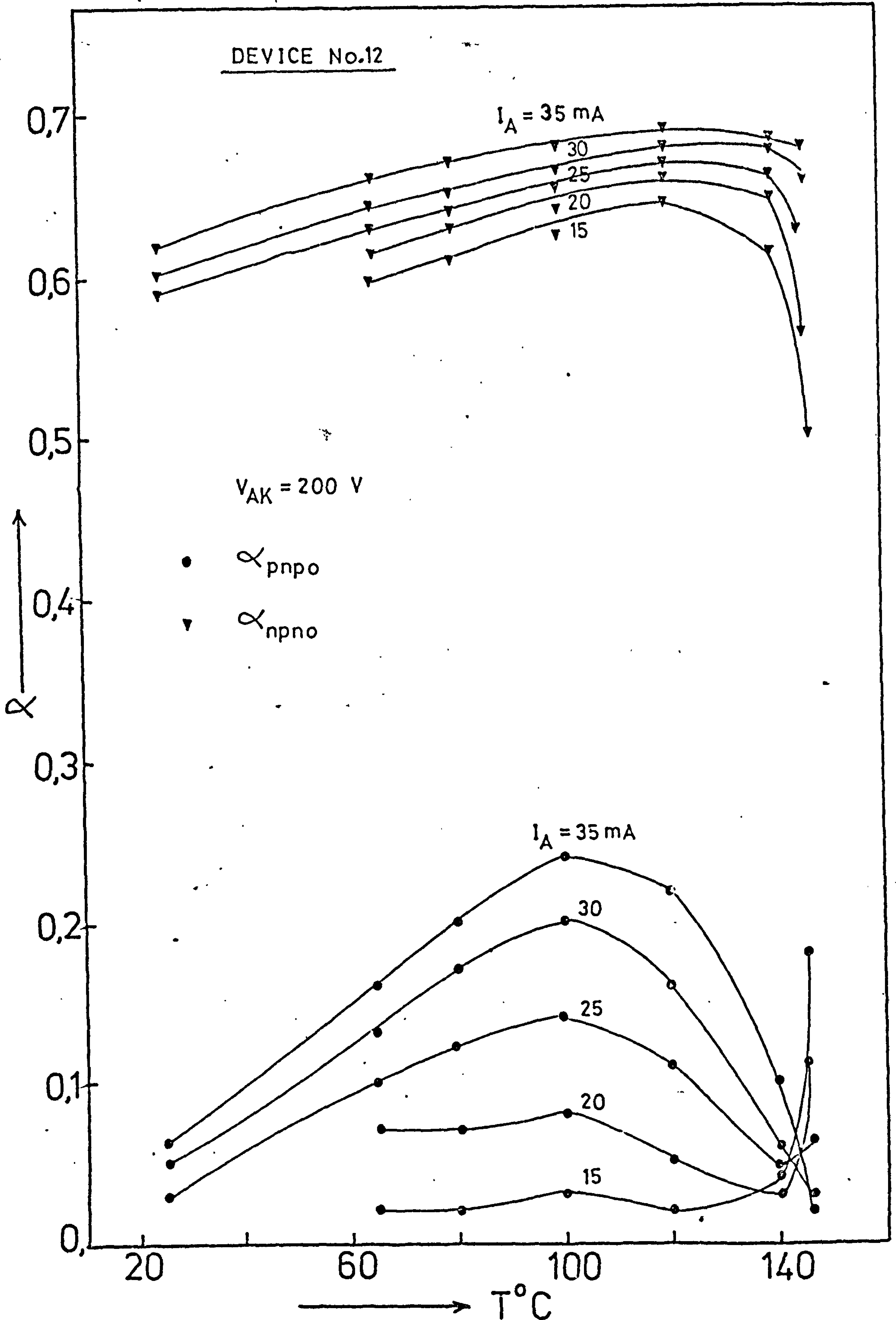


Figure (5-18) Current gain as a function of temperature for a medium-power thyristor (not shorted-emitter).

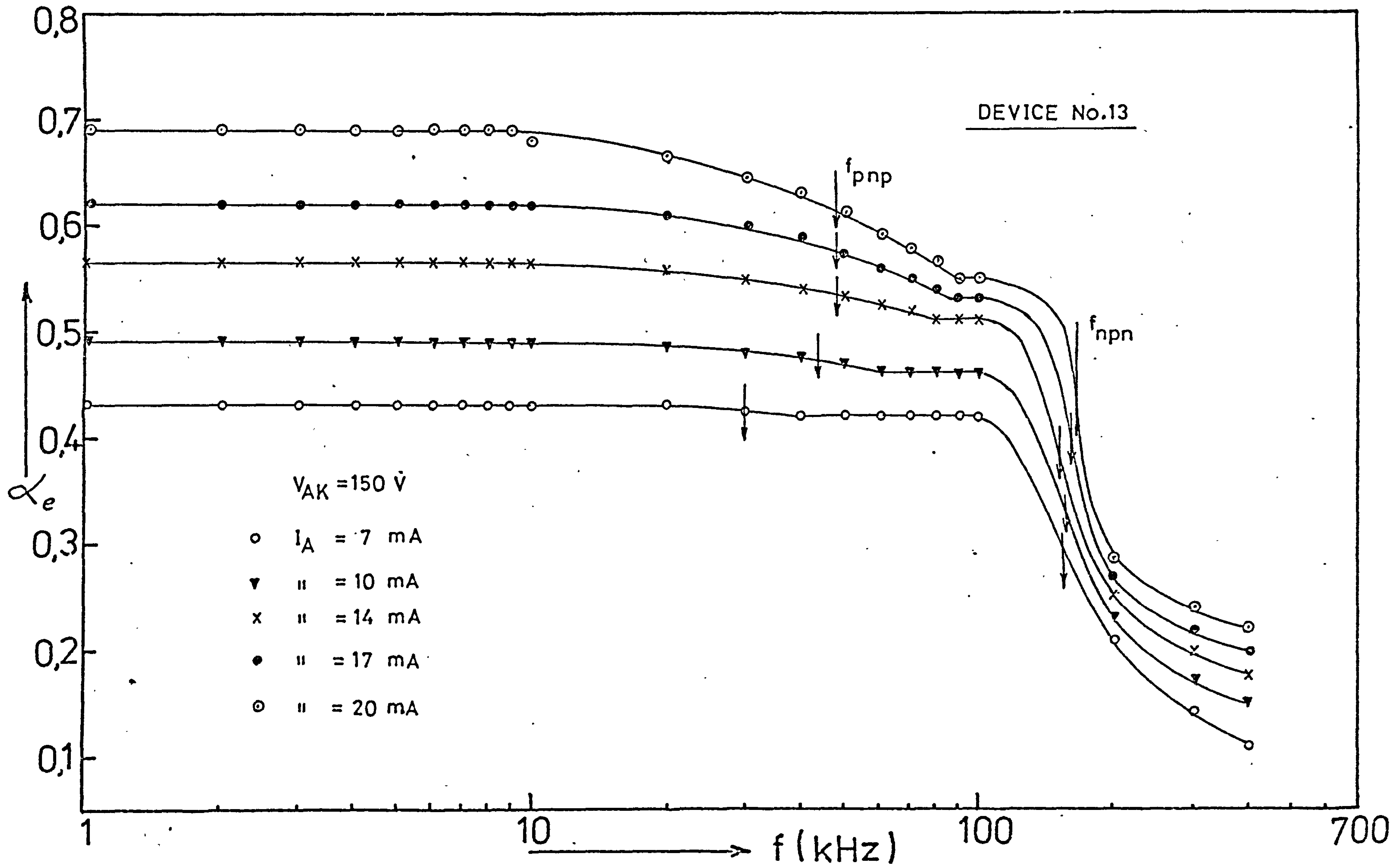


Figure (5-19) Frequency-response of current gain of a medium-power thyristor (not [illegible]

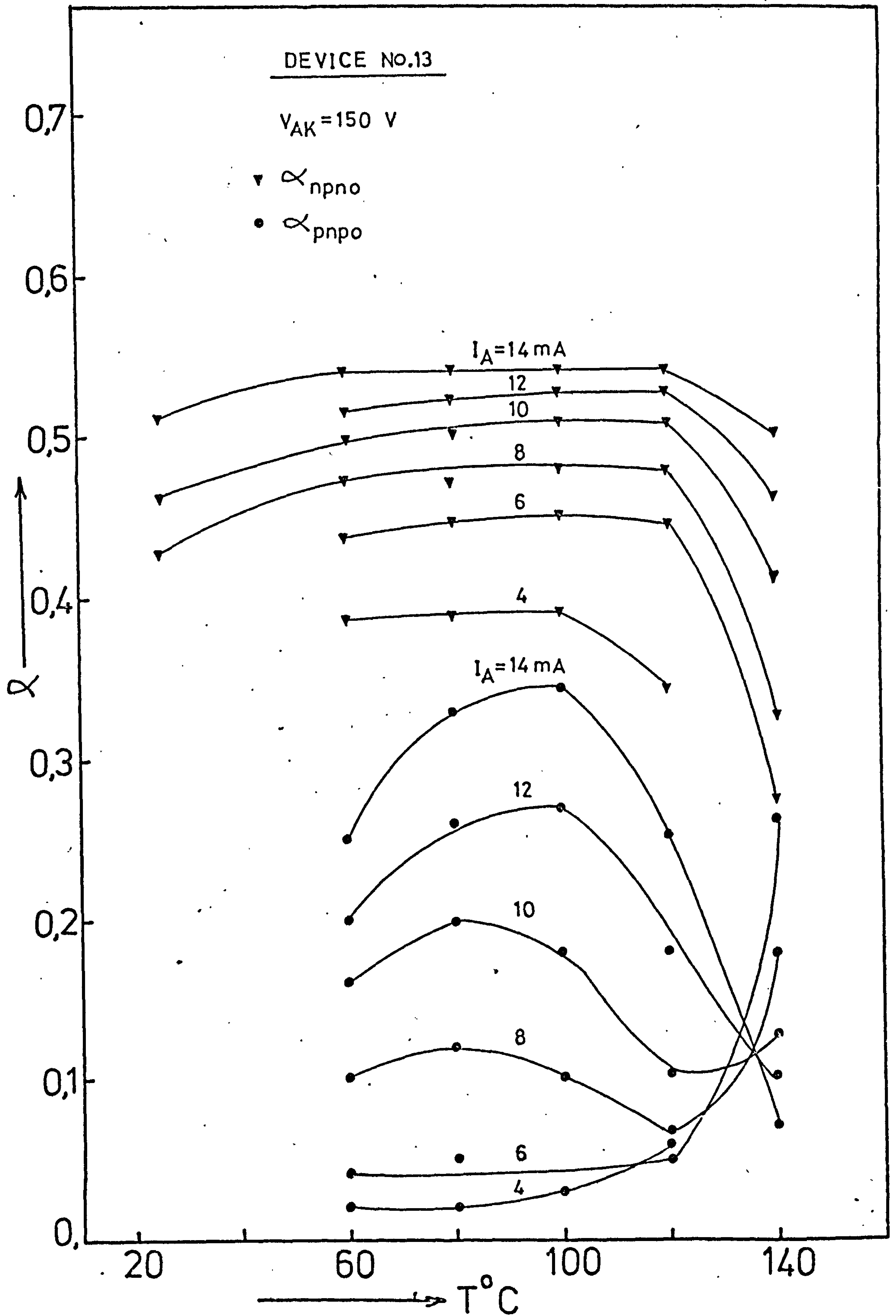
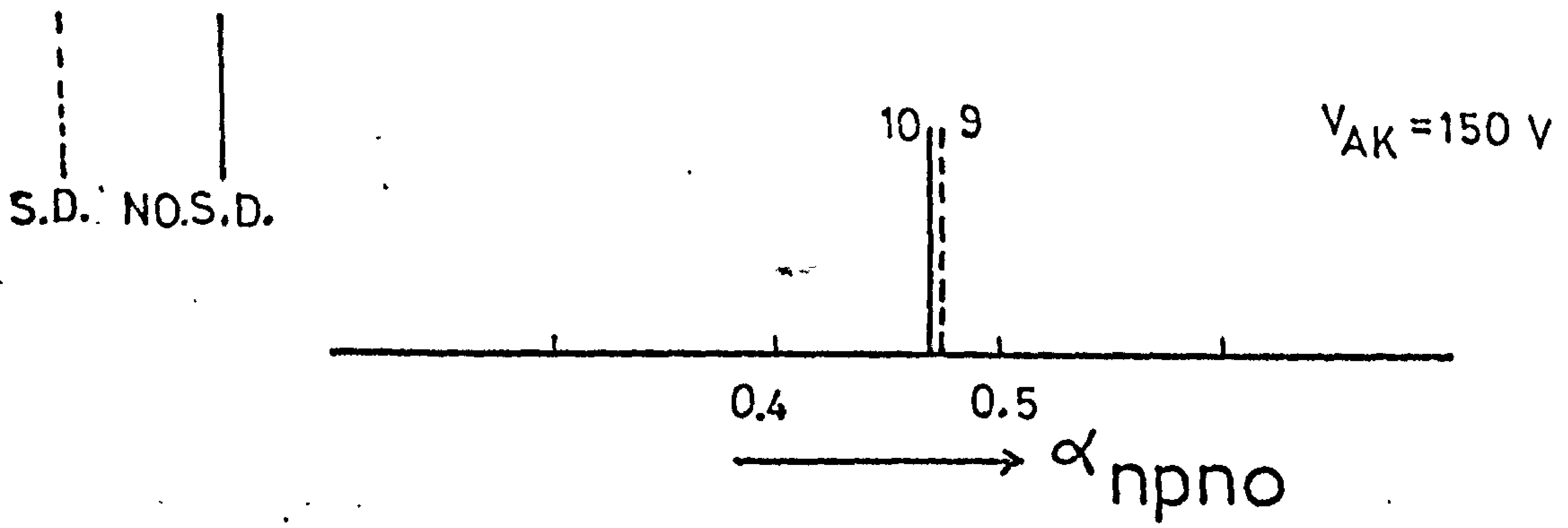
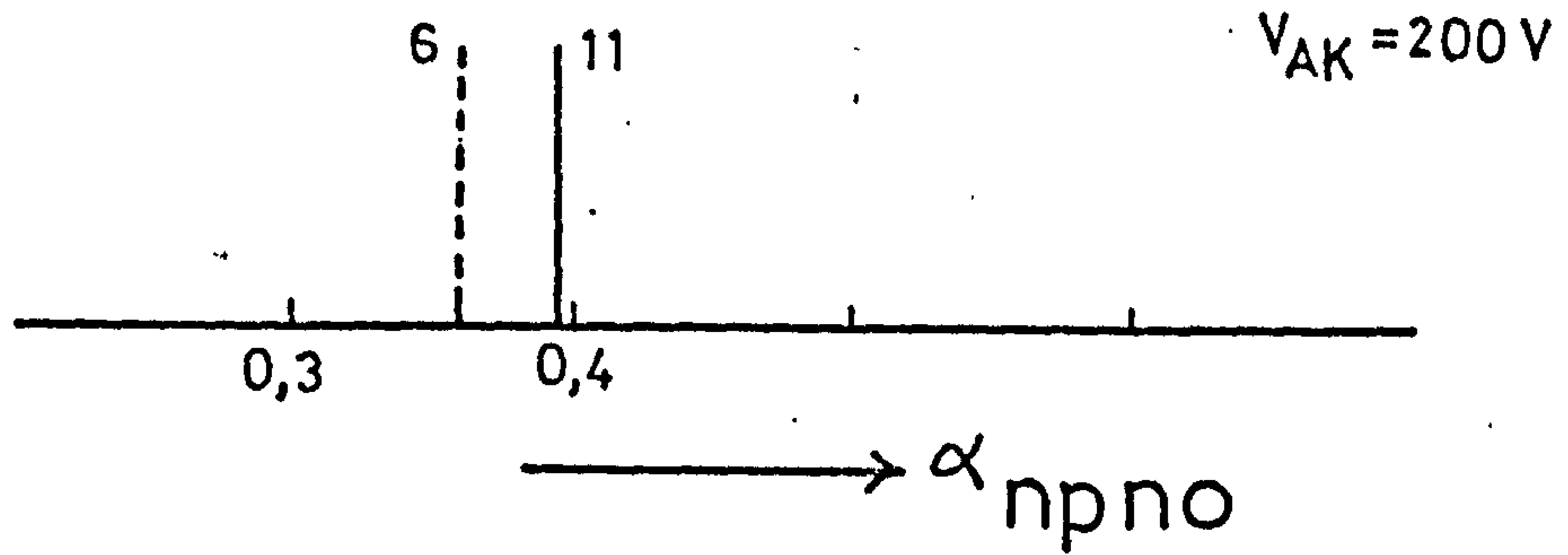


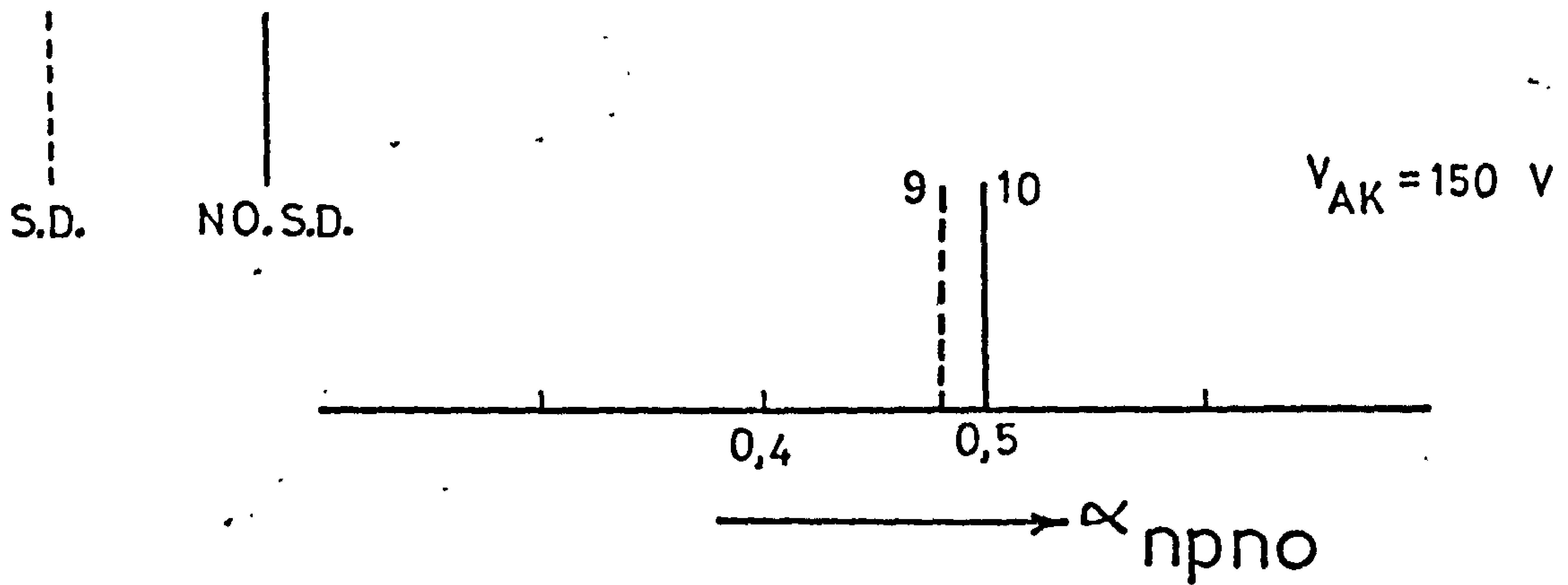
Figure (5-20) Current gain as a function of temperature for a medium-power thyristor (not shorted-emitter).



Room Temp.

I_A =10 mA





$T = 60^{\circ}C$

I_A =10 mA

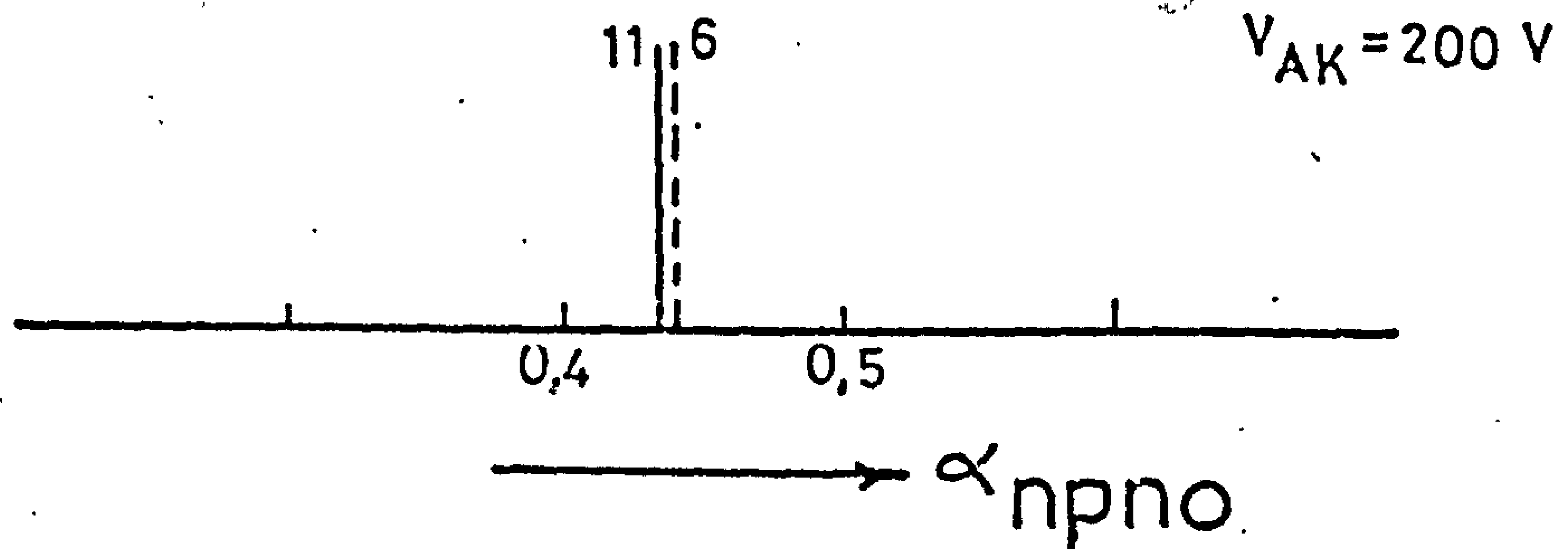
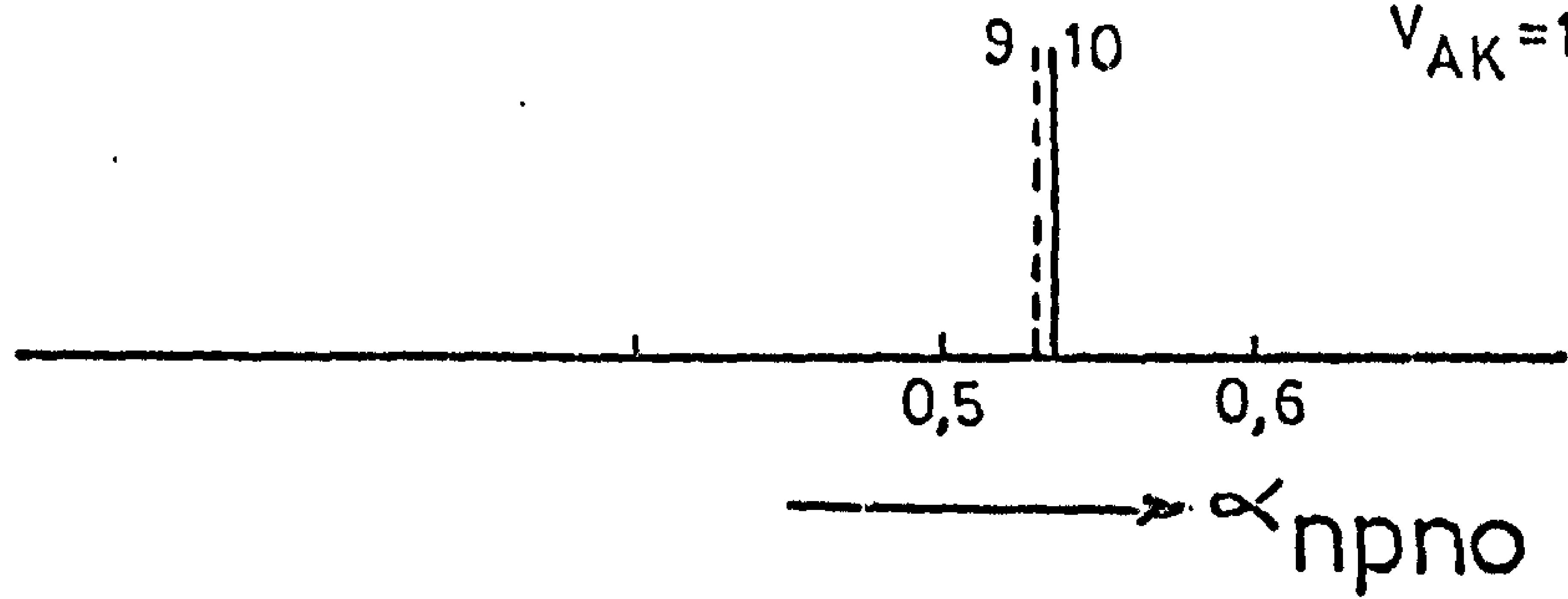


Figure (5-21) Histogrammatic diagram of current gain of NPN transistor section of thyristor at different temperatures.

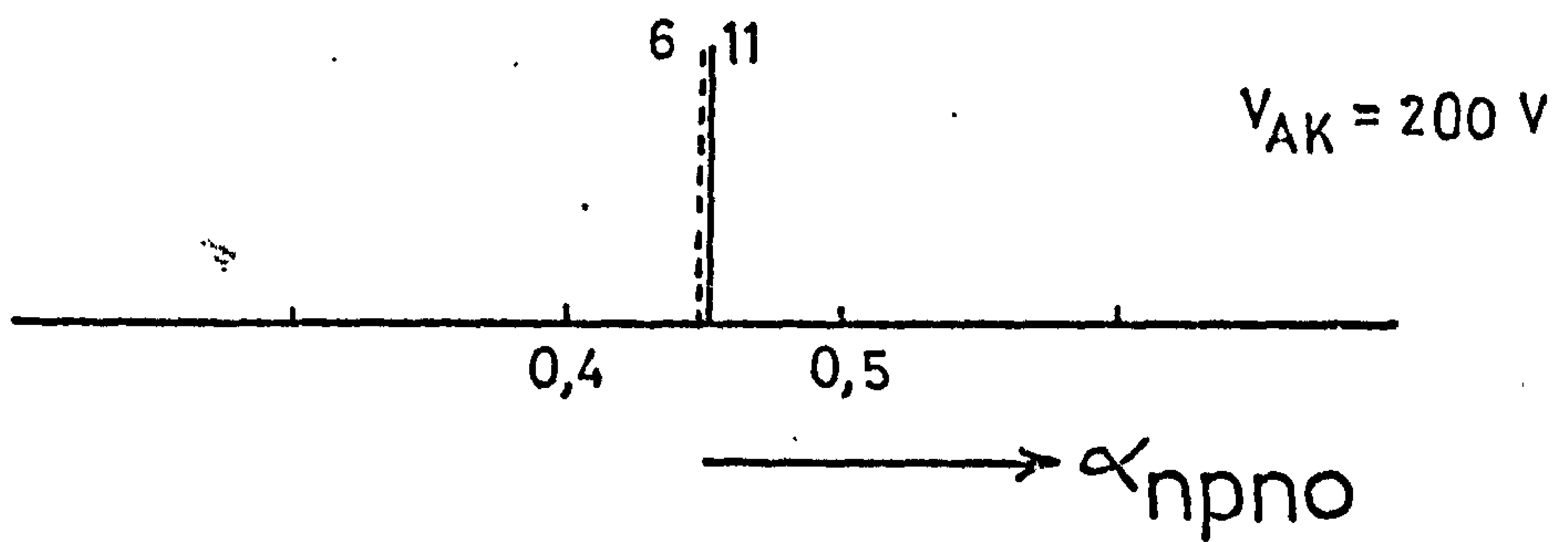
S.D NO.S.D.



$V_{AK} = 150$ V

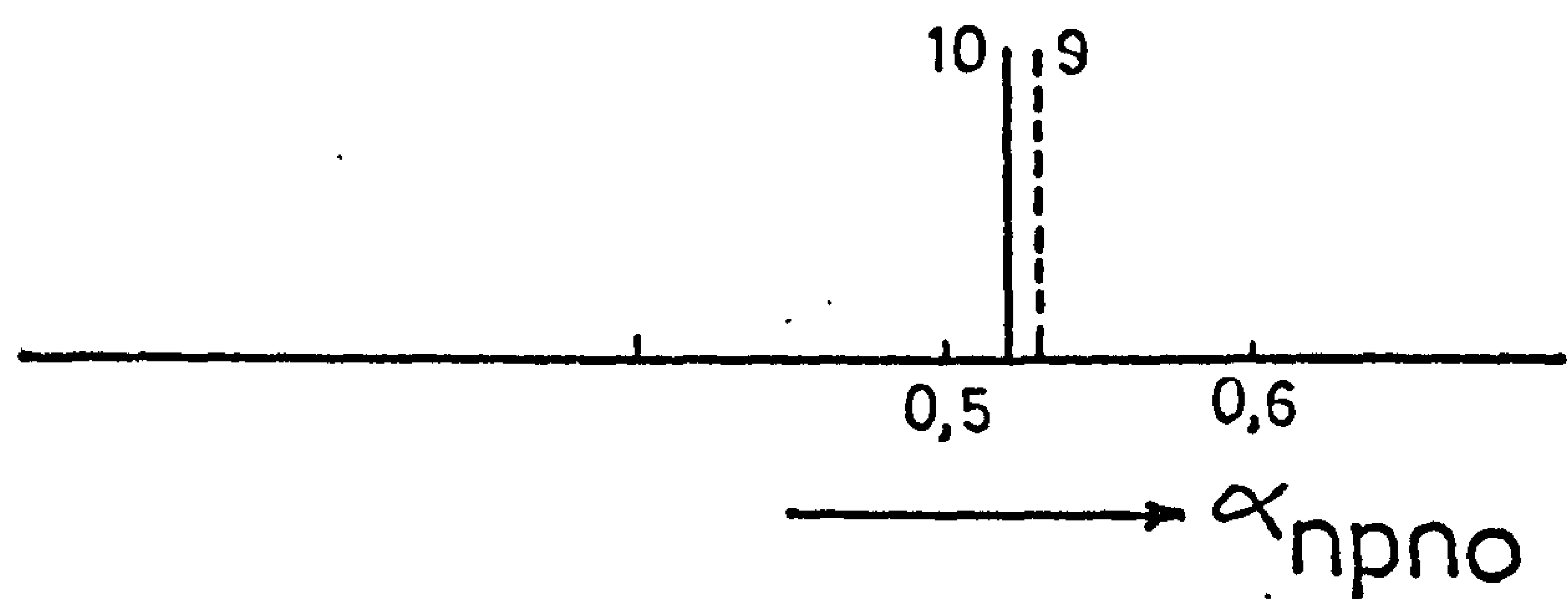
T = 80°C

$I_A = 10$ mA



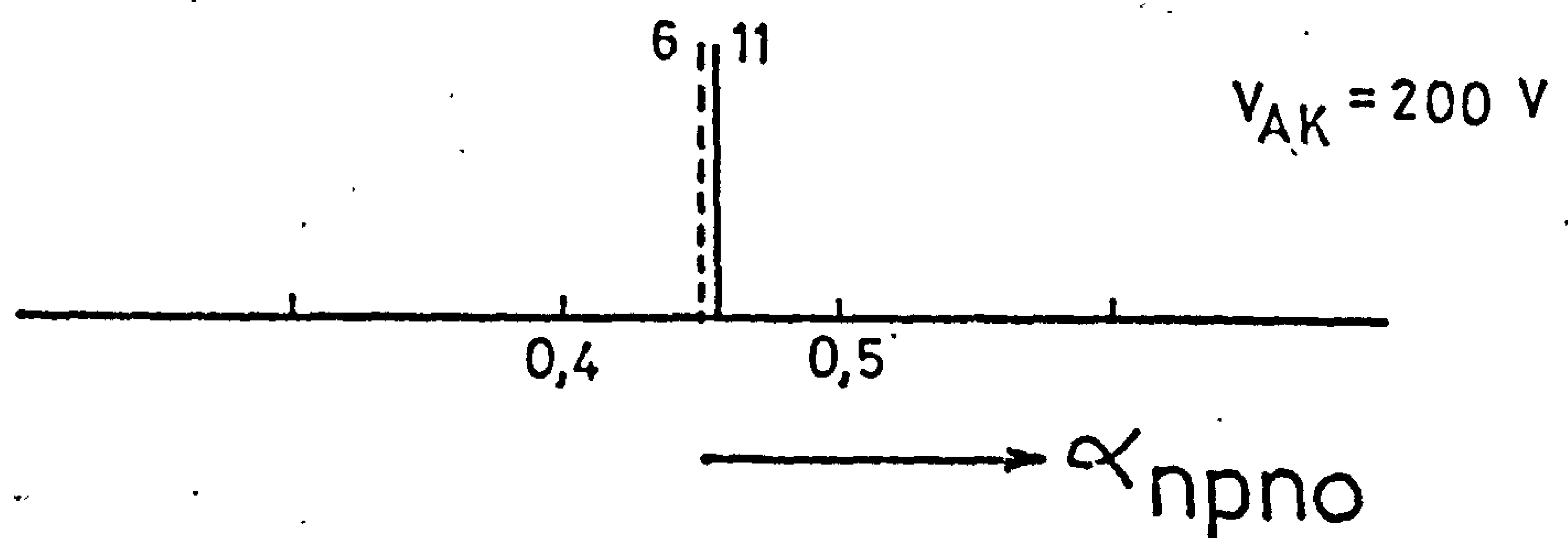
S.D. NO.S.D.

$V_{AK} = 150$ V

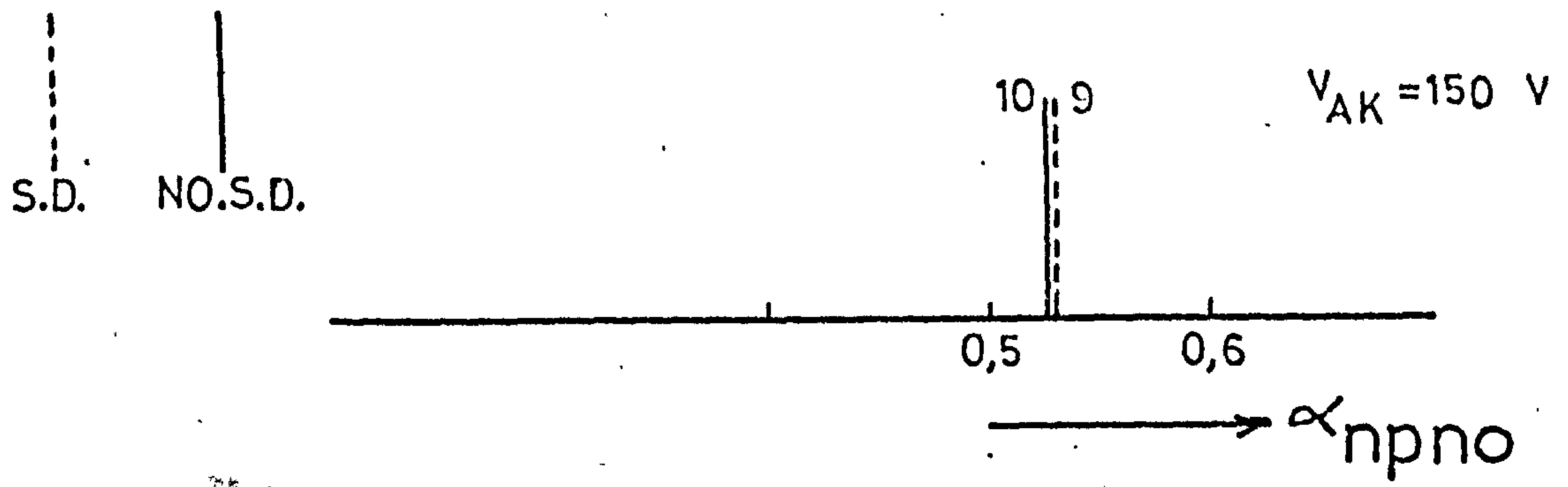


T = 100°C

$I_A = 10$ mA

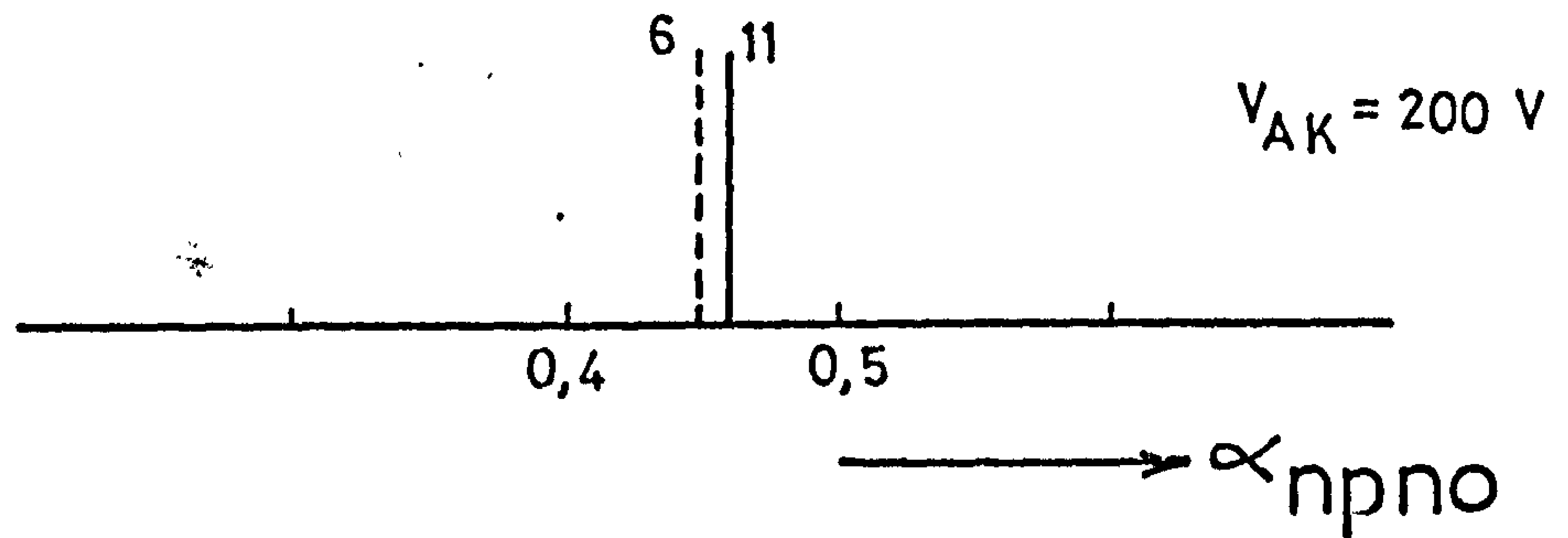


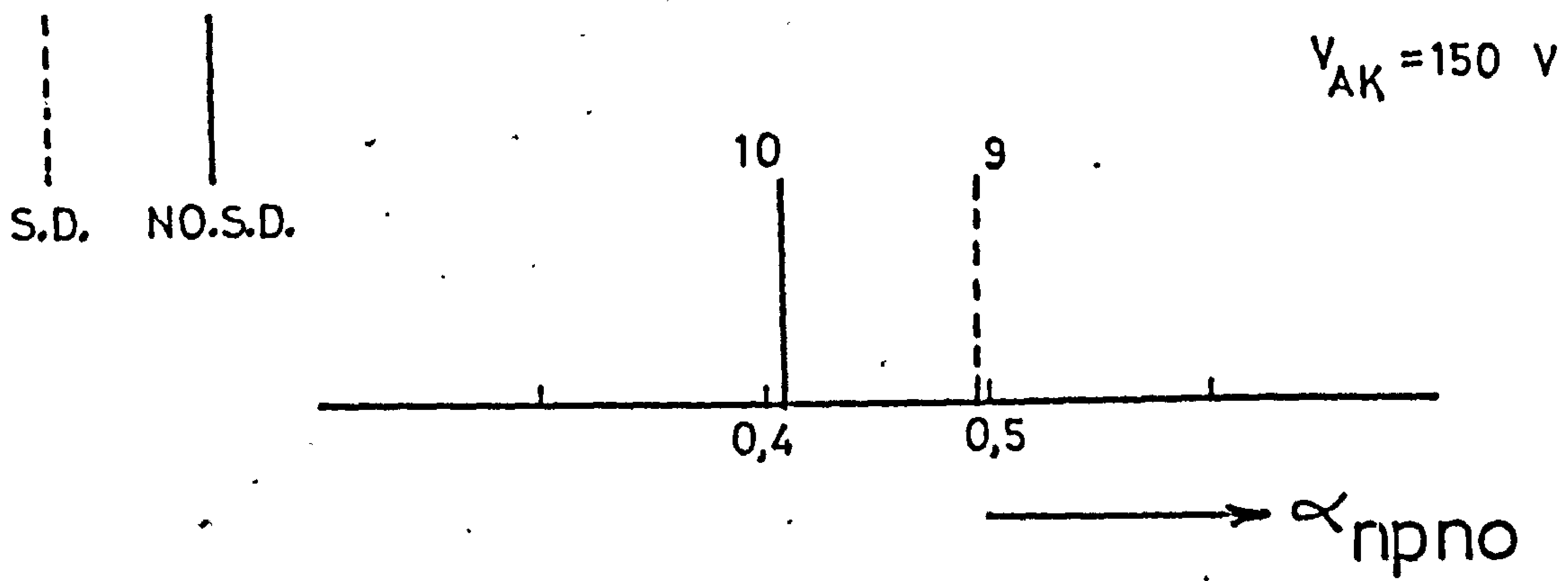
cont. of Figure (5-21).



T = 120°C

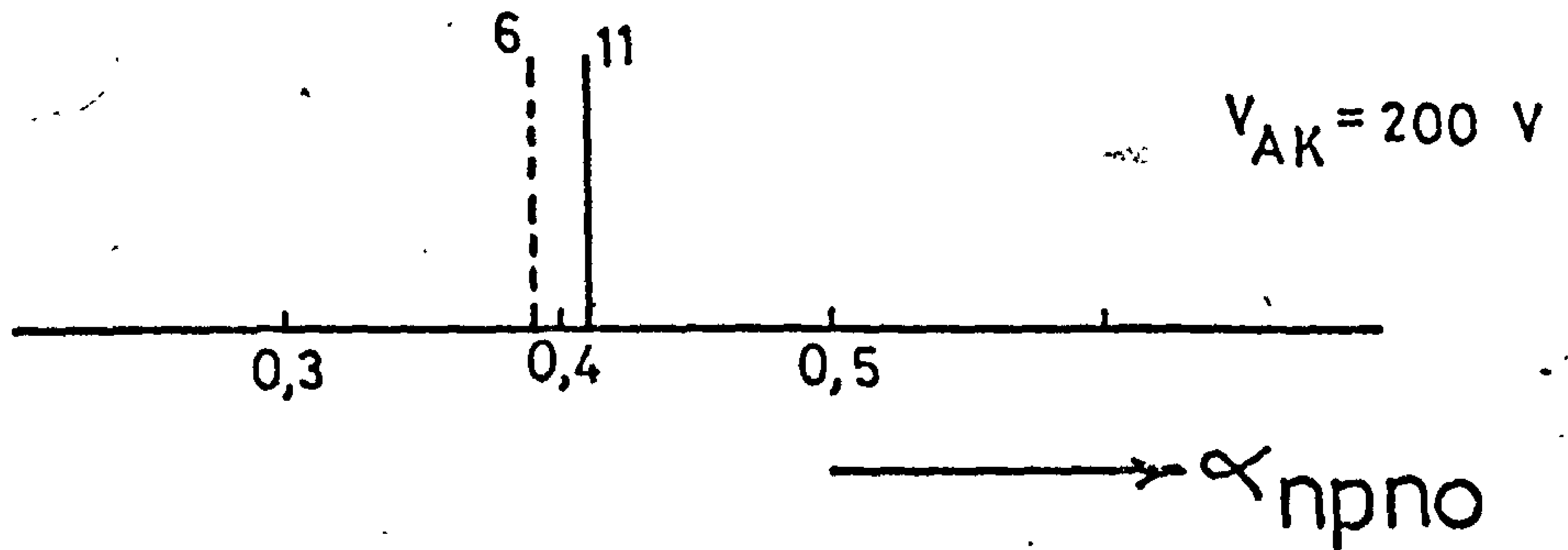
I_A = 10 mA





T = 140°C

I_A = 10 mA



cont. of Figure (5-21).

Figure (6-5) Plot of equation (106) for various A_S.

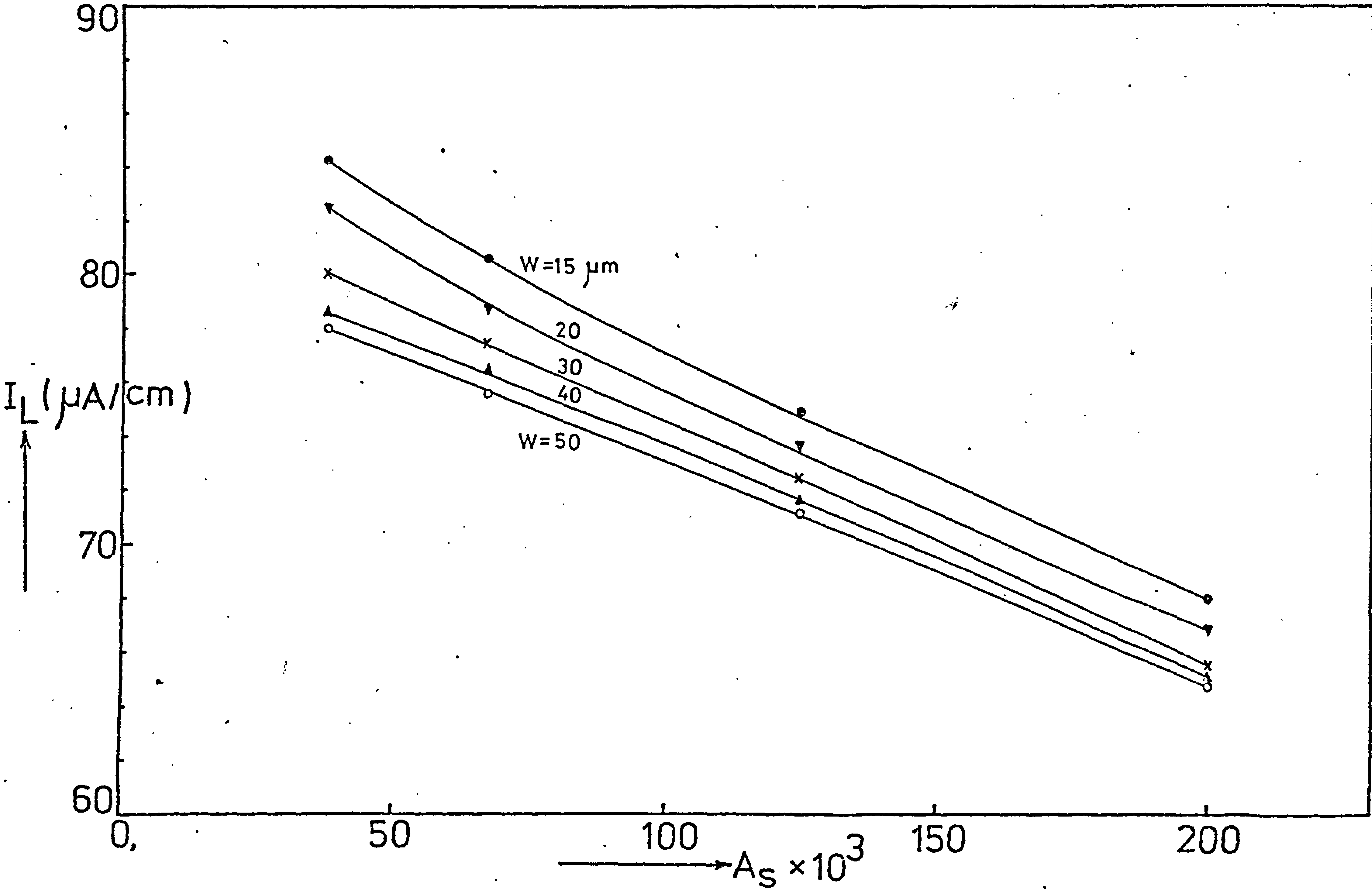


Figure (6-6) Variation of I_L at (1 - A_s) with A_s at constant W

Figure (6-7) Plot of non-linear equation of (106) for various W.

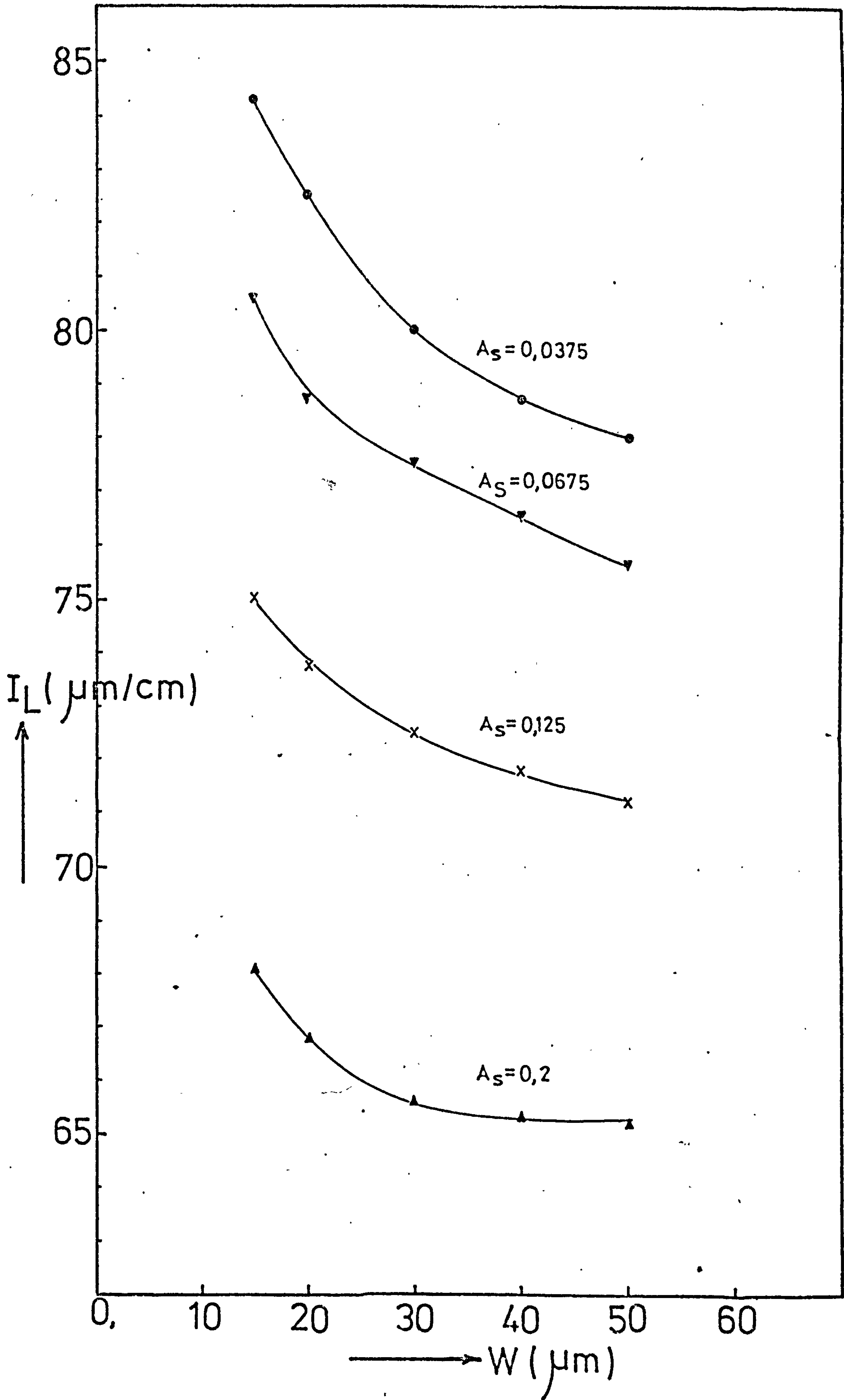
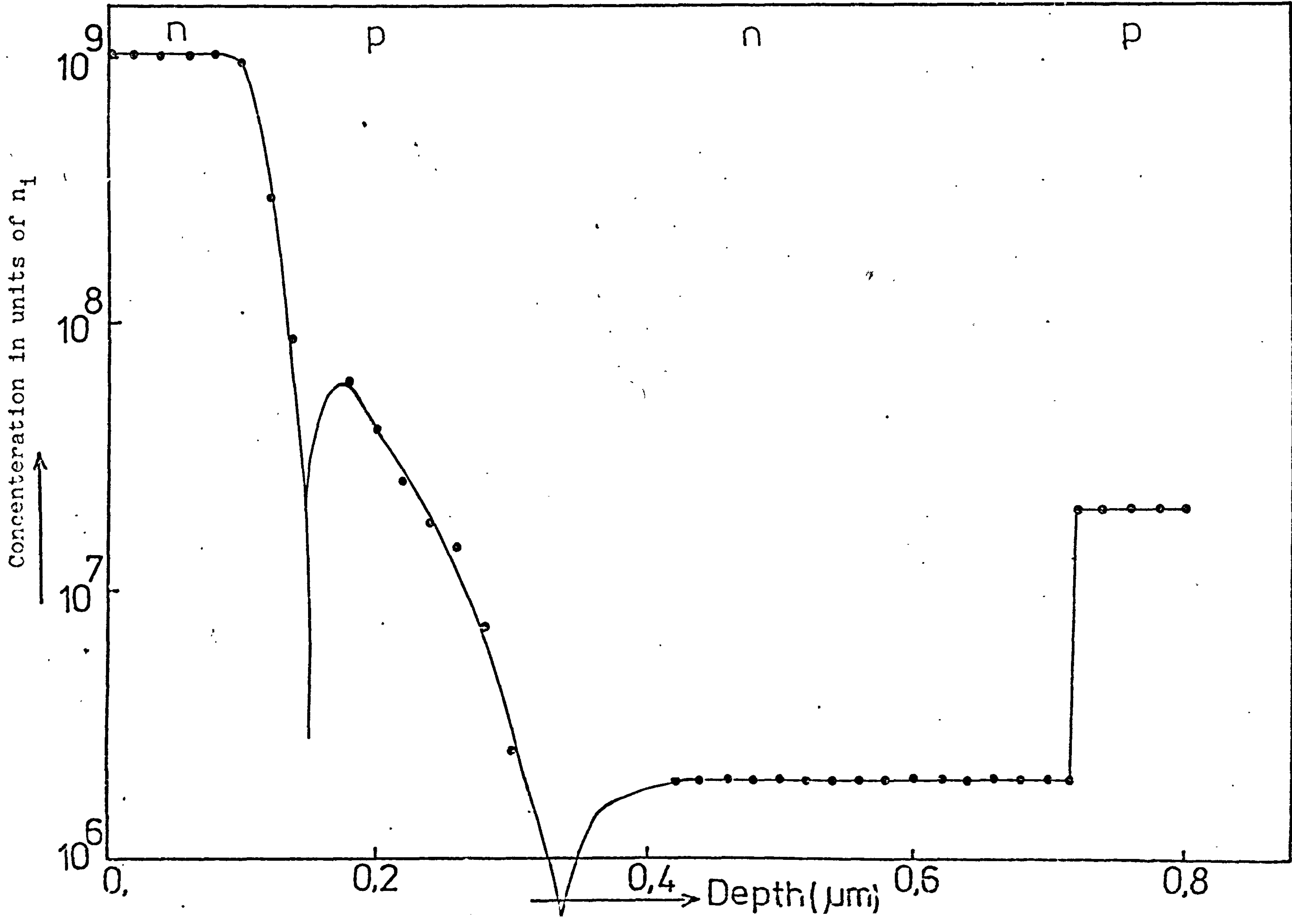


Figure (6-8) Variation of hole current I_L at $(1-A_S)$ with W at constant A_S.

Figure (7-9) Doping Profile.



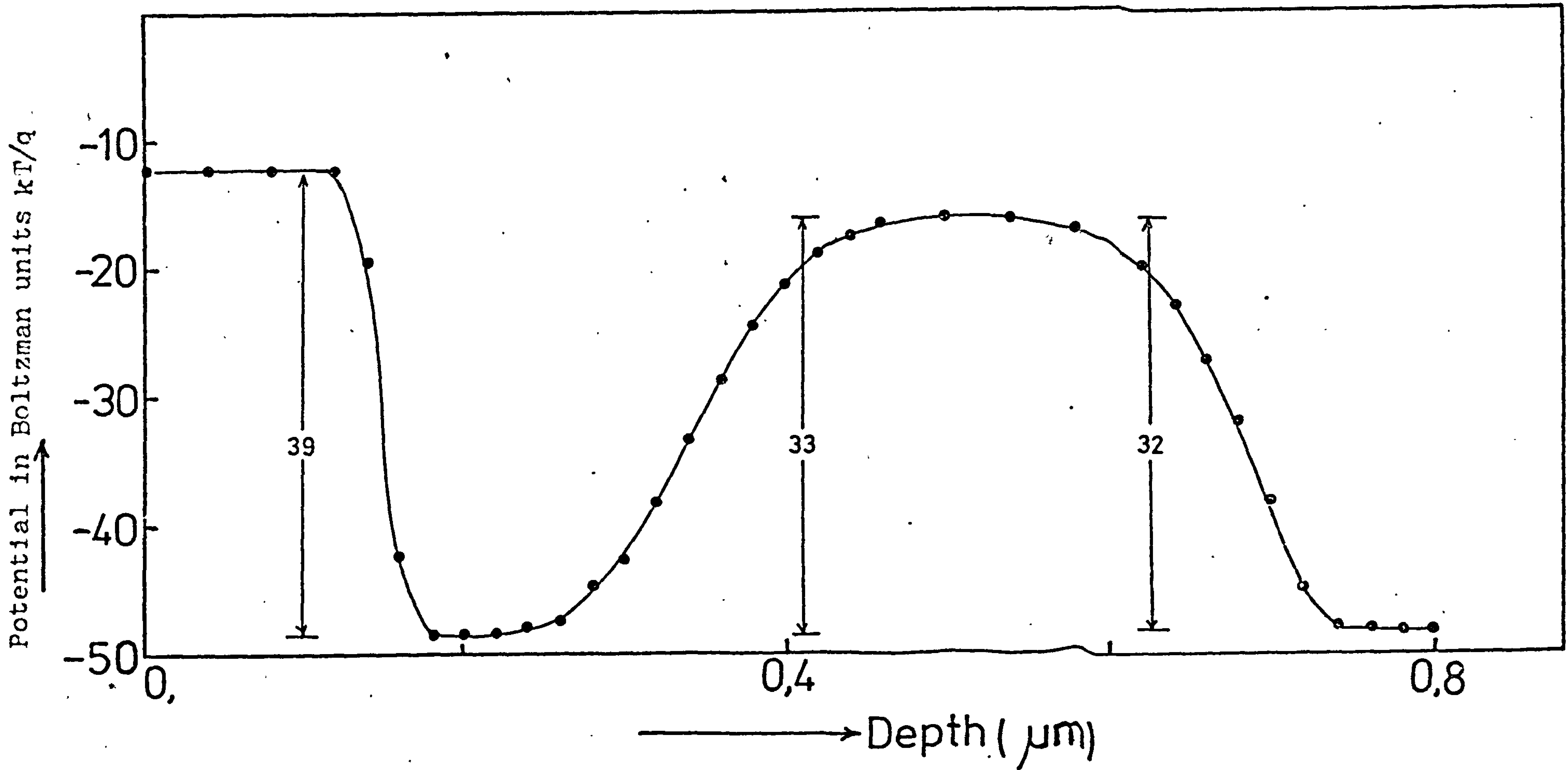


Figure (7-10) Plot of potential under zero bias condition.

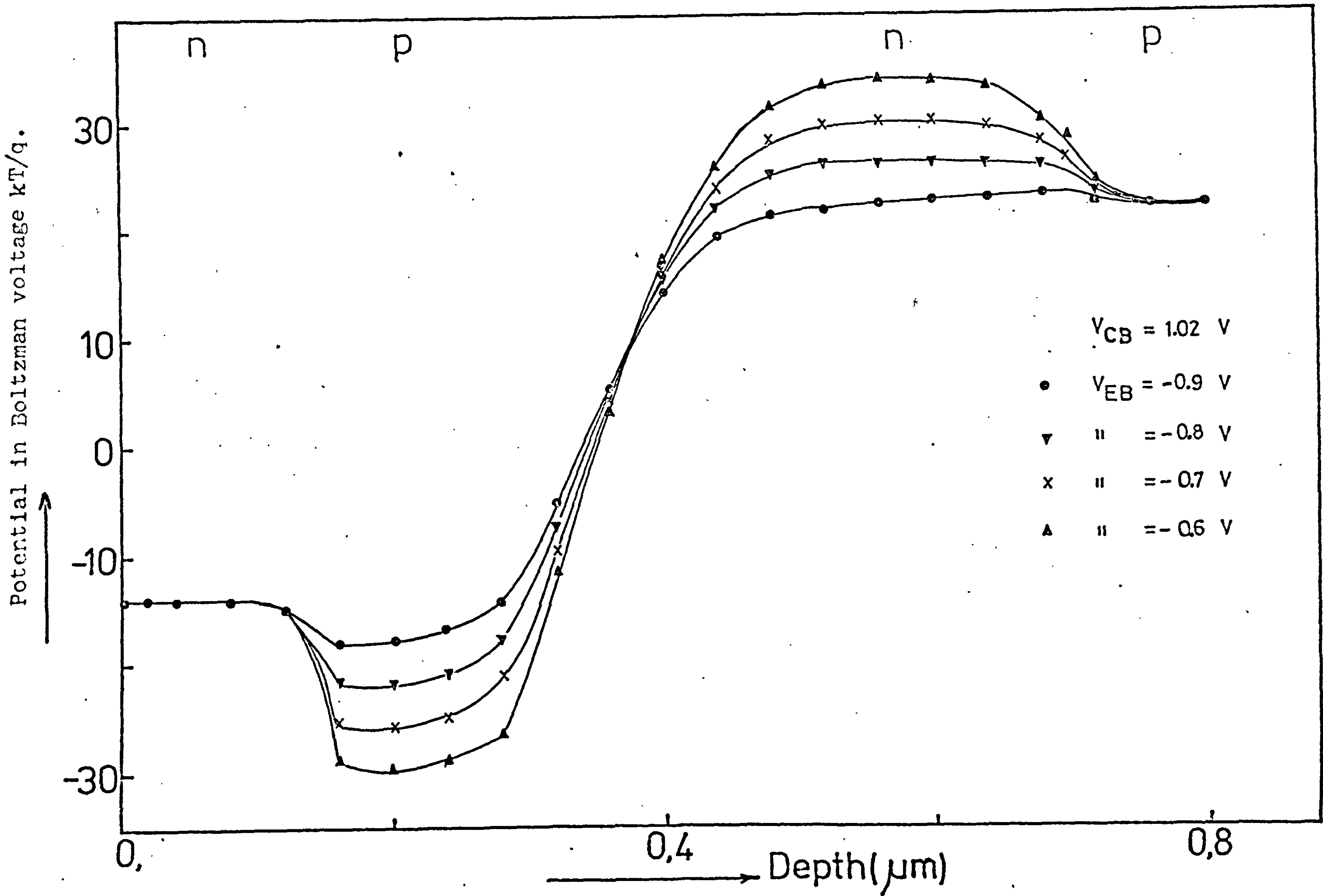


Figure (7-11) Electrostatic potential distribution in unit of Boltzman voltage kT/q.

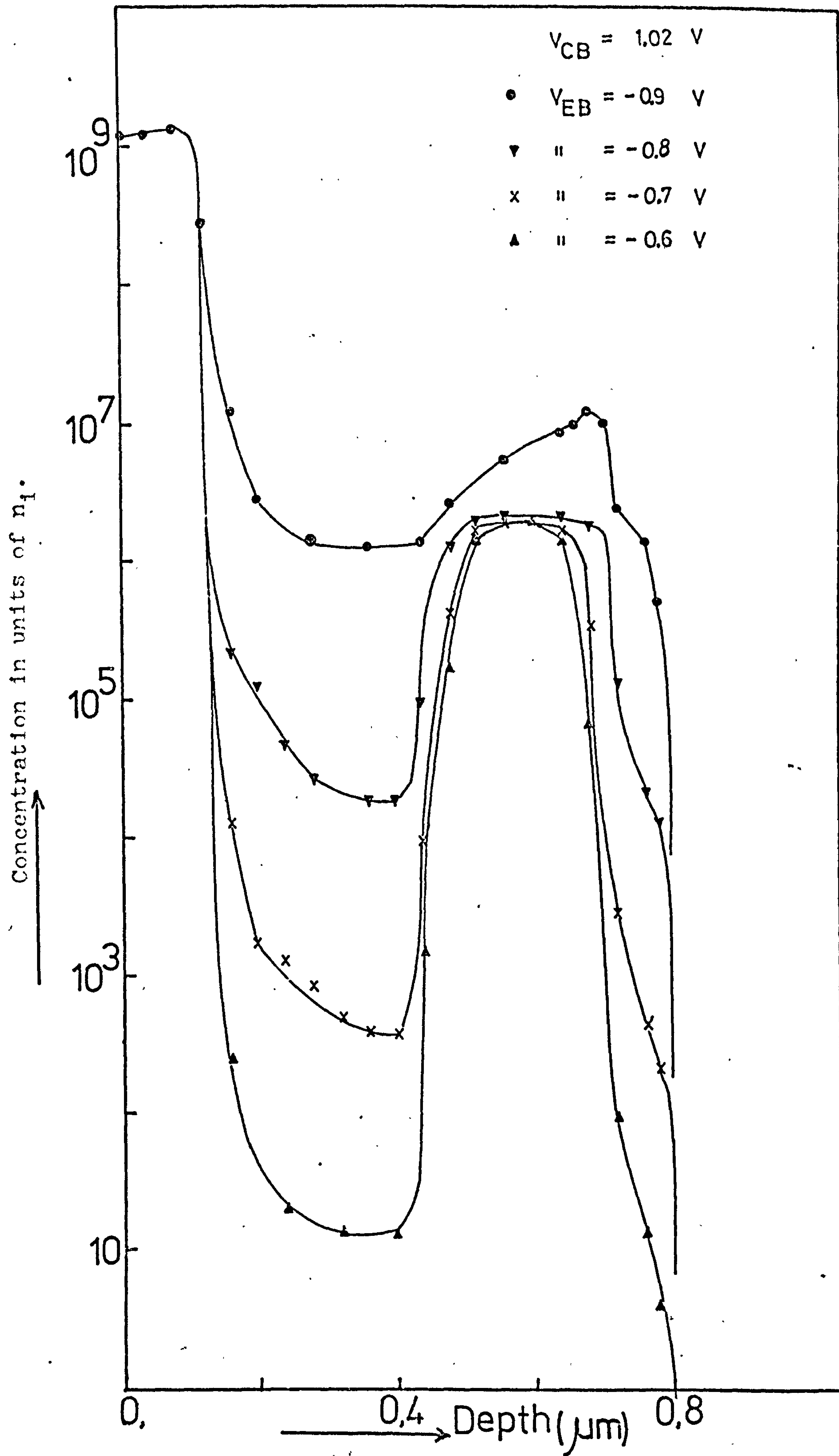


Figure (7-12) Normalized electron density distibution in units of n_i.

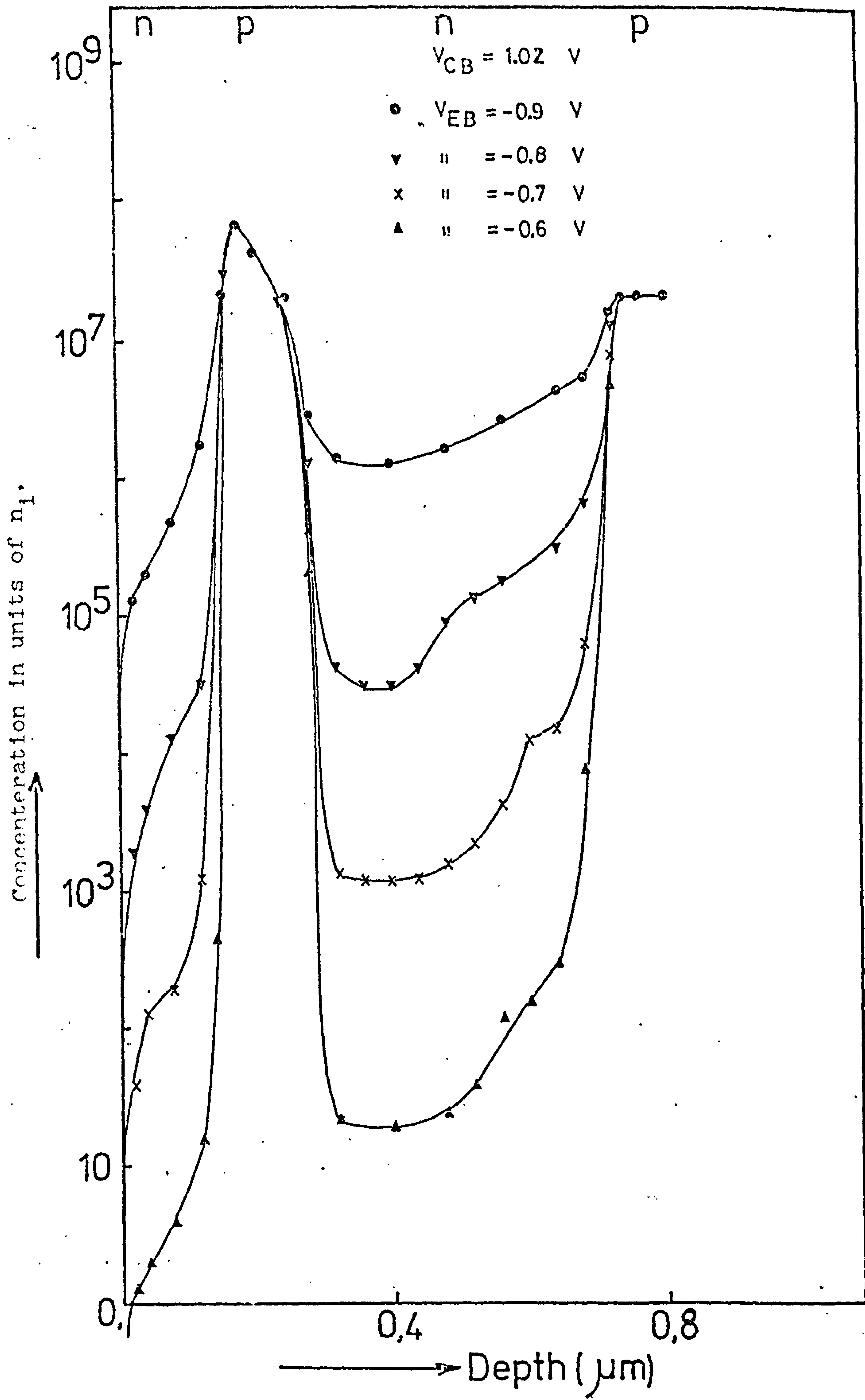


Figure (7-13) Normalised hole density distribution in units of n_i.