Development of CMOS Active Pixel Sensors

A thesis submitted for the degree of Doctor of Philosophy

by

Thomas Alexander Greig

Imaging for Space and Terrestrial Applications Group

e2v centre for electronic imaging

School of Engineering and Design

Brunel University

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Abstract

This thesis describes an investigation into the suitability of complementary metal oxide semiconductor (CMOS) active pixel sensor (APS) devices for scientific imaging applications. CMOS APS offer a number of advantages over the established charge-coupled device (CCD) technology, primarily in the areas of low power consumption, high-speed parallel readout and random (X-Y) addressing, increased system integration and improved radiation hardness. The investigation used a range of newly designed Test Structures in conjunction with a range of custom developed test equipment to characterise device performance. Initial experimental work highlighted the significant non-linearity in the charge conversion gain (responsivity) and found the read noise to be limited by the kTC component due to resetting of the pixel capacitance. The major experimental study investigated the contribution to dark signal due to hot-carrier injection effects from the in-pixel transistors during read-out and highlighted the importance of the contribution at low signal levels. The quantum efficiency (QE) and cross-talk were also investigated and found to be limited by the pixel fill factor and shallow depletion depth of the photodiode. The work has highlighted the need to design devices to explore the effects of individual components rather than stand-alone imaging devices and indicated further developments are required for APS technology to compete with the CCD for high-end scientific imaging applications. The main areas requiring development are in achieving backside illuminated, deep depletion devices with low dark signal and low noise sampling techniques.

Declaration

I hereby declare that no part of this thesis has been previously submitted to this or any other university as part of the requirement for a higher degree. The work described herein was conducted solely by the undersigned except for those items acknowledged in the text.

Thomas Greig

January 2008

Dedication

To everyone who believed I had it in me!

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Finally, I would like to gratefully acknowledge the financial support received from the Engineering and Physical Sciences Research Council and e2v technologies during my research studentship.

Contents

Acronyms

3T	Three transistor
ADC	Analogue to digital converter
APS	Active pixel sensor
CAD	Computer aided design
CCD	Charge-coupled device
CDS	Correlated double sampling
CIS	CMOS image sensor
CMOS	Complementary MOS
CTE	Charge transfer efficiency
DR	Dynamic range
DSNU	Dark signal non-uniformity
DSP	Digital signal processor
FET	Field effect transistor
FF	Fill factor
FPN	Fixed pattern noise
FWC	Full well capacity
IMO	Inverted mode operation
LOCOS	Local oxidation of silicon
MOS	Metal oxide semiconductor
MOSFET	MOS field effect transistor
MTF	Modulation transfer function
NIMO	Non-inverted mode operation
nMOS	n-channel MOS
PD	Photodiode
PG	Photogate
pMOS	p-channel MOS
PPD	Pinned photodiode
PPS	Passive pixel sensor
QE	Quantum efficiency
SF	Source follower
SPICE	Simulation program with integrated circuit emphasis
STI	Shallow trench isolation
VLSI	Very large scale integration

Chapter 1: Introduction

1.1. A history of Active Pixel Sensors

The field of semiconductor imaging devices has developed hugely since Gene Weckler first suggested operating p-n junctions in a 'photon flux integrating mode' in the late 1960's (Weckler, 1967). Weckler's idea was to collect photo-generated charge on the capacitance of a reverse biased p-n junction and utilise an active charge measurement circuit within each pixel that could be randomly accessed by a series of switches. Such a device formed the basis of what has now become known as an active pixel sensor (APS). The relatively complex architecture required fine feature sizes (< 1 μm) to incorporate the transistor circuitry into the pixel without sacrificing too much of the photosensitive area but such manufacturing techniques were unavailable at the time. The use of a different charge measurement circuit for each pixel also meant that fixed pattern noise (FPN) due to DC offset variations in transistors of the time would be severe.

Shortly after the APS was proposed, Boyle and Smith reported their idea for the charge-coupled device (CCD) in 1970 (Boyle and Smith, 1970). The charge-coupling technique had two key advantages over the APS technology at the time. The relatively simple structure of the CCD pixel enabled the production of small pixels (~20 μm in size) using the relatively coarse feature sizes of the existing metal oxide semiconductor (MOS) technology. The use of charge transfer to measure each photo generated charge packet with a single amplifier circuit at the output of the sensor array eliminated the fixed pattern noise problem of the APS technique. Some efforts did continue to develop the APS technology (then known as nMOS imagers) in the 1970's and 80's, but performance was consistently inferior to the best CCD. The CCD therefore was widely adopted and has since matured into an excellent performing technology, which has revolutionised digital imaging.

Although attempts at producing active pixels remained unsuccessful during the 1970's and 80's, integrated circuit (IC) technology continued to advance at a rapid rate as predicted by Gordon Moore's seminal paper (Moore, 1965). These advancements were dominated by the development of high density, low power and low cost complementary MOS (CMOS) manufacturing processes. The emergence of such processes began to

make APS a potentially viable option. Interest in the technology was therefore re-ignited in the early 1990's and it has developed rapidly over the last fifteen years. The developments were driven by the potential advantages that the APS approach, implemented in CMOS technology, offers relative to the CCD. The main benefits are:

- Lower power consumption
- Low cost due to wider availability of manufacturing process
- The possibility of random (X-Y) addressing
- Increased system integration such as on-chip analogue to digital conversion
- Improved radiation hardness due to minimal use of charge transfer
- Increased possibilities for high speed parallel readout

The recent realisation of devices encompassing the above qualities has enabled the APS to compete with the CCD for certain imaging applications. APS devices are now increasingly popular for use in consumer applications, such as mobile phones and digital still cameras, which require low cost, highly integrated imaging systems with low power consumption. The advantages of the APS approach also make the technology attractive for remote scientific applications where power, mass and space are limited and radiation environments can be harsh. Consequently there is a desire to replace the CCD with APS for applications in fields such as space science (Duvet and Martin, 2006). The most notable example is the plan to use APS within the extreme ultra-violet spectrometer (EUS) onboard the European Space Agency's Solar Orbiter mission, planned for launch in 2015 (Waltham et al., 2007). However such high performance imaging applications have stringent requirements of:

- Low dark signal
- Low read noise
- High sensitivity
- Robust technology

The CCD has been optimised to meet these demanding requirements through many years of research and development. The relatively mature technology can now provide excellent imaging performance. Future APS devices must match this standard of performance to compete with the CCD for scientific applications. At present, the use of existing CMOS very large scale integration (VLSI) processes to produce APS imagers

results in devices with poor performance. This is primarily because CMOS processes are generally optimised for high-speed logic circuits rather than photon detection. Therefore the use of such processes for APS manufacture tends to result in imagers that exhibit poor light sensitivity, high leakage current and degraded noise performance. Consequently the APS technology has not been widely employed in scientific imaging applications thus far. Efforts have been made to improve APS performance by optimising the manufacturing method to incorporate the types of custom processes employed within high-performance CCD imagers. However, such processes are still not readily available to the scientific community. Considerable work is therefore required to realise scientific grade image sensors able to compete with the more established CCD technology.

1.2. Research goals

This thesis describes a pilot project at Brunel University and e2v technologies, a world leading manufacturer of scientific CCD imaging sensors, to investigate the feasibility of producing CMOS active pixel sensors (APS) suitable for scientific imaging applications. The project aimed to formulate a series of design rules and processes, which could be utilised in future projects to produce high performance sensors for a given scientific application. The main objectives of the project were to:

- Produce a fully functioning imaging device
- Explore pixel design optimisation for a given scientific application
- Demonstrate scalability of pixel designs
- Develop a range of APS characterisation techniques
- Quantify foundry dependent parameters of dark signal and quantum efficiency
- Relate simulated layout-dependent parameters to measured values

The approach to achieving these objectives was to design and manufacture a range of small-scale test structures for direct pixel addressing with variation in pixel design and also a smaller number of larger format imaging devices with internal scanning circuitry. A detailed characterisation of the manufactured devices was then used to verify the design principles, and thereby give increased confidence in the design accuracy of future more advanced devices.

1.3. Thesis organisation

This thesis is organised into nine chapters, with Chapter 1 being this introduction.

Chapter 2 outlines the main features of CCD and APS image sensors. The fundamental difference between the two architectures is explained and the advantages and drawbacks of the two approaches are summarised.

Chapter 3 begins with a more detailed description of the theoretical operation of the photodiode and MOS transistor. This includes a description of how these components are combined to construct the most basic three transistor (3T) plus photodiode active pixel. A detailed explanation of pixel operation is given along with the advantages and drawbacks of the design. The chapter also includes a description of the various image sensor performance parameters including quantum efficiency, dark signal and noise sources. The chapter closes by outlining some developments that have been made in an attempt to improve the performance of the 3T pixel.

Chapter 4 begins with a description of CMOS manufacturing processes and explains how they are utilised to produce the 3T active pixel. The Tower Semiconductor TS50 CMOS process, selected by e2v technologies to manufacture the Test Structures, is also described. The second half of the chapter focuses on the electrical simulations performed during the design process and related design issues.

Chapter 5 gives a detailed description of the finalised Test Pixels and Imaging Arrays. The chapter also outlines the range of drive electronics and test equipment that were developed to enable characterisation of the different designs.

Chapter 6 describes the initial functional testing and characterisation of the new Test Structures using the mean-variance method and other techniques. The key measurement outlined in this chapter is the charge conversion gain (responsivity), which is necessary to enable the calculation of further parameters such as dark signal and quantum efficiency. The chapter closes with an assessment of the noise, dynamic range and node capacitance of the tested devices.

Chapter 7 outlines a detailed investigation into the dark signal behaviour of the Test Structures. The first section outlines an assessment of the dark signal characteristics of the Imaging Arrays, including an investigation into the variation with temperature. The different contributions to overall dark signal are then investigated in more detail using the smaller scale Test Pixels. This includes a major investigation into the hot-carrier injection effect.

Chapter 8 describes an investigation into the electro-optical characteristics of the devices. The first section outlines an experimental set-up developed to measure quantum efficiency. The results of the QE measurements are then described. The chapter closes by comparing these results with work performed at e2v technologies to assess pixel-pixel cross talk effects.

Chapter 9 summarises the key findings of this thesis and highlights some of the outstanding issues and the future work to be performed. The thesis closes with a discussion of the developments needed to further improve APS devices for scientific imaging applications.

1.4. Publications

The work contained within this thesis has been described in two publications. The details of these publications are listed below:

Greig, T., Castelli, C., Holland, A. & Burt D., The design of an active pixel sensor test structure optimised for the read out of scintillator screens, *Nuc. Inst. Meth.*, vol. **A573**, (2007), pp. 30-33.

Greig, T., Holland, A., Burt D. & Pike, A., CMOS pixel structures optimised for scientific imaging applications, *SPIE*, vol. **6660**, (2007).

Chapter 2: Introduction to active pixel sensors

This chapter describes two of the most popular solid-state image sensors that are in use today, the charge-coupled device (CCD) and the active pixel sensor (APS). The first section gives a brief history of their development. The fundamental difference between the CCD and APS architectures is then explained and the advantages and drawbacks of the two approaches are summarised. Finally the two technologies are compared with a third alternative, known as the hybrid image sensor, whereby a readout circuit is 'bump-bonded' to a detection layer.

2.1. Introduction

Solid-state image sensors have revolutionised the world of imaging during the last 40 years. Many existing imaging applications have been enhanced by their invention and many new ones, otherwise impossible with approaches such as conventional film or vidicon tubes, have also been developed. Two of the most significant devices are the now mature charge-coupled device and the more recently developed active pixel sensor, which is the focus of this thesis. The active pixel sensor offers some potential advantages over the CCD approach for scientific imaging and is the subject of significant funding from organisations such as ESA, NASA and CERN.

2.2. A brief history of solid-state imagers

This section outlines a brief history of the development of solid state imagers. A more detailed description is given by Fossum (1997). The first attempts at MOS transistor-based imaging devices were made in the early 1960's but the devices had an output proportional to the instantaneous incident light and as such had poor sensitivity. A major breakthrough was made in the late 1960's when Gene Weckler suggested operating p-n junctions in a 'photon-flux integrating mode' (Weckler, 1967). The basic principle was to collect photo-generated charge on the capacitance of a reverse biased p-n junction and measure the subsequent voltage change. The first type of solid-state image sensor to successfully incorporate this idea was a device that is now referred to as a passive pixel sensor (PPS). The PPS consisted of a 2-D array of pixels each containing a photodiode and a switch in the form of an n-channel MOS transistor to access the photodiode output. Therefore, at the time, the devices were referred to as nMOS imagers. The architecture was susceptible to noise sources introduced by the

large capacitance of the metal track connecting the pixel to the amplifier at the edge of the array, so it was suggested that if the charge measurement could be performed close to the pixel, these noise issues would be eliminated. It was therefore proposed to place an amplifier transistor within each pixel (Noble, 1968). Such a pixel with one or more active transistors within it is known as an "active pixel" and the complete device with many pixels an "active pixel sensor" or APS. However, the concept was difficult to implement in practice due to the relatively large photo-lithographic feature sizes available at the time. The problem was that the resulting pixel required to contain the electronics and an appreciable sized photodiode would be too large for many applications.

Soon after the APS was proposed, Boyle and Smith reported their famous idea for the charge-coupled device (Boyle and Smith, 1970). The CCD approach promised a number of advantages. The relatively simple pixel architecture could be manufactured using the existing coarse photo-lithographic technology and the pixel array was less susceptible to fixed pattern noise problems, as all the pixel signals were measured by a single output amplifier. The active pixel approach used a different amplifier for each pixel, which introduced a different DC offset from pixel to pixel. These fundamental differences led the CCD to dominate the field of solid-state imaging. The dominance of the CCD and the disadvantages of the APS approach using the existing VLSI technology meant there was minimum effort applied to improving the nMOS imagers during the 1970's and 1980's. Companies such as Matsushita and Hitachi continued to investigate the devices (Fossum, 1997), but performance was consistently inferior to equivalent CCDs.

Interest in Active Pixel Sensor research was not rekindled until the early 1990's, primarily by researchers at Edinburgh and Linkoping Universities in Europe, Technion University in Israel (Yadid-Pecht et al., 1991) and the Jet Propulsion Laboratory in the United States (Mendis et al., 1993). These groups were driven to develop low power, low cost, highly integrated image sensors using the more advanced VLSI CMOS processing. The APS was now possible since the photolithography was now fine enough to realise usefully small pixels (< 50 μm). The theory was that other functions could also be included on the chip, such as analogue signal processing and even analogue to digital conversion. The emergence of high-density, sub-micron, low power

and low cost manufacturing processes in the early 1990's enabled such a "camera-on-a-chip" to be created (Nixon et al., 1995) without the specialised foundries required by CCDs. Interest in the technology therefore grew and it has developed rapidly over the last fifteen years. The fact that image sensors could potentially be manufactured using the same foundries used for many other semiconductor devices also meant that sensor designers could take advantage of the large economies of scale reducing the cost of production. The use of CMOS processing has led to the devices now being referred to as CMOS active pixel sensors (CMOS APS) or simply CMOS image sensors (CIS).

Several varieties of active pixel have evolved from the original passive pixel design and a comprehensive review of the developments can be found in El Gamal (2005). The most commonly produced active pixel is the three transistor (3T) plus photodiode design which is the focus of this thesis. The first high performance examples were demonstrated by JPL (Nixon et al., 1995), Toshiba (Iida et al., 1997) and Edinburgh University (Hurwitz et al., 1997). Many other designs have also been developed to improve performance. A more detailed analysis of the 3T pixel structure and the other variants is given in Chapter 3.

2.3. Charge-coupled devices

The charge-coupled device, or CCD, was originally conceived in the late 1960's by researchers at Bell Labs in the United States (Boyle and Smith, 1970). It was originally intended as a new type of memory circuit, but it was soon realised that the sensitivity of silicon to light made the CCD ideal for imaging applications. Further information on the CCD can be found in Holst (1998) and Janesick (2001).

2.3.1. Architecture

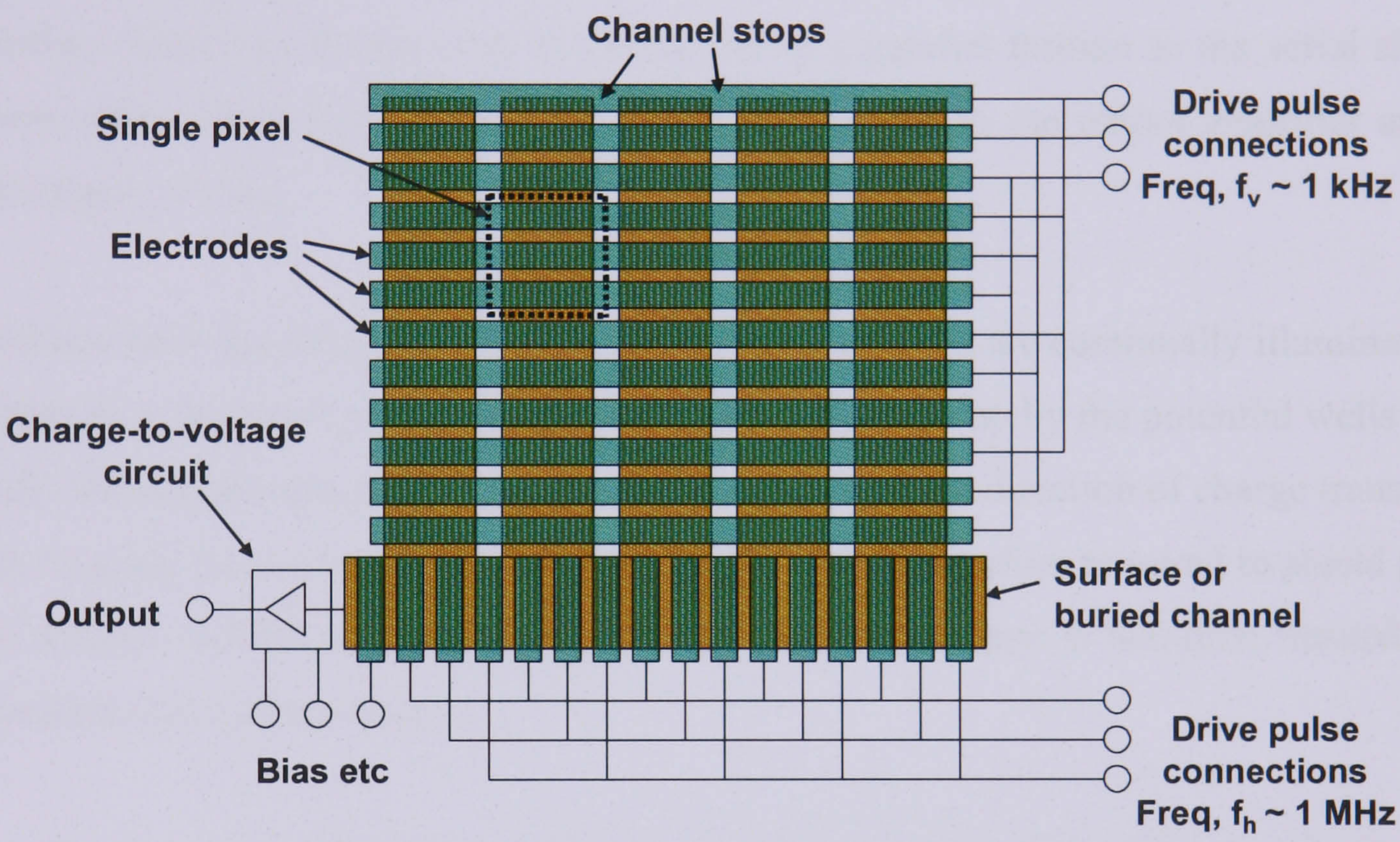


Figure 2.1 A schematic of the three-phase CCD pixel showing the repeating electrode structure combined with a serial readout register and single output amplifier stage

The charge-coupled device consists of an array of oxide-insulated electrodes or "gates" (essentially Metal Oxide Semiconductor (MOS) capacitors) below which charge signals can be stored and transferred in the underlying semiconductor under the control of externally applied drive pulses. **Figure 2.1** shows a schematic of the popular three-phase CCD pixel. The pixel consists of three electrodes bounded by the channel stops on either side. The pixel is effectively created by applying a positive potential to the central gate and a lower (or negative) potential to the two adjacent gates. This forms a "potential well" for collecting charge. Any electrons photo-generated under the three adjacent gates will diffuse to the middle gate where the potential well is deepest and be collected as a "packet" of charge. Electrons are confined in the horizontal direction by

channel stops. These are made of heavily doped p-type materials with an extra thickness of oxide over the top. This makes them relatively insensitive to voltages applied to the gate and the lower voltage creates an effective potential barrier.

The electrodes in the CCD can be arranged in one or two-dimensional arrays to collect and transfer charge through the silicon. Packets of charge stored under the gates of a CCD are moved from pixel to pixel by varying the voltages on neighbouring gates. The most basic arrangement is the full-frame CCD (Bosiers et al., 2003), consisting of a parallel CCD shift register, a serial CCD shift register and a signal sensing output amplifier. Each row in the array is shifted out in a parallel fashion to the serial shift register, which then shifts the row of image information to the output amplifier as a serial stream of data.

A problem with the design is that, during readout, the pixels are continually illuminated resulting in a 'smeared' image as spurious charge is picked up by the potential wells on transfer through the array. The image will be smeared in the direction of charge transfer in the imaging part of the array. A mechanical shutter is therefore required to shield the array during read-out to eliminate the effect. The architecture is therefore limited to applications such as astronomy.

In an effort to reduce the effects of smear, the frame-transfer (FT) CCD was developed (van de Steeg et al., 1985). The frame transfer CCD utilises an additional store section between the image section and register. After integration the entire frame of image data is quickly shifted vertically in a column-parallel fashion to the store section, which is covered by a metal light shield. The image data can then be read out from the store without being corrupted by illumination at the same time that charge from a new image is being collected in the image section. The frame transfer array is useful for TV and other such fast-framing scientific applications.

Another solution to reduce the effects of smear is the interline-transfer (ILT) CCD (Miyatake et al., 1980). The pixel contains a photosensitive diode and an adjacent storage and transfer area covered by a light shield. After integration, the charge generated in the photodiodes is quickly (~ 1μs) transferred to the vertical CCD registers, thereby minimising the effects of smear. There is of course only a single transfer in each

case, rather than the whole column of transfers in the case of a frame-transfer device, hence the fast transfer time. However, the light sensitive area (fill factor) of an ILT CCD pixel can be as low as 20% due to the presence of the storage and transfer area. There can also be some residual smear due to light leaking under the shield. The ILT smear levels are generally much lower than the FT levels and the ILT architecture has come to dominate the consumer TV markets, e.g. in camcorders. The opaque areas are actually used to advantage for one-chip colour cameras as they provide a region for the filter to change from one colour to the next.

2.3.2. Operation

The charge transfer process (also known as clocking or charge-coupling) is illustrated in **Figure 2.2**. As the gates are clocked, charge is transferred from gate to gate along the parallel register (parallel to the channel stops and each other) to the serial register at the bottom of the columns. A row of charge packets is then transferred laterally along the serial register to the CCD output node. The node is essentially a small capacitor C_{node} (actually a reverse biased diode which has capacitance) connected to the gate of an output MOS field effect transistor (MOSFET) amplifier. Before each packet is transferred, the node is reset to a known voltage, which is sampled by the output circuit. Charge from a pixel is then transferred onto the node causing a voltage change proportional to the signal charge transferred (i.e. where $\Delta V=\Delta Q/C_{node}$). The new voltage is sampled and subtracted from the initial reset level to determine the signal output from the pixel (White et al., 1973). This process, known as correlated double sampling (CDS), cancels a major noise source known as kTC noise and is explained in more detail in Chapter 3. The operation is continued for all outputs from a row and then all rows to achieve complete read-out from the whole image section.

The MOSFET amplifier is the only active element in a CCD and the fundamental advantage of the CCD approach is that all the charge packets are read out through the same amplifier. This means that certain offsets and noise sources introduced by the output circuit are the same for all pixels and can easily be removed with simple analogue circuitry to provide a stable image reference.

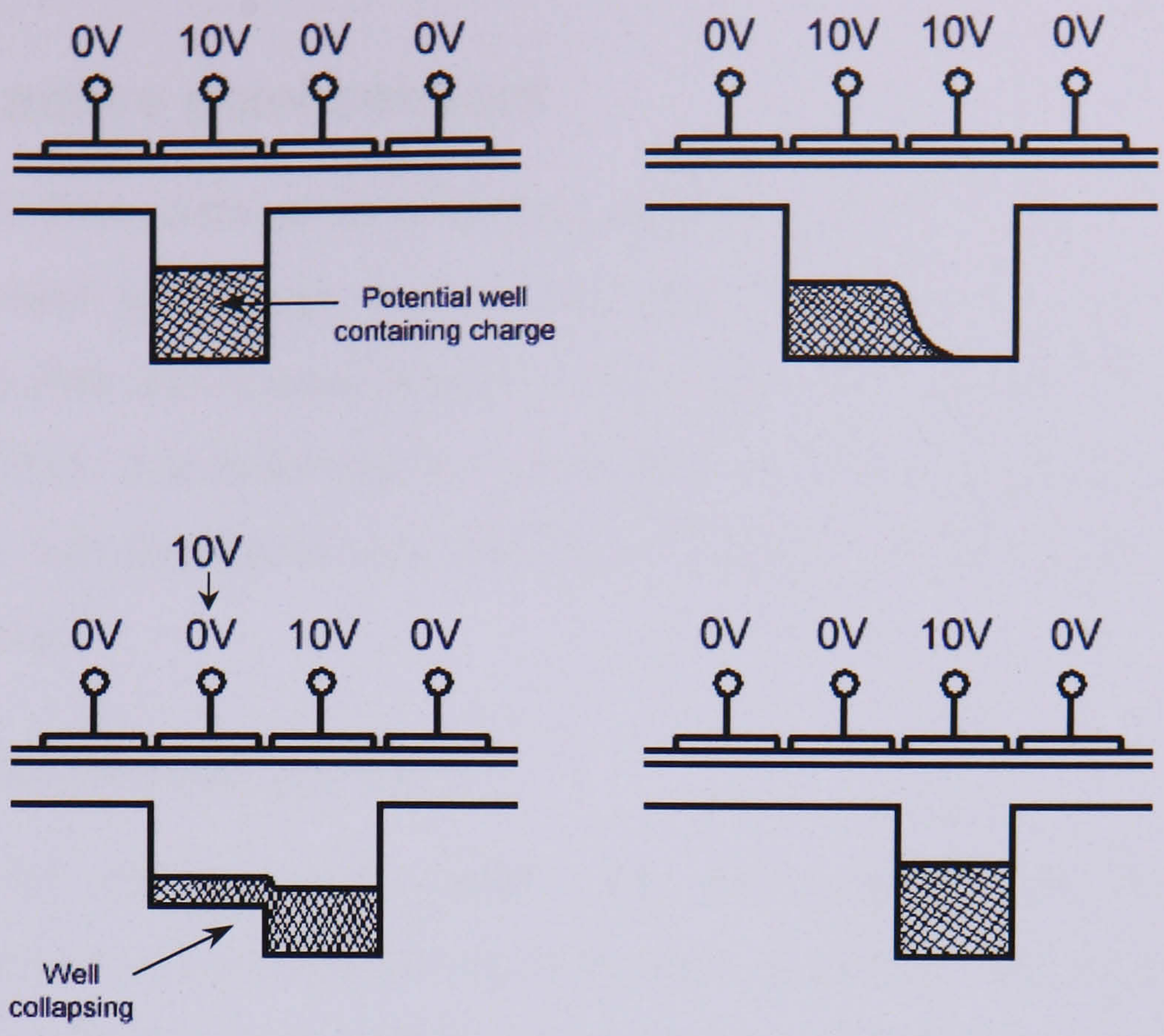


Figure 2.2 The CCD charge transfer process. A charge packet is transported through the array by alternating the voltages on subsequent gates to adjust the potential well beneath the gates

A major concept in the CCD is the efficiency of the charge transfer process. During the charge-coupling process a packet of charge may require thousands of transfers before reaching the output node. If a significant percentage of the packet is lost during every transfer, very little information will remain when the packet reaches the output. A charge packet generated in the centre of a 1024^2 pixel device will undergo 1024 transfers (512 transfers along the parallel register, 512 along the serial register) to reach the output node. If 1 % of the charge is lost for each transfer, by trapping for example, then the percentage reaching the node will be:

$$(0.99^{1024}) \times 100\ \% = 0.0034\ \%, \qquad (2.1)$$

The percentage of the charge correctly transferred per pixel, known as the charge transfer efficiency (CTE), must therefore be very close to 100 % for the CCD approach to be effective. Therefore, for a charge packet to retain 99 % of the information when reaching the output node, a CTE of 99.999 % would be required. This has been achieved through many years of CCD development and has resulted in the approach being very successful for producing imaging devices. However the CTE can be severely degraded in some applications by radiation damage to the bulk silicon (Hardy et al., 1998).

2.4. CMOS active pixel sensors

Although the CCD has dominated solid-state imaging since it invention in 1970, CMOS active pixel sensor technology is now emerging as a strong competitor for some applications. Before active pixel sensors existed there were devices known as passive pixel sensors (PPS). The following sections outline the original concept of the PPS and explain how it has developed into the fully integrated CMOS active pixel sensor 'camera-on-a-chip'.

2.4.1. The passive pixel device

The idea of the passive pixel sensor was first proposed in the late 1960's (Weckler, 1967) and it has changed very little since that time. The basic passive pixel consists of a photodiode and an MOS enable transistor, which is accessed by a column and row scan circuit common to the array. The arrangement is shown in **Figure 2.3**.

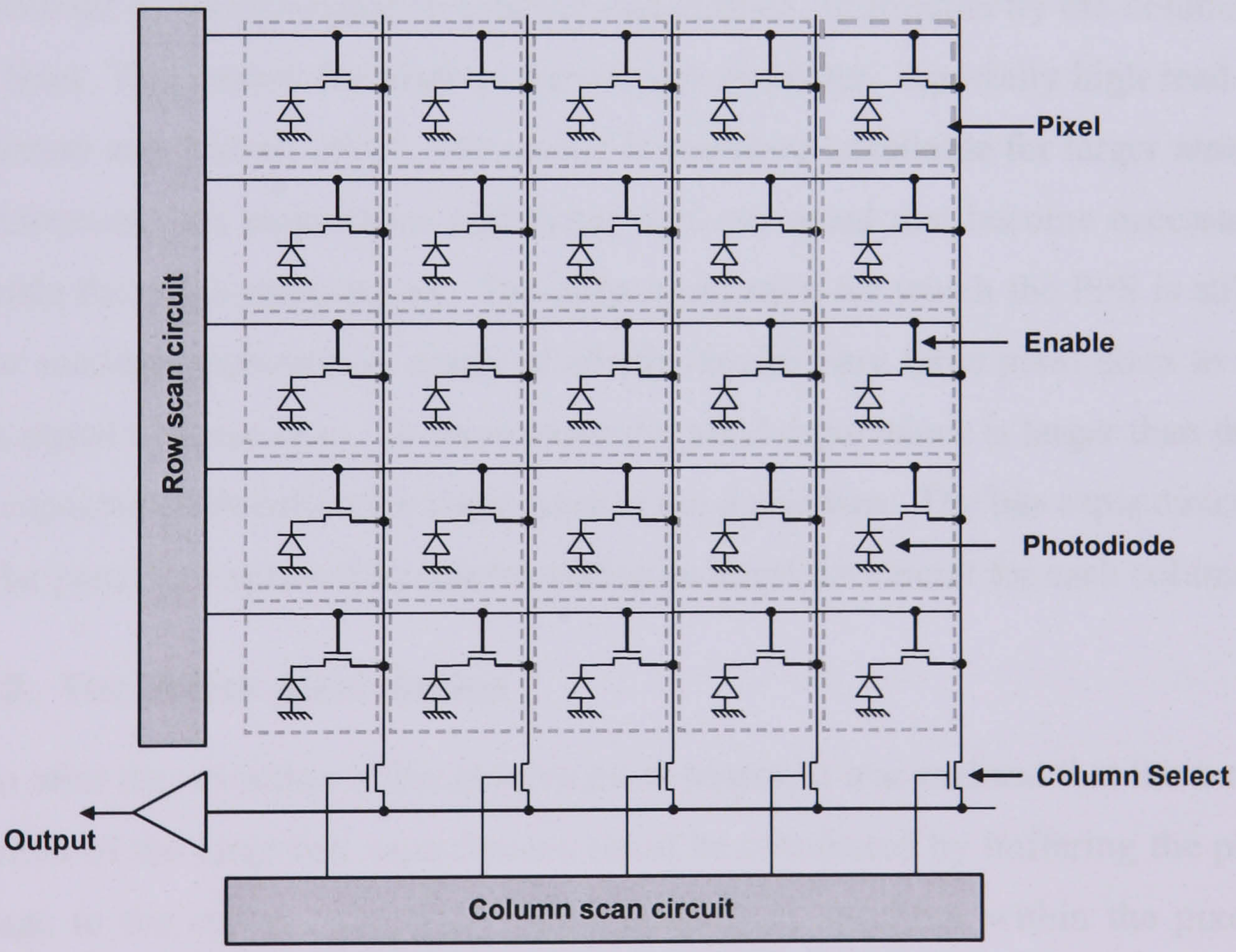


Figure 2.3 A schematic of the passive pixel sensor. The device consists of a photodiode and enable transistor within each pixel. The array is addressed with the use of horizontal and vertical scanning registers and the signal is buffered off-chip by a single amplifier

Before image acquisition, the row scan circuit operates to select a particular row and each pixel in the row is connected to the adjacent column bus. The column bus is then biased to the reference voltage level and all the photodiodes within each pixel are reverse biased to the reference level. The row is then de-selected and photo-generated signal charge is collected by the photodiode. At the end of the integration period the row is selected by enabling the row transistor and the photodiode output level is sampled onto the column bus. Each pixel in the row is then read out by connecting each pixel sequentially to an output amplifier circuit using the column scan circuit. The main advantage of the passive pixel approach for imaging is the minimal amount of electronics required within the pixel. This leaves most of the area available for the photodiode (e.g. > 80%, known as a high fill factor) and results in a high sensitivity to incident light signals.

The main disadvantage of the passive pixel array is that the capacitance of the in pixel-photodiode is small compared with the capacitance contributed by the column and row bus lines. This causes the pixel to have major problems, especially high read-out noise (Fujimori and Sodini, 2002). The sensor is therefore unsuitable for larger array sizes as the increased bus capacitance and faster read-out speed that become necessary further degrade the noise performance. The only application for which the PPS is still suitable is for medical applications, many of which require very large pixel sizes to achieve a high signal to noise ratio. In these cases the pixel capacitance is larger than the column bus capacitance therefore the noise issue is not a problem. The bus capacitance problem can be partially improved by implementing an amplifier circuit for each column.

2.4.2. The active pixel device

Soon after the invention of the passive pixel sensor, it was realised that the fundamental problem of the large bus capacitances could be eliminated by buffering the photodiode voltage to the column output by implementing an amplifier within the pixel (Noble, 1968). The architecture of a basic active pixel sensor is shown in **Figure 2.4**. It is a development of the passive pixel device with the addition of two further transistors within each pixel. The first extra transistor is used as an amplifier (shown by the amplifier symbol) and the second is required to reset the photodiode to the reference level. The reset transistor is not shown in **Figure 2.4** for simplicity. The architecture is

the most well-known active pixel structure and further detail on its design (and other variants) and operation is given in Chapter 3 and 4.

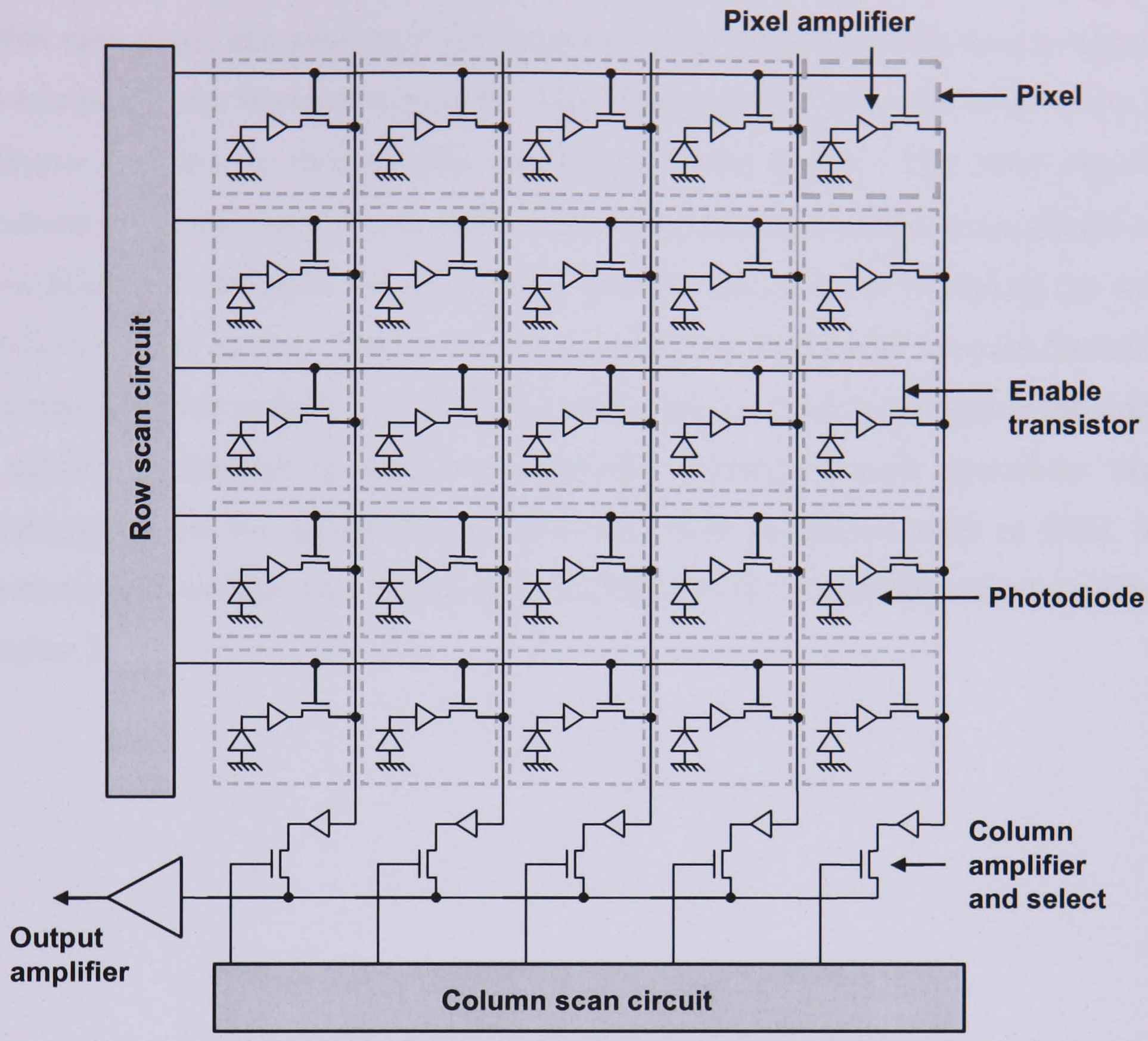


Figure 2.4 A schematic of the basic Active Pixel Sensor. Signal is collected by the diode and the output voltage is buffered off chip by the in-pixel amplifier when the pixel is selected

The use of an MOS transistor amplifier circuit for charge to voltage conversion within the pixel has a number of benefits, but also drawbacks. The main advantage is there is no need to transfer the photo-generated charge packet to the edge of the array for charge to voltage conversion. This facilitates random access of pixels and increases the possibility for high-speed readout. Also the lack of charge transfer through the bulk silicon is advantageous for scientific applications in a high radiation environment (Hopkinson et al., 2003) such as space science or particle physics. As stated earlier, radiation damage in silicon can cause major problems with charge transfer efficiency (CTE) (Hardy et al., 1998), therefore if charge transfer is minimised, the sensor will be less susceptible to CTE problems caused by the radiation damage.

The fundamental disadvantage of the APS concept compared to the CCD is the increased fixed pattern noise (FPN). This occurs because an APS uses an amplifier within each pixel, and pixel-to-pixel variations in the amplifier offset tend to occur due to variations in the fabrication process. This offset variation has to be removed by extra analogue circuitry or through post processing of the image. The other significant disadvantage is that the active circuitry within the pixel reduces the area available to the photodiode and decreases the fill factor. This has the effect of degrading the overall sensitivity of the device. Ideally the device would be illuminated from the backside as is commonly done with CCDs. A further disadvantage of the basic APS is the inability to perform operations in the charge domain. Charge domain operations can be advantageous for the application of noise reduction techniques such as CDS. More advanced APS designs have begun to be incorporate charge transfer and are outlined in Chapter 3.

2.4.3. 'Camera on a chip'

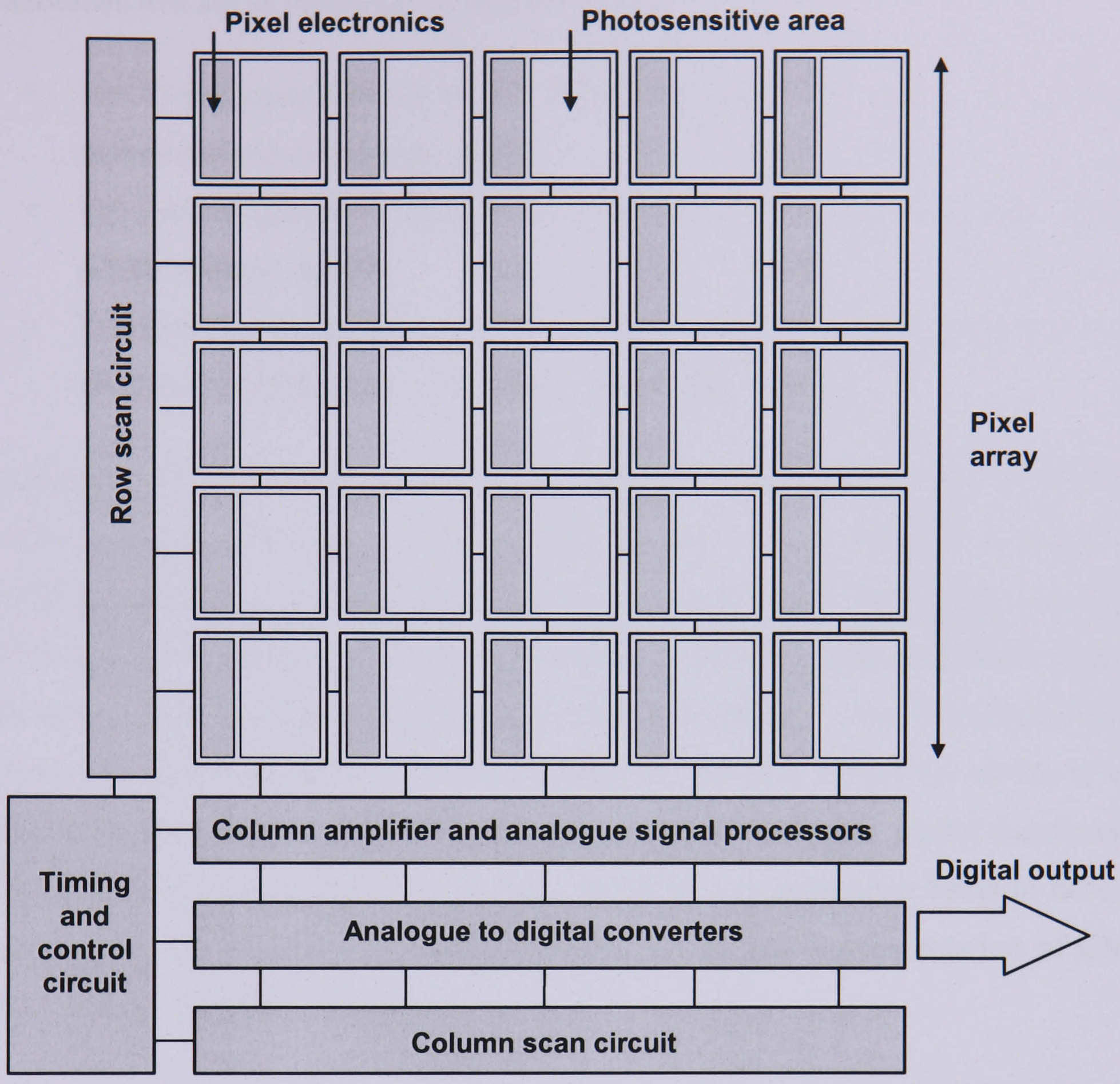


Figure 2.5 A block diagram illustrating the integrated approach to CMOS imaging. The major advantages over the CCD are the high speed parallel readout, low power dissipation and high level of on-chip integration

The majority of active pixel sensors can be produced with CMOS manufacturing processes that are also used for a wide range of integrated circuits. The use of advanced CMOS processing provides a number of additional benefits to the APS approach. The main advantage is the ability to integrate other analogue or digital processing functions onto the sensor, thus creating a complete integrated imaging system or 'camera-on-a-chip' (Fossum, 1997). A block diagram illustrating the integrated approach to CMOS imaging is shown in **Figure 2.5**. The use of CMOS manufacturing not only enables the production of the array of active pixels and scanning circuitry, but also timing and control electronics, further analogue signal processing and even analogue to digital

conversion. The development of CMOS imagers can now be divided into three generations that are as follows (Theuwissen, 2007):

- The first generation contained the pixel array along with some analogue electronics and an analogue output
- The second generation included an integrated analogue to digital converter giving a digital output
- The latest third generation includes a full system on a chip approach whereby the camera is simply powered up and image data results

At present, the use of existing advanced CMOS VLSI processes to produce imagers sensors still results in devices with poor performance. This is primarily because the CMOS processes are generally optimised for high-speed logic circuits and their use for APS manufacture tends to result in imagers that exhibit poor light sensitivity (quantum efficiency), high dark signal and degraded noise performance. The second generation is the most popular architecture. This is because the imaging part of the device is more suited to a more conservative older technology but the complex digital functions are best suited to the latest CMOS technology, therefore it is quite often better to have two separate devices. Further consideration on the design and implementation of CMOS image sensors is given in Chapter 4.

2.4.4. Digital pixel sensors

The most extreme case of on-chip integration is the digital pixel sensor (DPS) whereby the digital signal processing is incorporated into each pixel. The approach was first proposed in the late 1990's by researchers at Stanford (El Gamal et al., 1999) and the principle is illustrated in **Figure 2.6**. However, the group did not implement the concept until 2001 (Kleinfelder et al., 2001). The DPS approach enables many new readout techniques to be employed and the speed of operation can be extremely fast (> 10,000 frames/s) due to the parallel nature of the signal processing. The main disadvantage is that many transistors have to be employed which drastically reduces the photosensitive area (fill factor) of the pixel.

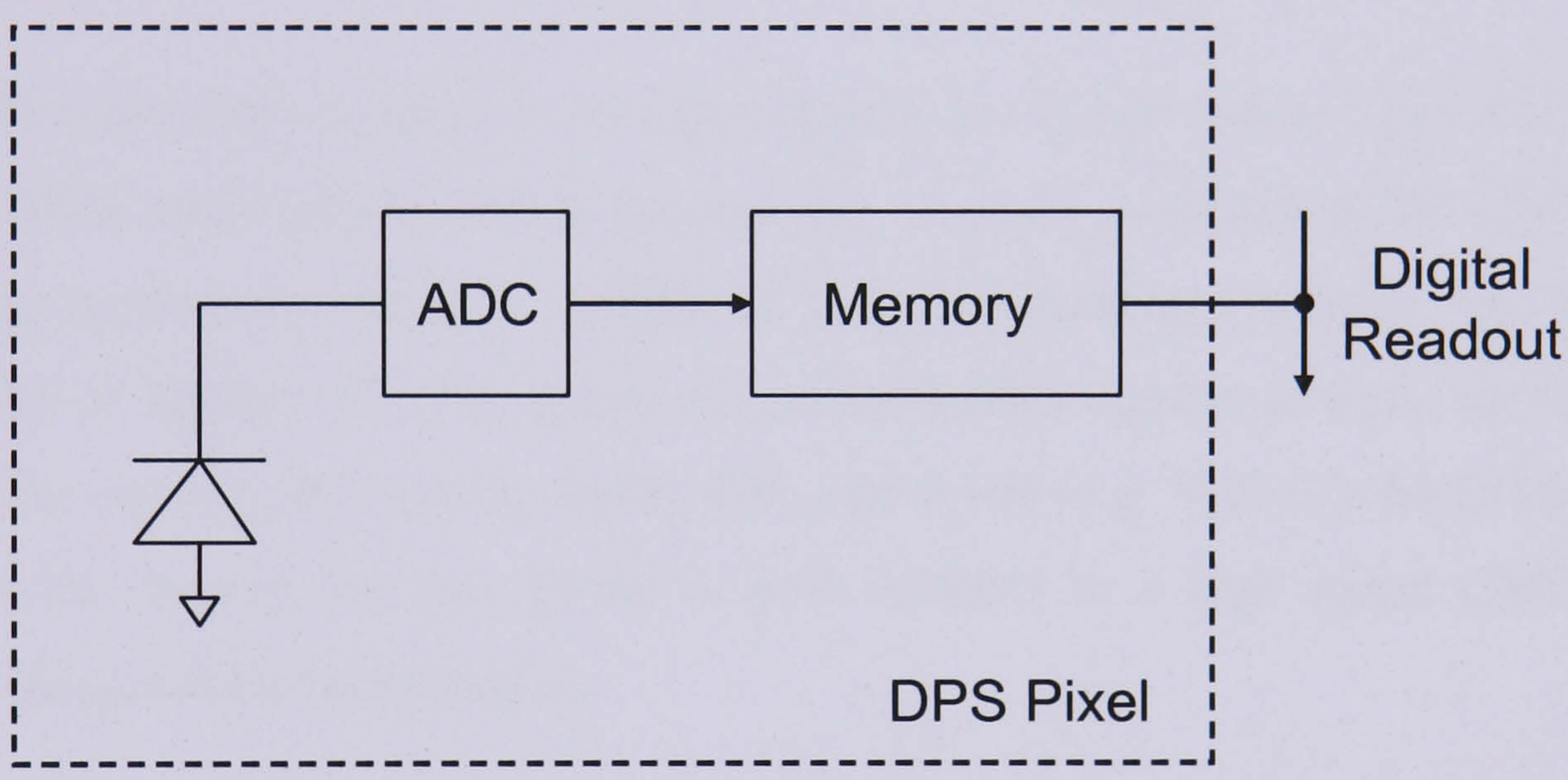


Figure 2.6 The Digital Pixel Sensor. Each Pixel contains a photodiode, an analogue to digital converter and a logic memory circuit. The high number of components results in large pixel sizes and/or a low fill factor

2.5. Hybrid and 3-d SOI imaging devices

The problem with using a CMOS process to produce an image sensor is that, in general, it is not optimised for detecting photons, rather for faster more efficient digital logic. The CCD process on the other hand has been carefully optimised over the past 30 years for imaging applications, but not for high performance digital logic circuitry. A solution to this problem is to create two separate devices, one of which is optimised for imaging performance and the other for read-out and analogue and/or digital signal processing. The subsequent combination of the two devices into one is then known as a hybrid sensor.

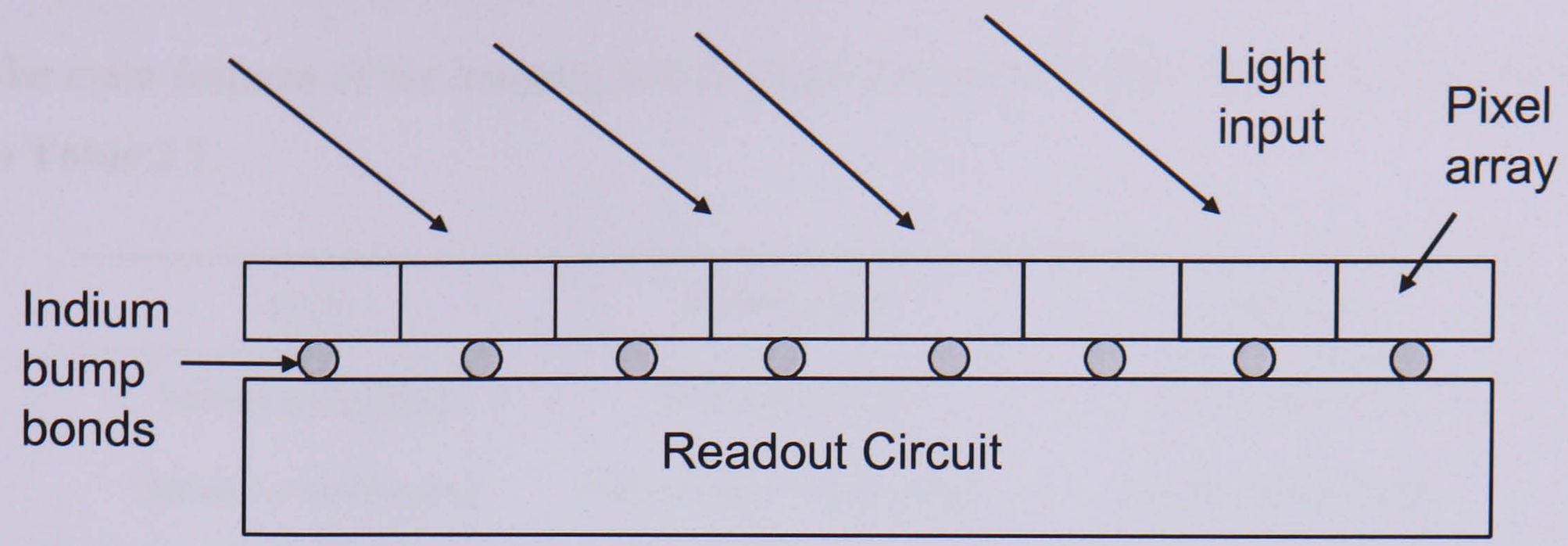


Figure 2.7 The Hybrid pixel sensor. The highest performance imaging system may only be achievable with the hybrid approach. An optimised imaging structure is interfaced to a high performance readout circuit using indium bump bonds to make connections between the two layers

There are three main techniques to implementing the hybrid sensor: the CMOS-CMOS, CCD-CMOS and Hybrid-CMOS approaches. A good example of the CMOS-CMOS approach is given by Bai et al. (2005) of Teledyne Imaging Systems. The principle is illustrated in **Figure 2.7**. The group use an optimised custom process for the imaging part of the array, which can be wavelength optimised (e.g. HgCdTe for Infrared (IR) or CdZnTe for X-ray), but the device is then coupled to a high speed CMOS readout circuit using indium bump bonds.

The hybrid concept has been taken one step further with the emergence of 3-D silicon-on-insulator (SOI) technology (Suntharalingam, 2007). The SOI approach enables the production of much more integrated monolithic sensors, as the detection and readout layers are only isolated by a thin insulating layer of silicon dioxide. Connections between the two layers are then made using three dimensional metal 'vias', similar to CMOS processing, hence the term 3-D SOI.

The main disadvantage of hybrid and SOI imagers is the much higher cost. It should be noted that the two approaches are major areas of research in their own right and further detail is beyond the scope of this thesis. They are mentioned here only for completeness.

2.6. Discussion

The main features of the imaging technologies discussed in this chapter are summarised in **Table 2.1**.

CCD	CMOS APS	Hybrid
Mature technology	New technology	New technology
Optimised for imaging	Optimised for digital logic	Spectrally optimised
Minimal system integration	Major system integration	Moderate system integration
Simple manufacturing	Complex manufacturing	Complex manufacturing
High market penetration	Low market penetration	Low market penetration
High power consumption	Low power consumption	Low power consumption
Very low read noise	Medium read noise	Low read noise
Low dark signal	Medium dark signal	Low dark signal
Charge domain operations	In-pixel charge conversion	
Serial readout	High speed parallel readout	
	Random (X-Y) pixel access	Random (X-Y) pixel access
Global shutter		
Moderate system cost	Low system cost	High system cost
Few manufacturers	Many manufacturers	Few manufacturers

Table 2.1 A comparison between CCD, CMOS APS and hybrid imaging technologies

The fundamental advantage of the CCD approach is that all charge packets are read out through the same amplifier. This means that certain offsets and noise sources introduced by the output circuit are the same for all pixels and can easily be removed with simple analogue circuitry to provide a stable image reference. The CCD manufacturing process has also been optimised for the detection of photons through many years of research and development. The relatively mature technology can now provide near perfect imaging performance in terms of detection efficiency (close to 100 %), read noise (< 1 e^-) and dark signal (1 pA/cm^2). The major drawback of the CCD approach is that it is not compatible with mainstream CMOS VLSI processing. This means that it is not practicable to provide on-chip drive circuitry or

signal processing functions. This is either because the voltage levels required are incompatible with conventional integrated circuits, such as low voltage CMOS, or because of increased power consumption. The fabrication processes also tend to be highly specific to individual manufacturers, with the result that there are few possibilities for foundry and second-sourcing of device manufacture.

The more recently developed APS technology has emerged as a competitor to the CCD due to the advantages listed in **Table 2.1**. The approach is clearly well suited to portable applications and the technology is now employed in numerous consumer-imaging devices such as digital still cameras and mobile phones. The aforementioned qualities, in conjunction with the increased potential for radiation hardness, also make the technology of interest for scientific applications such as space science and particle physics. Consequently research into APS technology is the subject of significant funding by organisations such as ESA, NASA and CERN (Turchetta et al., 2003, Clampin et al., 2005).

At present, the use of existing mainstream CMOS VLSI processes that are not optimised for imaging has tended to result in CMOS APS devices with poor performance. Efforts have been made to improve APS performance by optimising the manufacturing method to incorporate the types of custom processes employed within high-performance CCD imagers such as the pinning implant or backside illumination (see Chapter 3). However, the optimised processes are still not readily available to the scientific community. The best CCD still has a clear lead in most performance areas and consequently it has continued to dominate high quality scientific imaging applications. Future APS devices must match the standard of performance set by the CCD to be seriously considered for scientific applications. The CMOS process will have to be optimised for imaging and this will remove the cost advantage of using mainstream manufacturing processes. It is likely that that the best performing imaging device, regardless of cost, will be produced using the hybrid approach to take the best qualities of all the technologies (Janesick and Putnam, 2003).

2.7. Summary

This chapter has briefly described two of the main approaches to solid-state imaging: the CCD and the CMOS APS. The fundamental advantages and drawbacks of the two approaches were outlined along with a third solution, the hybrid imager, which aims to combine the best of both approaches. The next chapter outlines the theoretical operation of active pixel sensors in more detail and also outlines some of the developments that have been made to improve the basic design.

Chapter 3: CMOS active pixel sensor theory

Chapter 3 provides a more detailed description of the individual components that are used to form an active pixel sensor. The first section describes the operation of the p-n junction photodiode and the MOS transistor. The chapter then describes how these devices are combined to form the three transistor plus photodiode (3T) pixel. A detailed description of the operation of the pixel is then given. The chapter then discusses the range of noise sources and performance parameters used to describe image sensor behaviour. The chapter closes by describing a number of different evolutions of the 3T architecture used to improve performance.

3.1. Introduction

Several varieties of active pixel have evolved from the original passive pixel. The most popular structure is the three transistor (3T) plus photodiode design which is the focus of this thesis. The first high performance examples were demonstrated by JPL (Nixon et al., 1995), Toshiba (Iida et al, 1997) and Edinburgh University (Hurwitz et al., 1997). Further developments have since been made to the 3T pixel to optimise the performance and they are discussed towards the end of this chapter. However, the basic structures contained within the majority of active pixels are the p-n junction photodiode and the MOS transistor, therefore one must first understand the operation of these two devices to understand the operation and performance limitations of the 3T pixel.

3.2. The p-n junction

The p-n junction is one of the simplest semiconductor structures. It is used in the reverse biased mode as a photodiode and as the source and drain regions of the MOS transistor. A description of p-n junction characteristics is given below.

3.2.1. Basic characteristics

A cross section of the p-n junction is shown in **Figure 3.1**. The device is formed when two homogenous regions of n- and p- type silicon are brought into close contact (Sze, 1981). At the boundary between the two regions there is a large concentration gradient. The electron concentration in the n-type region is very high and the p-type region contains a high concentration of holes. The gradient causes electrons to diffuse from the n-type region into the p-type region and holes to diffuse in the opposite

direction. Consequently a region of negatively charged acceptor ions develops in the p-type region close to the boundary and a region of positively charged donor ions accumulates in the n-type region close to the boundary. This process leaves a region at the junction which is depleted of majority carriers known as the space-charge or depletion region. The presence of the positive and negatively charged regions causes an electric field to form across the boundary. As the electric field develops it opposes the flow of electrons due to the diffusion process and causes them to drift in the opposite direction from n- to p-type. This process occurs until an equilibrium condition is reached whereby the drift and diffusion currents are equal and opposite and zero net current flows. As a result there is a built potential barrier across the junction. Applying a positive voltage to the p-type region with respect to the n-type region reduces the potential barrier, causing the diffusion current to dominate over the drift current resulting in a net flow of current from the p-type region to the n-type region. This reduces the width of the depletion region and is known as operating in forward biased mode. If the junction is biased in the opposite manner such that the potential of the p-type region is negative with respect to the n-type region, the potential barrier across the boundary will increase and the diffusion current will be reduced, resulting in the drift current becoming the dominant component. This has the effect of widening the space charge region. This mode of operation is known as reverse-biasing. The case of the reverse biased p-n junction is most relevant to this work so it will be examined in more detail here.

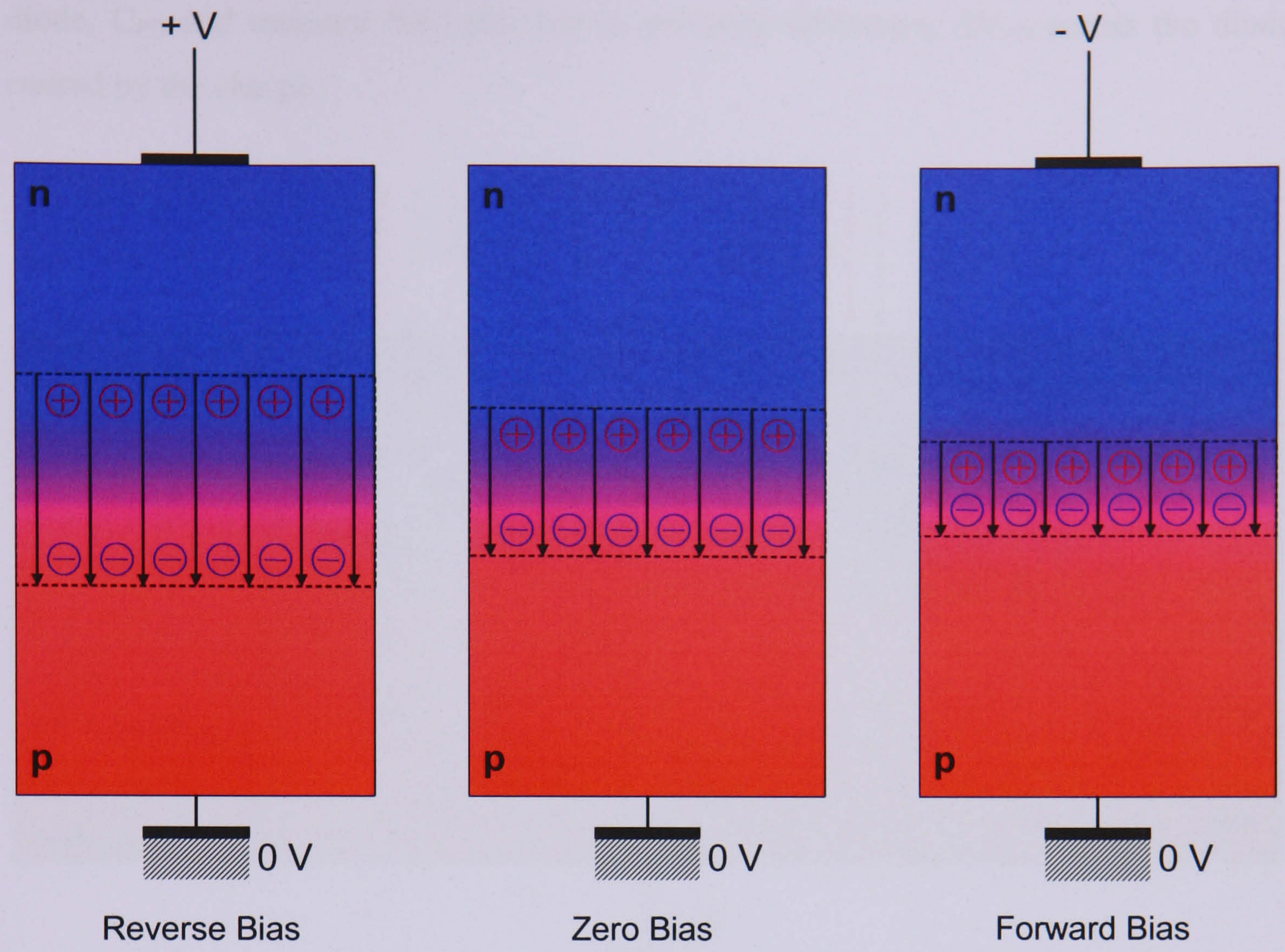


Figure 3.1 p-n junction biasing. The width of the depletion region can be controlled by forward or reverse biasing of the device.

3.2.2. The reverse biased photodiode

The p-n junction photodiode (Grove, 1967) is simply a p-n junction operated in a reverse-biased mode fabricated such that it can be exposed to light. The structure is illustrated in **Figure 3.2** and with bias applied is depleted of carriers in the depletion region shown.

Light entering the structure generates electron hole pairs within the semiconductor due to the photoelectric effect. The band gap of silicon is ~ 1.1 eV therefore only incident photons with energy greater than this will generate an electron-hole pair (i.e. wavelengths shorter than about 1.1 μm). If the charge is generated within the depletion region, it will be swept apart by the electric field across the junction, thereby causing a current to flow in the diode. The current is usually very small and, for practical device purposes, difficult to measure. It is far simpler to utilise the parasitic capacitance of the

diode, C_{PD} and measure the reduction in potential difference, ΔV_{PD} across the diode caused by the charge.

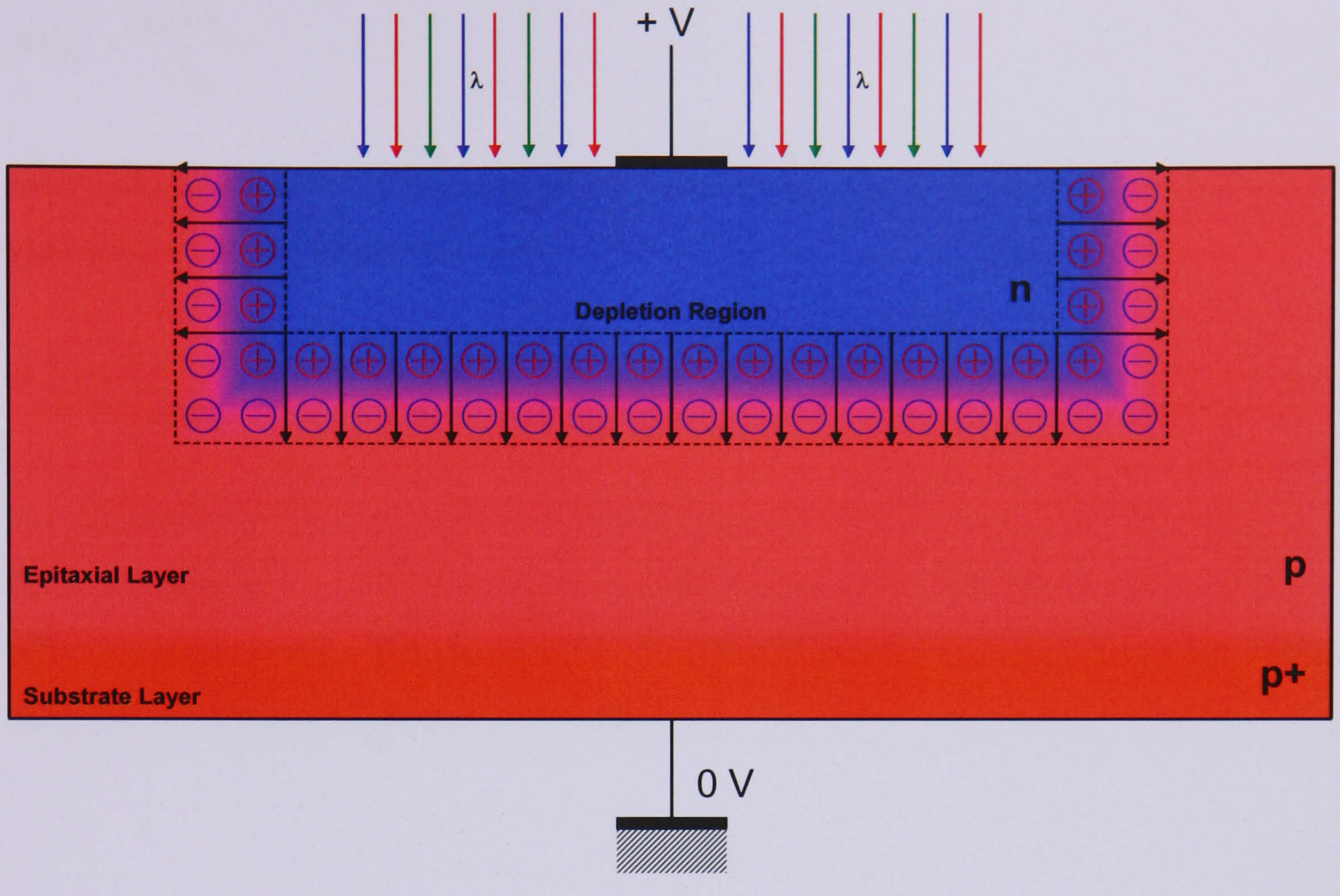


Figure 3.2 The reverse-biased p-n junction photodiode. The device normally consists of a p-type substrate into which an n-type region is introduced usually by means of ion implantation or diffusion. The depletion region is increased by reverse biasing of the device

The magnitude of the voltage change for each photo-generated carrier ($\mu V/e^-$) is known as the responsivity and is given by Equation 3.1:

$$R = \frac{\Delta V_{PD}}{\Delta N_e} \tag{3.1}$$

The voltage change ΔV_{PD} on the photodiode capacitance due to a change in charge ΔQ is:

$$\Delta V_{PD} = \frac{\Delta Q}{C_{PD}} \tag{3.2}$$

The change in charge ΔQ in terms of the fundamental parameters is:

$$\Delta Q = q_e \Delta N_e \tag{3.3}$$

where q_e is the electron charge and N_e is the total number of electrons collected by the capacitance. Substituting Equation 3.3 into Equation 3.2 gives:

$$\Delta V_{PD} = \frac{q_e \Delta N_e}{C_{PD}} \tag{3.4}$$

Substituting Equation 3.4 into Equation 3.1 gives the responsivity in terms of the diode capacitance and the electron charge:

$$R_{PD} = \frac{q_e}{C_{PD}} \tag{3.5}$$

The responsivity is therefore inversely proportional to the capacitance of the diode. The diode capacitance is determined by a number of parameters and can be designed to suit different applications. The photodiode capacitance and the associated responsivity are discussed in more detail later in this chapter.

3.3. The MOS transistor

The MOS field effect transistor (MOSFET) is one of the most important devices used in integrated circuit technology. It is the main building block of most microprocessors and semiconductor memories, and more recently it has become the fundamental component in the active pixel. A detailed description of MOS transistor operation is given below.

3.3.1. Basic characteristics

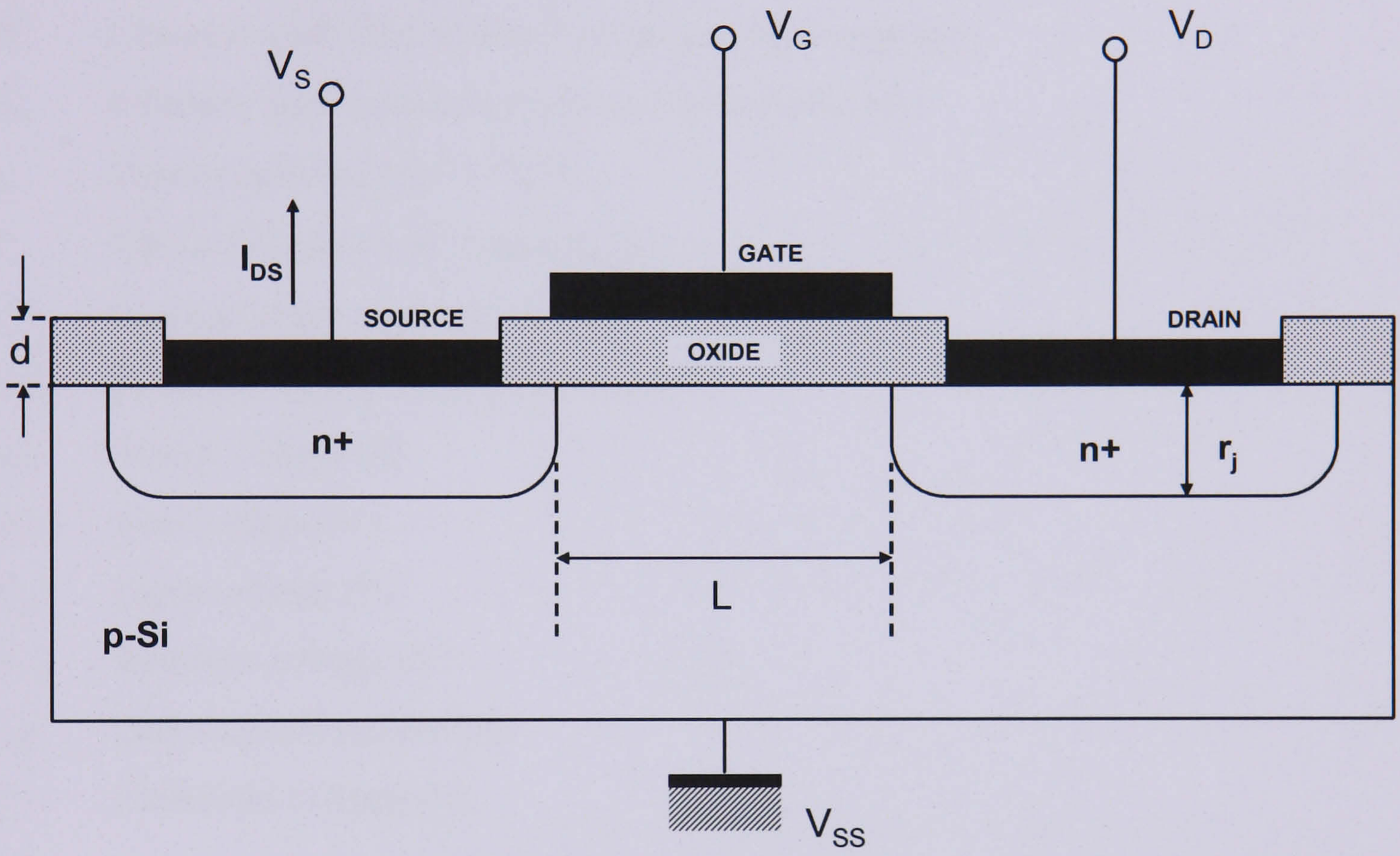


Figure 3.3 Cross section of an n-channel 'enhancement' mode MOSFET

The basic structure of an n-channel 'enhancement' type MOSFET is shown in **Figure 3.3** (Sze, 1981). It is a four terminal device consisting of a p-type substrate into which two n+ regions are formed (e.g. by ion implantation). These are known as the source and drain regions. The control electrode or 'gate' is formed over a layer of silicon dioxide (SiO_2) deposited on the surface of the substrate between the two n+ regions and known as the gate oxide. Finally three 'metal' contacts are made, one to the source, one to the gate and one to the drain region. These electrical contacts are usually made using highly doped polysilicon or a combination of silicide and polysilicon. The opposite device type is the p-channel type where the conduction is due to holes. In this case the substrate would be n-type silicon and the source and drain regions would be p+

implants. In addition to the enhancement mode MOSFET there is also the depletion type, which has an extra implant beneath the gate. This has the effect of enabling conduction between the source and drain regions with zero voltage applied to the gate.

The basic device parameters describing a MOSFET are:

L	Channel length (the distance between the source and drain regions)
y	Distance along channel from drain
W	Channel width (the width of the source/drain regions)
C_0	Effective gate capacitance per unit area in (F/cm^2)
μ	Carrier mobility ($cm^2 V^{-1} s^{-1}$)
d	Gate oxide thickness (typically Å)
r_j	Junction depth (typically in μm)
N_A	Substrate doping concentration (cm^{-2})
V_S	Source voltage (V)
V_G	Gate voltage (V)
V_D	Drain voltage (V)
V_{SS}	Substrate voltage (V)
I_{DS}	Drain-source current (A)
V_T	Threshold voltage (V)

In general all voltages are referenced to the source voltage.

If a voltage is applied between the source and drain regions, the device initially behaves like two p-n junctions connected back to back. In this case the only current which will flow is that due to reverse leakage current. However, if a large enough voltage is applied to the gate contact, a surface inversion layer or channel is created underneath the gate between the two n+ regions. This allows a current to pass through the channel from the source region to the drain region. The conductance of the surface channel can be adjusted by changing the voltage on the gate. In general the substrate voltage is kept the same as the source voltage, however in some cases the source-substrate junction can be reverse-biased.

3.3.2. The linear, pinch-off, and saturation regions

Figure 3.4, **Figure 3.5** and **Figure 3.6** illustrate the structure of the conduction channel in the three distinct regions of operation of a MOSFET. These are known as the linear or triode region, pinch-off, and the saturation region.

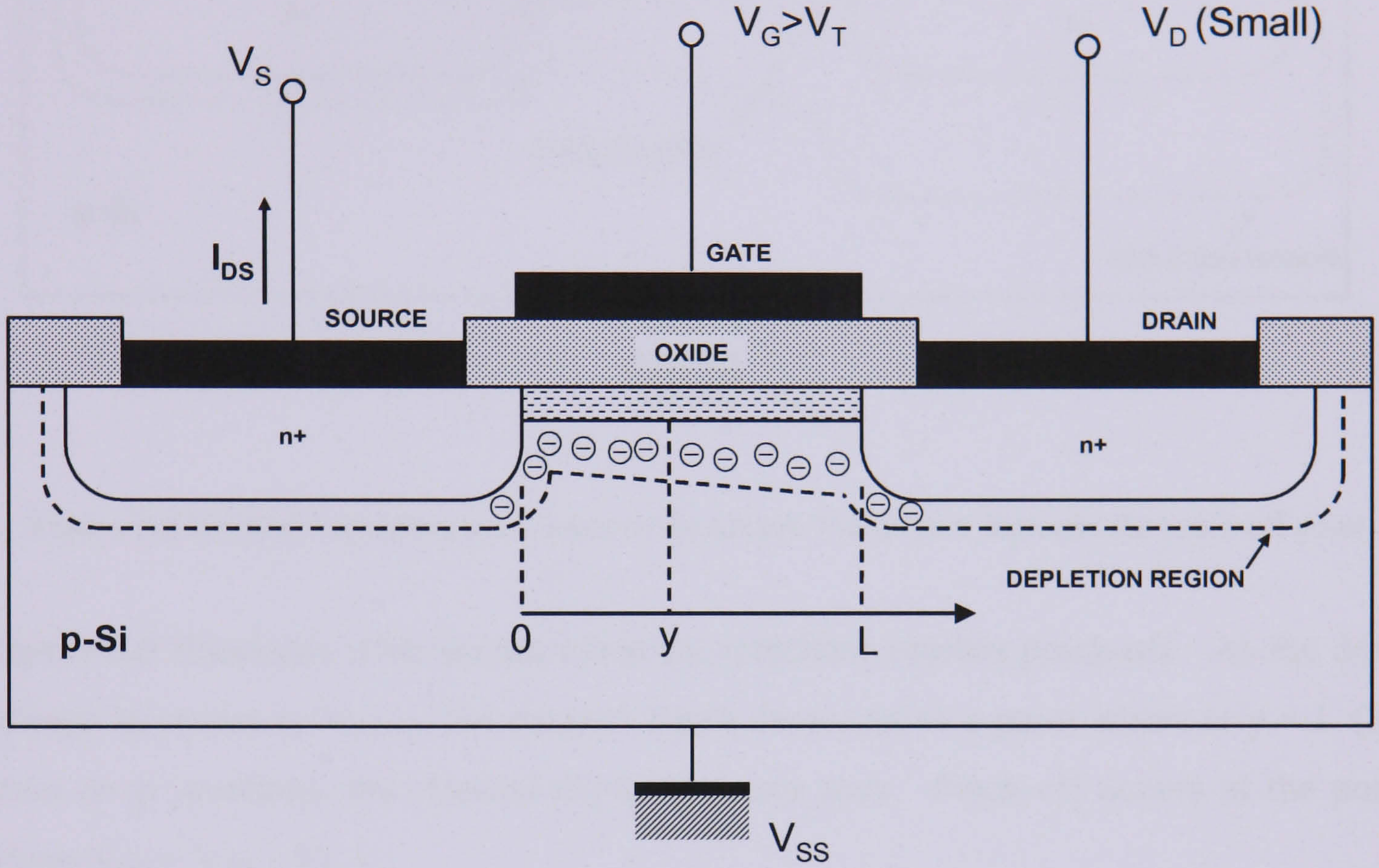


Figure 3.4 MOSFET operating in the linear region (low drain voltage)

The first region of operation, the linear (or triode) region is illustrated in **Figure 3.4**. If a voltage is applied to the gate to create an inversion layer, and a small voltage is applied between the source and drain regions, a current flows through the channel from the source to the drain regions. The channel acts as a resistance, and the current, I_{DS}, flowing is approximately proportional to the applied drain voltage, V_D. As the voltage increases the variation of current in the linear/triode region is then described by Equation 3.6 where V_{DS} and V_{GS} are the drain and gate to source voltages respectively:

$$I_{DS} = \mu C_0 \frac{W}{L}\left(V_{GS}V_{DS} - \frac{1}{2}V_{DS}^2\right) \tag{3.6}$$

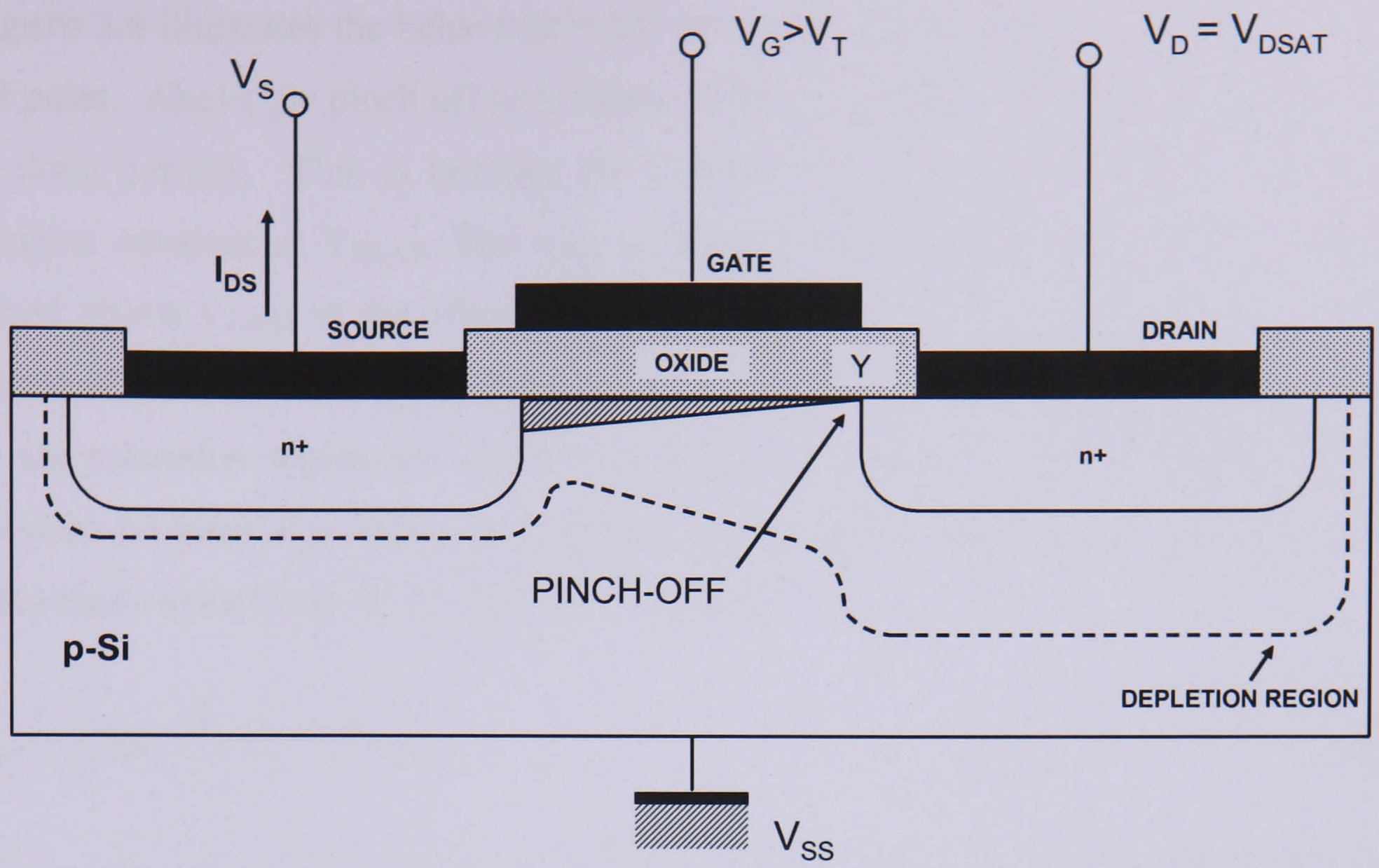


Figure 3.5 MOSFET operating at the onset of saturation. The point Y indicates the pinch-off point

Figure 3.5 illustrates what occurs when the transistor reaches pinch-off. As the drain voltage increases to V_{DSAT}, the channel depth decreases to a point where at y = L (the drain n+-p junction), the channel depth becomes zero. Pinch-off occurs at the point where $V_{DS} = V_{GS} - V_T$.

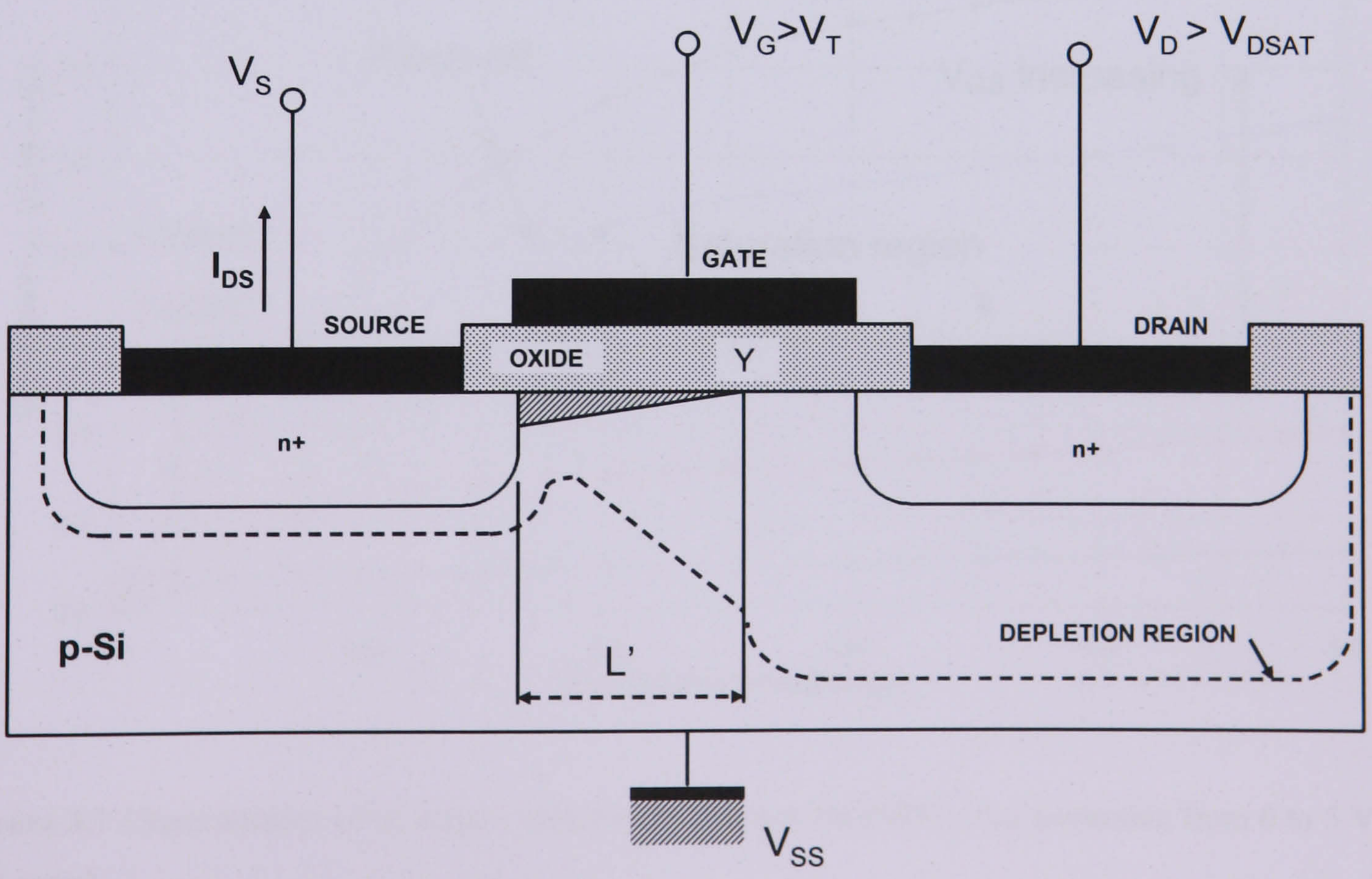


Figure 3.6 MOSFET operating beyond saturation. The effective channel length is reduced

Figure 3.6 illustrates the behaviour when the drain voltage increases beyond the pinch-off point. Above the pinch off point any increase in voltage will not increase the source to drain current. This is because for voltages above V_{DSAT} the voltage at point Y remains constant at V_{DSAT}. The only parameter that changes as the drain voltage is raised above V_{DSAT} is the effective channel length L. As V_{DSAT} increases, pinch off occurs at the edge of the drain depletion region and the channel length will reduce to L'. In the saturation region the current is no longer dependent on the drain voltage and remains constant at a value determined by the gate voltage only. The value of the saturation current is given by Equation 3.7 below.

$$I_{DS} = \frac{1}{2}\mu C_0 \frac{W}{L}(V_{GS} - V_T)^2 \qquad (3.7)$$

Figure 3.7 shows how the equations for the triode and saturation regions combine to describe the operation of an n-channel MOSFET over a range of bias conditions. The plot includes a more complex addition to the model to account for the variation of mobility with electric field, and the effects of drain current modulation above the drain pinch-off voltage.

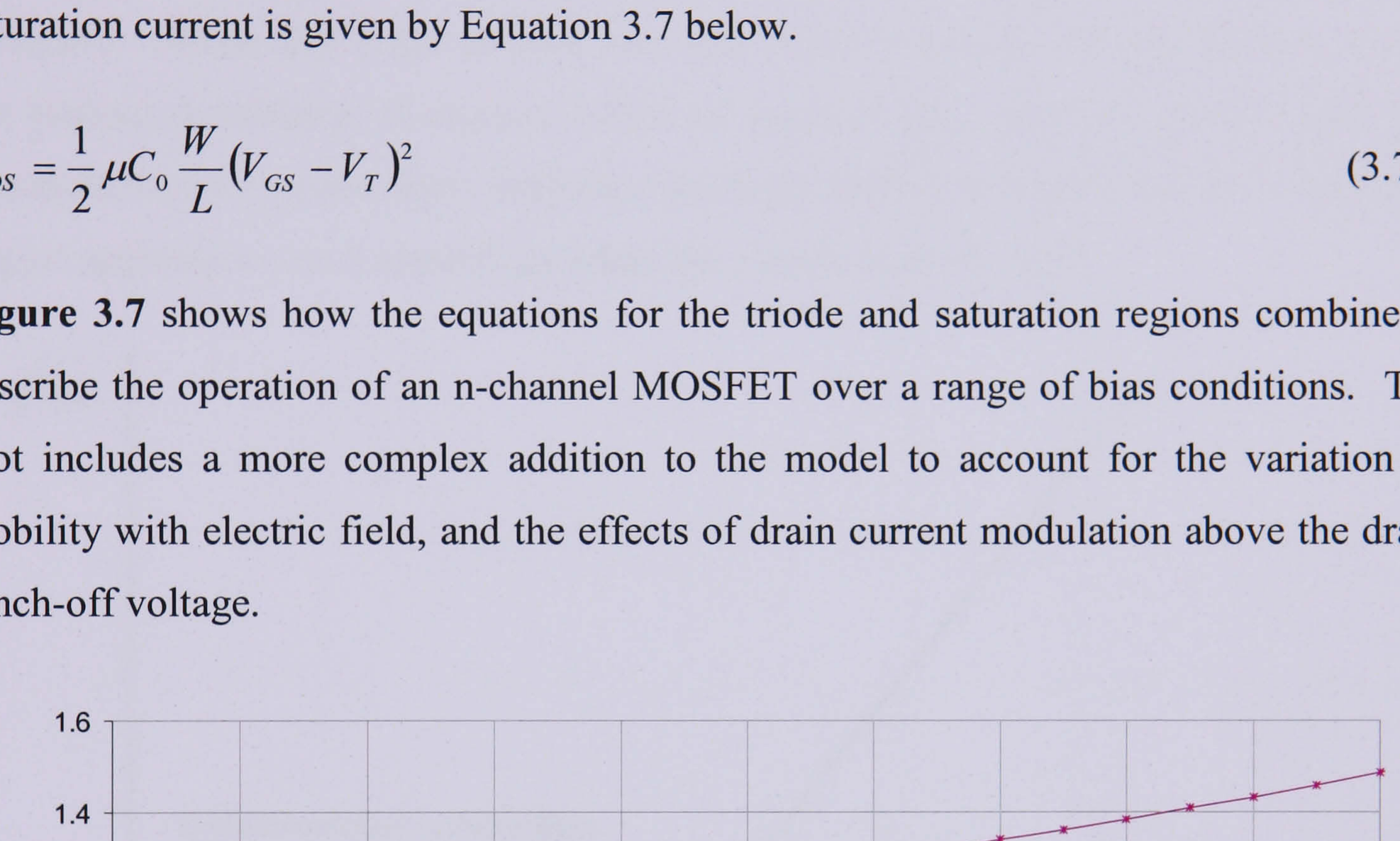


Figure 3.7 Characteristics of an n-type 'enhancement' mode MOSFET (V_{GS} increasing from 0 to 5 V in 1 V steps)

3.3.3. Sub-threshold conduction

From the above equations describing MOSFET operation it can be seen that if the gate-source voltage, V_{GS}, of the transistor is below a certain level the device will not conduct current between the source and drain regions. This voltage is known as the threshold voltage of the transistor (V_T). **Figure 3.8** shows a plot of Equation 3.7 of I_{DS} versus gate-source voltage. This shows that when the gate-source voltage is between zero and V_T no current flows and once the voltage passes V_T the current increases quadratically. Although it would seem that no current should flow when the gate voltage is below the threshold voltage, this is not actually the case. There is actually current flowing due to the thermal distribution of carriers within the source region (Gosney, 1972). The sub-threshold region is particularly important when the MOS transistor is used as a switch in digital applications as it determines when the switch turns on or off.

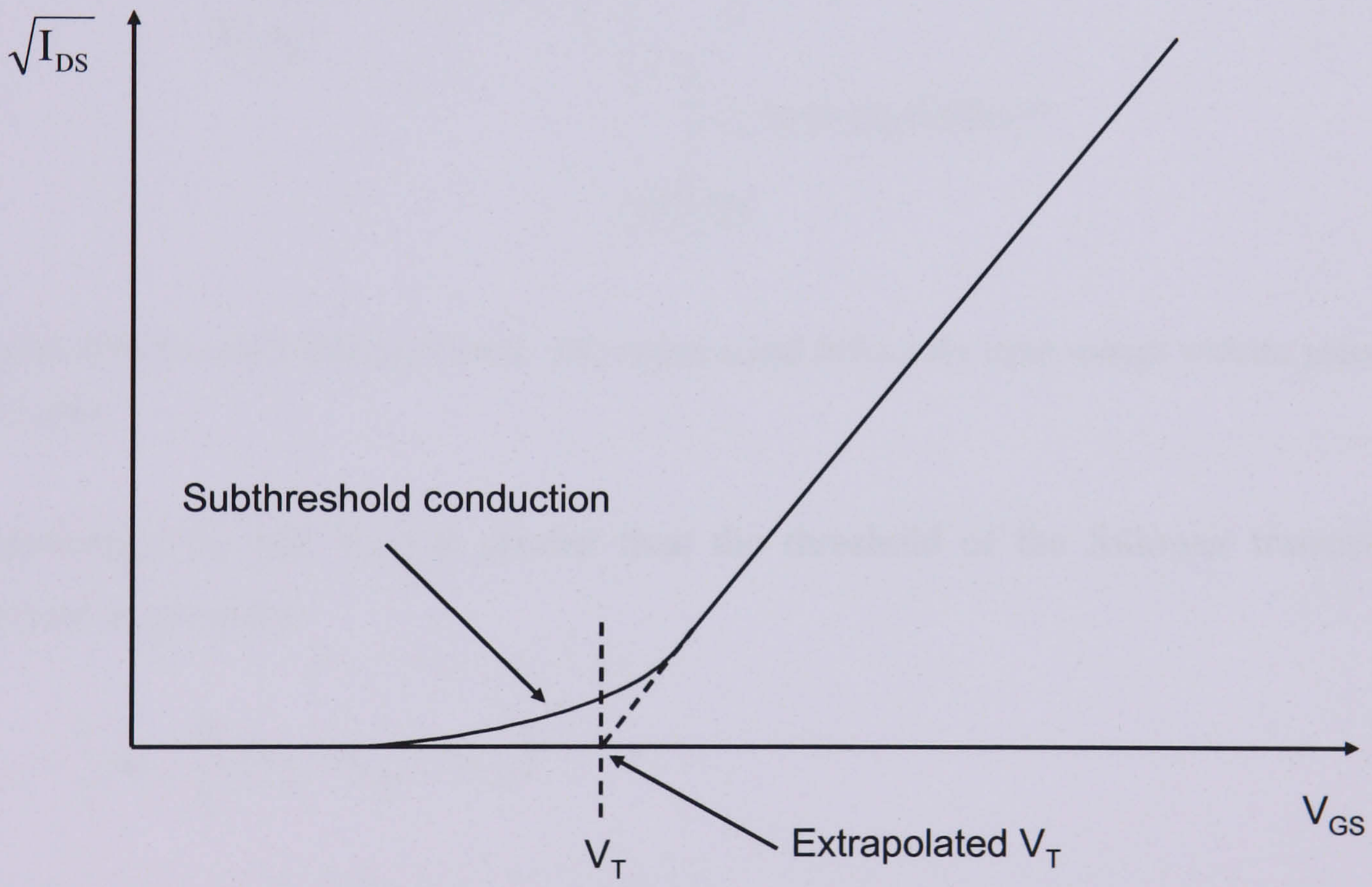


Figure 3.8 Sub-threshold conduction in an MOS transistor

3.3.4. The source follower circuit

The source follower circuit (Horowitz and Hill, 1989) is used to buffer the photodiode voltage to the output of the sensor. The configuration is shown in **Figure 3.9** and consists of two transistors connected in series between the supply voltage and ground. The load transistor is biased in the saturation region such that it is used as current source. The constant current load ($I_0 = I_{DS}$) is set in the appropriate range by adjusting

the gate to source voltage of the load transistor (V_{LG}). For a given supply voltage (V_{DD}), the gate to source voltage of the follower transistor (V_{in} - V_{out}) adjusts to match the current through it (I_{DS}).

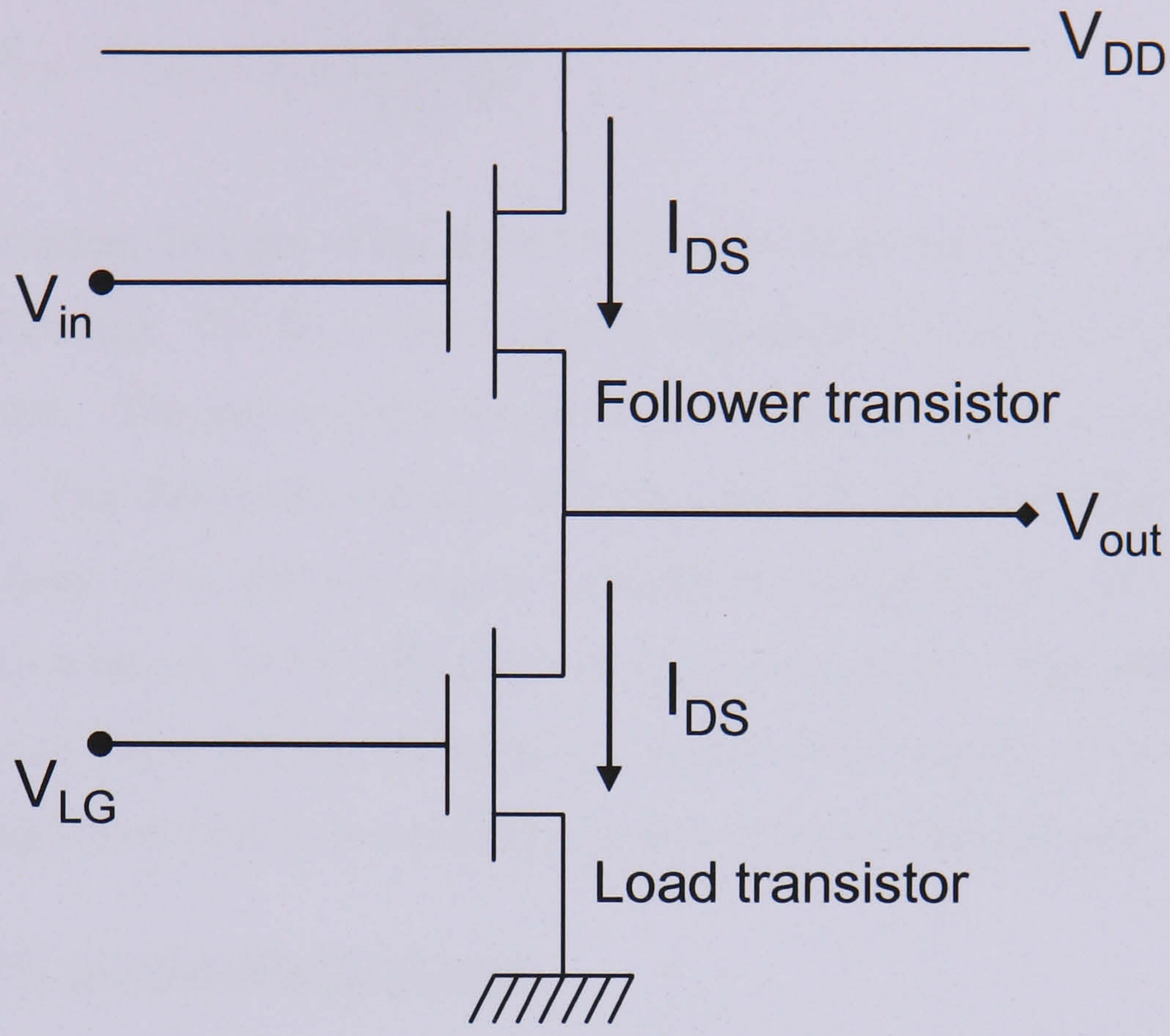


Figure 3.9 The source follower circuit. The output signal follows the input voltage with the presence of a DC offset

Assuming (V_{in} and V_{out}) is greater than the threshold of the follower transistor, the current is given by:

$$I_{DS} = \frac{1}{2}\mu C_0 \frac{W}{L}\left(V_{in} - V_{out} - V_{T,D}\right)^2 \qquad (3.8)$$

Assuming I_{DS} is constant, rearranging for V_{out} gives:

$$V_{out} = V_{in} - V_{T,D} - \sqrt{\frac{2I_{DS}L_D}{\mu C_0 W_L}} \qquad (3.9)$$

The result is that when the input voltage fluctuates the output voltage follows it with an offset being dependent on the threshold voltage of the follower transistor. The DC offset is given by:

$$V_{out} = V_{in} - V_{T,D} - (V_{load} - V_{T,L}).\sqrt{\frac{W_L.L_D}{L_L.W_D}} \tag{3.10}$$

In an ideal situation the gain of the source follower circuit would be unity, however it is always less than one. The DC offset is highly dependent on the threshold voltage of the driver transistor. The active pixel sensor uses a different follower amplifier for each pixel circuit. The threshold variation between the follower transistors from pixel to pixel can be from 10 to 100 mV due to manufacturing variations. Therefore there can be significant variations in DC offset level from pixel to pixel. This offset variation is a major source of fixed pattern noise in the active pixel sensor. Fixed pattern noise sources are discussed further in the noise sources section of this chapter.

3.4. The 3T photodiode pixel

The most common circuit architecture used in active pixel sensors is the three transistor (3T) plus photodiode pixel. The structure is popular due to its relatively simple design and conformity to many widely available CMOS manufacturing processes. The following sections focus on the 3T pixel circuit architecture and its electrical characteristics. Further details on the physical implementation of the 3T design, using CMOS processing, are given in Chapter 4.

3.4.1. Basic architecture

The 3T active pixel requires two additional transistors compared with the original passive pixel. The architecture of the pixel is shown in **Figure 3.10**. The pixel consists of four separate elements. These are:

- Photodiode
- Reset transistor
- Follower (amplifier) transistor
- Row select (enable) transistor

The reset transistor is connected in series between the photodiode and the reset drain voltage V_{RD}. The photodiode is reset to the V_{RD} reference level before an image acquisition by clocking the gate of the reset transistor high or low (depending on the transistor polarity). The photodiode voltage is buffered to the column output line by the follower transistor. A row select transistor is connected in series between the column output and the follower transistor drain to ensure the output of the pixel is only connected to the column output when necessary by clocking gate of the row select transistor.

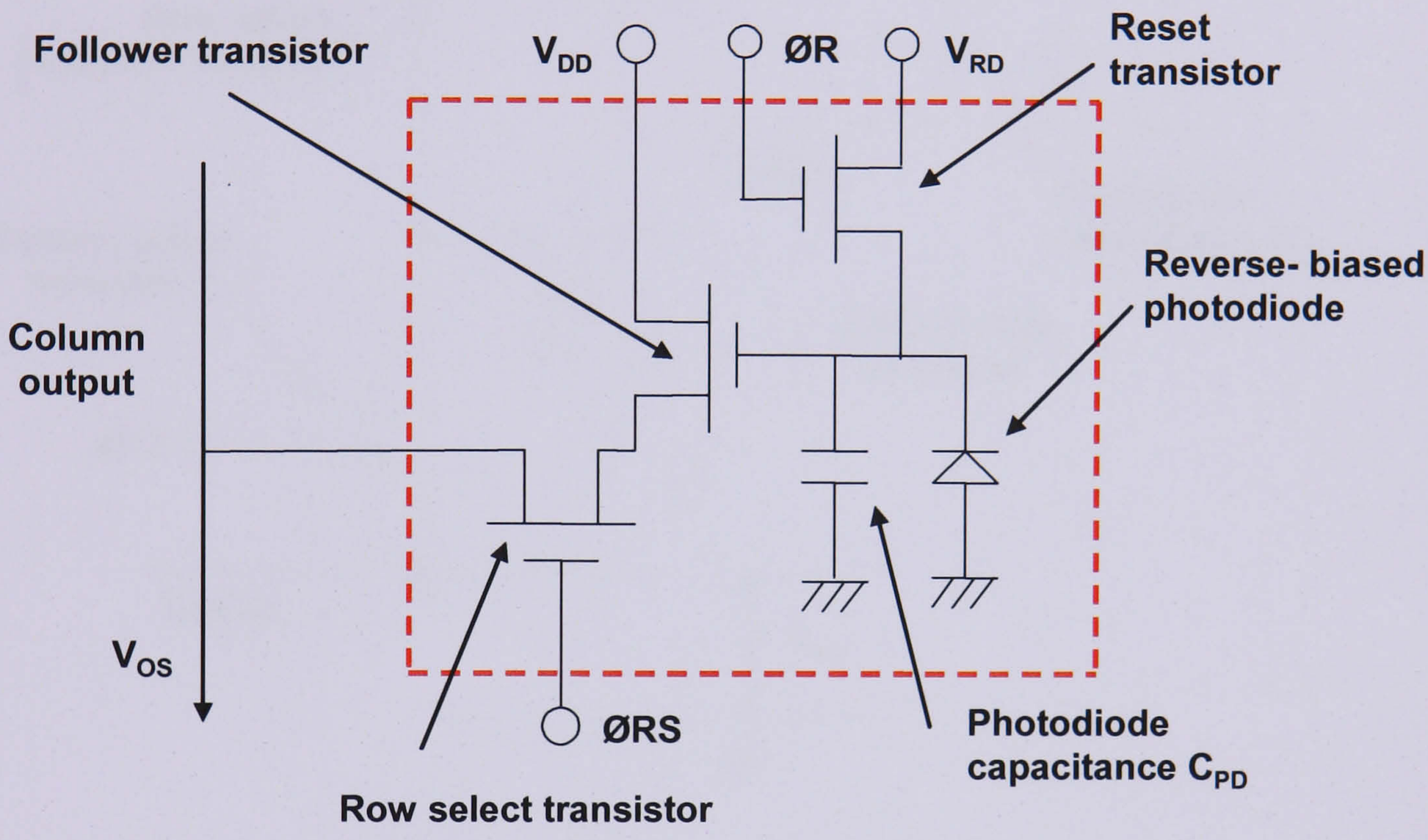


Figure 3.10 Three transistor photodiode pixel circuit schematic. The photodiode voltage is reset by turning on the reset transistor. Signal is then collected by the diode and the output voltage is buffered off chip by the source follower and a row select transistor

3.4.2. Column output circuit

The pixel photodiode output can only be read when the pixel is connected to a load transistor to complete the source follower circuit. It is possible to time-share a single load transistor between all pixels in the array, but it is more common to implement a load transistor for each column to enable parallel readout and analogue/digital signal processing. The complete 3T pixel and column output circuit is shown in **Figure 3.11**. Two extra transistors are required per column to buffer a pixel output to the array output. These are the column load transistor and the column select transistor. When a row of pixels is selected, the column select transistors are used to readout the row of

pixels in sequence. It is also possible to put a load transistor in each pixel, but the total current drain becomes excessively large.

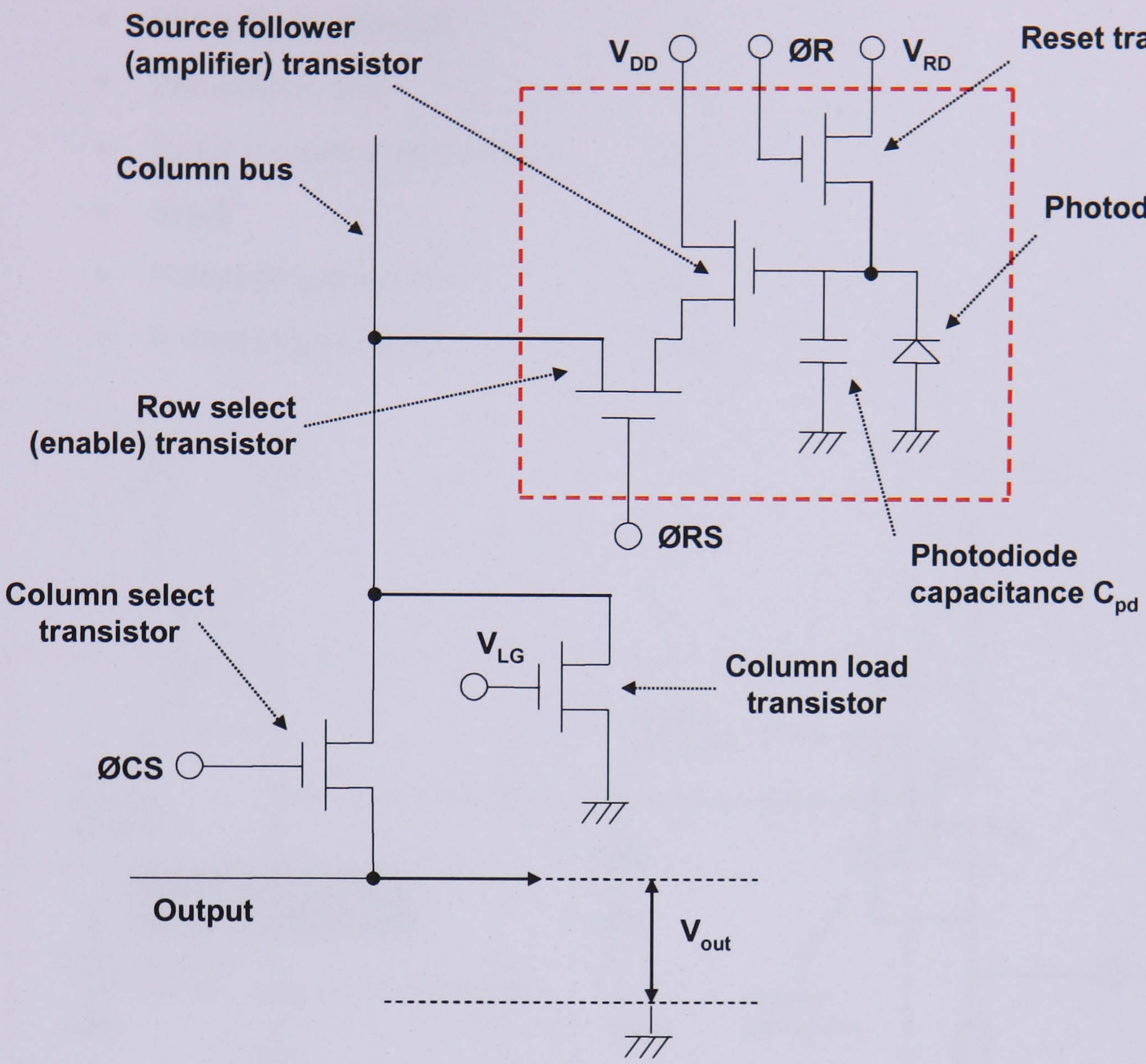


Figure 3.11 The three transistor plus photodiode pixel and column readout circuit

3.4.3. Responsivity and pixel capacitance

The photodiode in the 3T pixel is connected to the gate of the in pixel source follower transistor, which 'senses' any voltage fluctuation and translates it to a voltage change at the source. The connection at the follower gate is therefore known as the sense node. The photodiode is directly connected to the sense node and therefore the node responsivity is directly related to the photodiode capacitance, as shown earlier in Equation 3.1. However there are other parasitic capacitances within the pixel adding to the photodiode capacitance. The combination of these capacitances is known as the sense node capacitance, C_{Node}, and the resulting voltage change per electron sensed at the node is the sense node responsivity, R_{Node}, given by q_e/C_{Node}.

The different contributions towards the sense node capacitance in a 3T pixel are illustrated in **Figure 3.12** and are as follows:

- Photodiode sidewall C_{PDS}
- Photodiode area C_{PDA}
- Reset transistor gate-source C_{RGS}
- Track C_{Track}
- Follower gate-source C_{FGS}
- Follower gate-drain C_{FGD}

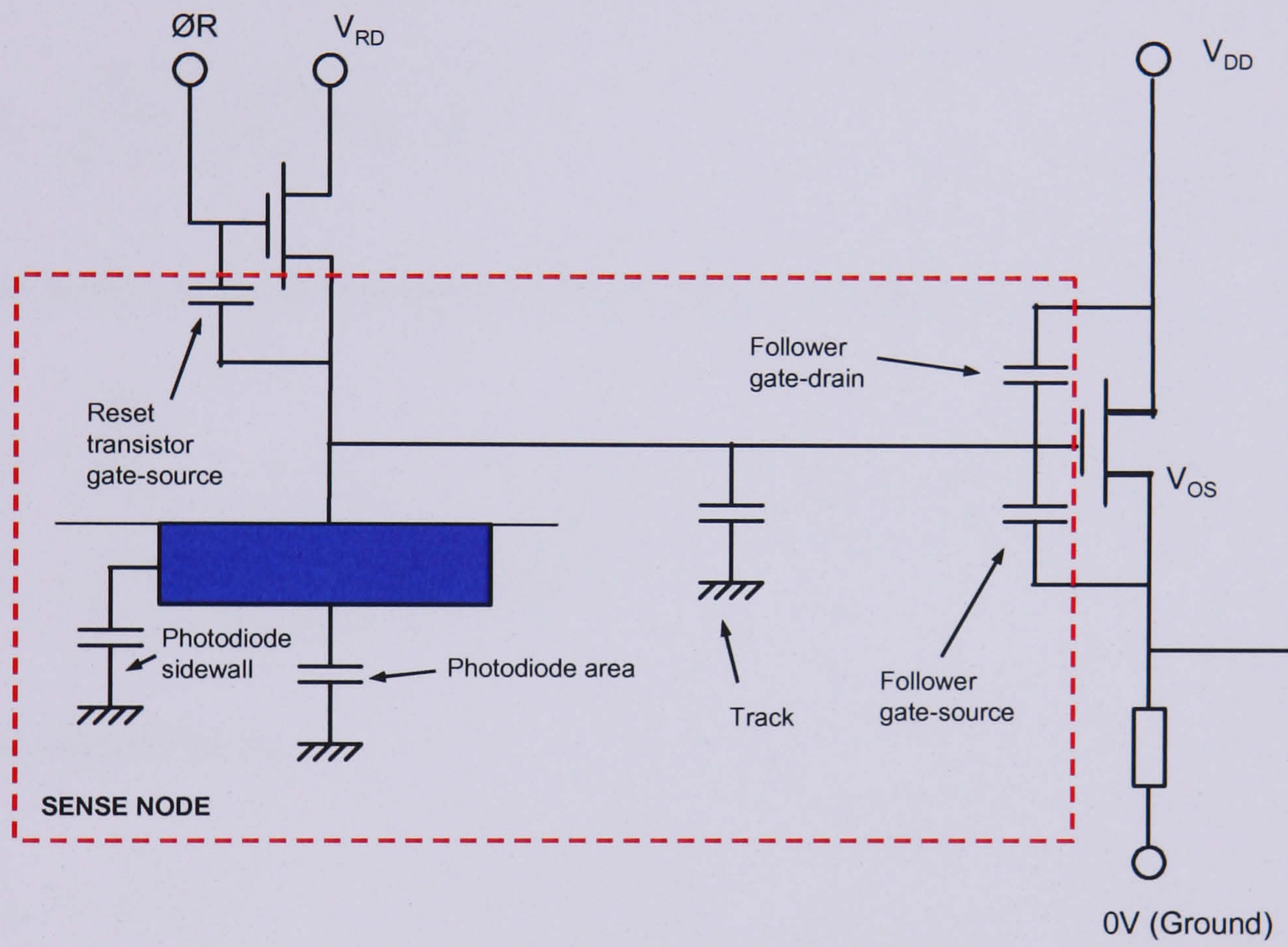


Figure 3.12 Sources of parasitic capacitance in a 3T photodiode CMOS pixel

The track and gate source capacitances are highly process dependent and are usually given as empirical values (fF/μm) which are directly proportional to the track or gate-source/drain dimensions. The largest of these capacitances is the photodiode capacitance. The photodiode capacitance comprises two components, the diffusion capacitance and the depletion layer capacitance. In the case of a reverse biased junction the majority of the contribution is from the depletion layer capacitance. The diffusion component is only significant when the junction is forward biased. As the photodiode in a CMOS active pixel is always reverse biased, only the theory behind the depletion layer capacitance will be considered here.

The depletion region charge per unit area is given by (Sze, 1981):

$$Q_j = \sqrt{(2\varepsilon_{si} q \frac{N_A N_D}{N_A + N_D})(\phi_0 - V_{PD})} \tag{3.11}$$

Where ε_{Si} is the dielectric constant for silicon, q is the electron charge, N_A and N_D, are the acceptor and donor concentrations respectively, ϕ_0 is the built in potential of the diode, and V_{PD} is the reverse bias voltage. The depletion region width, W_j is given by:

$$W_j = \sqrt{\frac{2\varepsilon_{si}}{q} \frac{N_A + N_D}{N_A N_D} (\phi_0 - V_D)} \tag{3.12}$$

The depletion layer capacitance per unit area is defined as:

$$\begin{aligned} C_{PD} &= \frac{dQ_j}{dV_{PD}} \\ &= \sqrt{\frac{\varepsilon_{si} q_e}{2} \frac{N_A N_D}{N_A + N_D} (\phi_0 - V_{PD})^{-1}} \end{aligned} \tag{3.13}$$

This simplifies to:

$$C_{PD} = \frac{C_{PD_0}}{\sqrt{1 - \frac{V_{PD}}{\phi_0}}} \tag{3.14}$$

Where C_{PD0} is the capacitance per unit area of the device under zero bias conditions. This is only a function of the physical parameters of the device and is defined as:

$$C_{PD_0} = \sqrt{\frac{\varepsilon_{si} q_e}{2} \frac{N_A N_D}{N_A + N_D} \phi_0^{-1}} \tag{3.15}$$

The total node capacitance is therefore:

$$C_{Node} = C_{PD} + C_{RGS} + C_{FGS} + C_{FGD} + C_{Track} \tag{3.16}$$

Substituting Equation 3.14 into 3.16 gives:

$$C_{Node} = \frac{C_{PD_0}}{\sqrt{1 - \frac{V_{PD}}{\phi_0}}} + C_{RGS} + C_{FGS} + C_{FGD} + C_{Track} \tag{3.17}$$

Therefore the sense node capacitance increases as the voltage decreases. Recall the responsivity at the sense node is:

$$R_{Node} = \frac{q_e}{C_{Node}} \tag{3.18}$$

Therefore the sense node responsivity decreases as the voltage on the node decreases. Under constant illumination, assuming all photons incident on the photodiode generate charge within it, the photocurrent i_{ph} is related to the incident photon flux I_0 photons/cm²/s by:

$$i_{ph} = I_0 A_D \tag{3.19}$$

Where A_D is the area of the diode. Then, starting with the sense node (photodiode) at an initial reset voltage V_{RD}, the resulting variation with time may be described as follows:

$$V_{Node}(t) = V_{RD} - i_{ph} t R_{Node} \tag{3.20}$$

Substituting 3.18 and 3.19 into 3.20 gives:

$$V_{Node}(t) = V_{RD} - \frac{I_0 A t q_e}{C_{Node}} \tag{3.21}$$

Therefore the photodiode output will be non-linear because as the voltage across the photodiode reduces, the capacitance increases and the node responsivity reduces. So under constant illumination, the rate of discharge of the diode will reduce as photo-generated charge accumulates. The non-linearity of the node voltage as a function of time is shown in **Figure 3.13**.

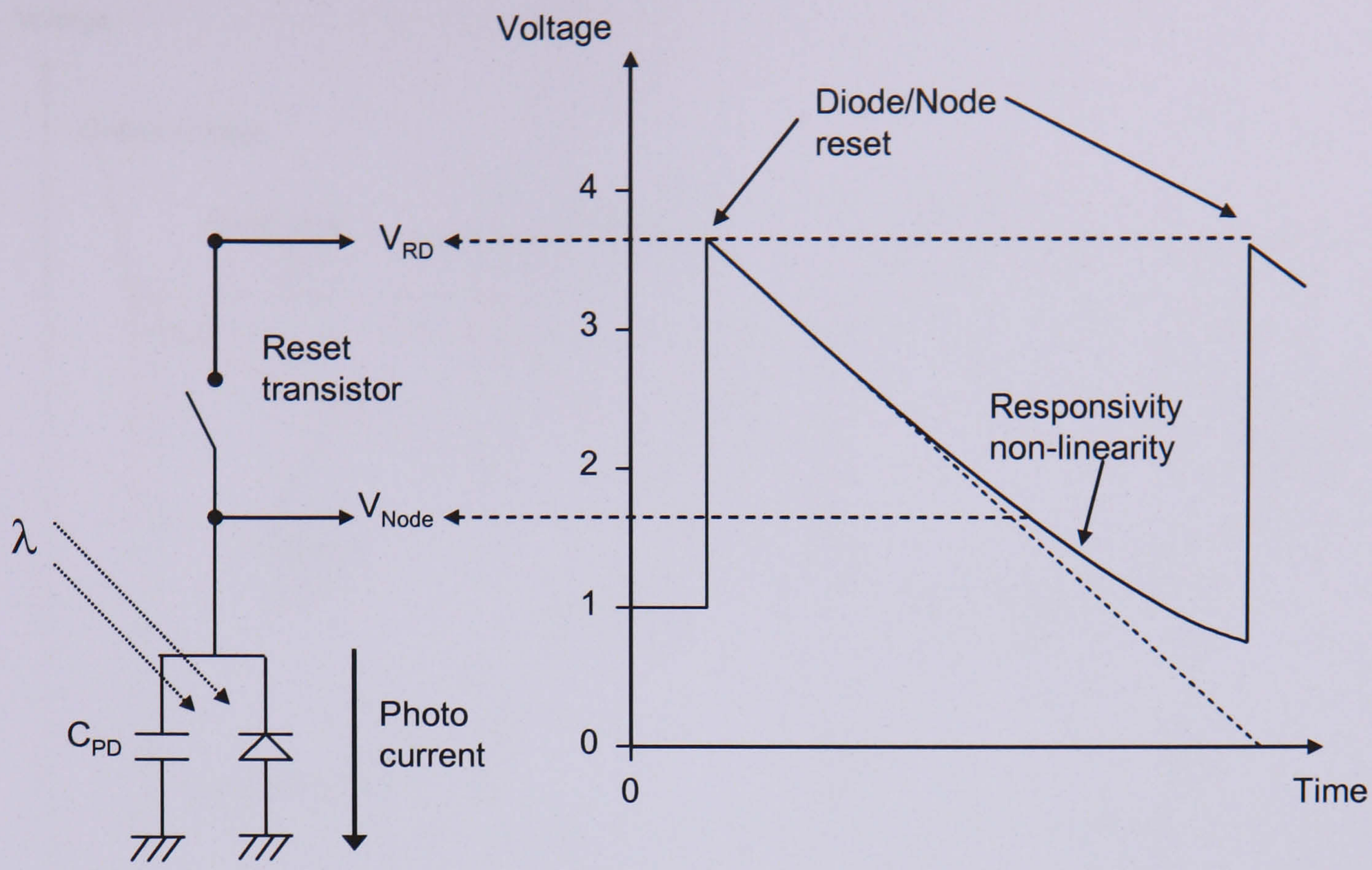


Figure 3.13 The photodiode in integrating mode. The diode is reverse biased to a reference level by closing the switch. When the switch is opened the voltage reduces due to collection of photo generated charge

3.4.4. Pixel operation

Typical operation of a 3T pixel is illustrated in **Figure 3.14**. By applying a pulse to the gate of the reset transistor to turn it on, the photodiode is initially biased to the reset level and then left floating. Any free carriers collected by the diode will reduce the potential difference across it until the pixel is reset or it reaches saturation. When a signal is measured from a given pixel, the select transistor for that pixel is similarly pulsed on, thereby completing the source follower circuit between the in-pixel driver (follower) transistor and the column load transistor, to buffer the pixel output to the array output. Although the photodiode output can in principle discharge down to 0 V, the pixel output never reaches that point. This is because the gate-source voltage of the in pixel follower transistor reduces to below its threshold level and it turns off. This can be seen as the pixel saturates in **Figure 3.14**. Note that the source follower circuit introduces an extra source of non-linearity because the, less than unity, gain varies with the bias conditions. It also introduces also a negative DC offset relative to the sense node (photodiode) voltage.

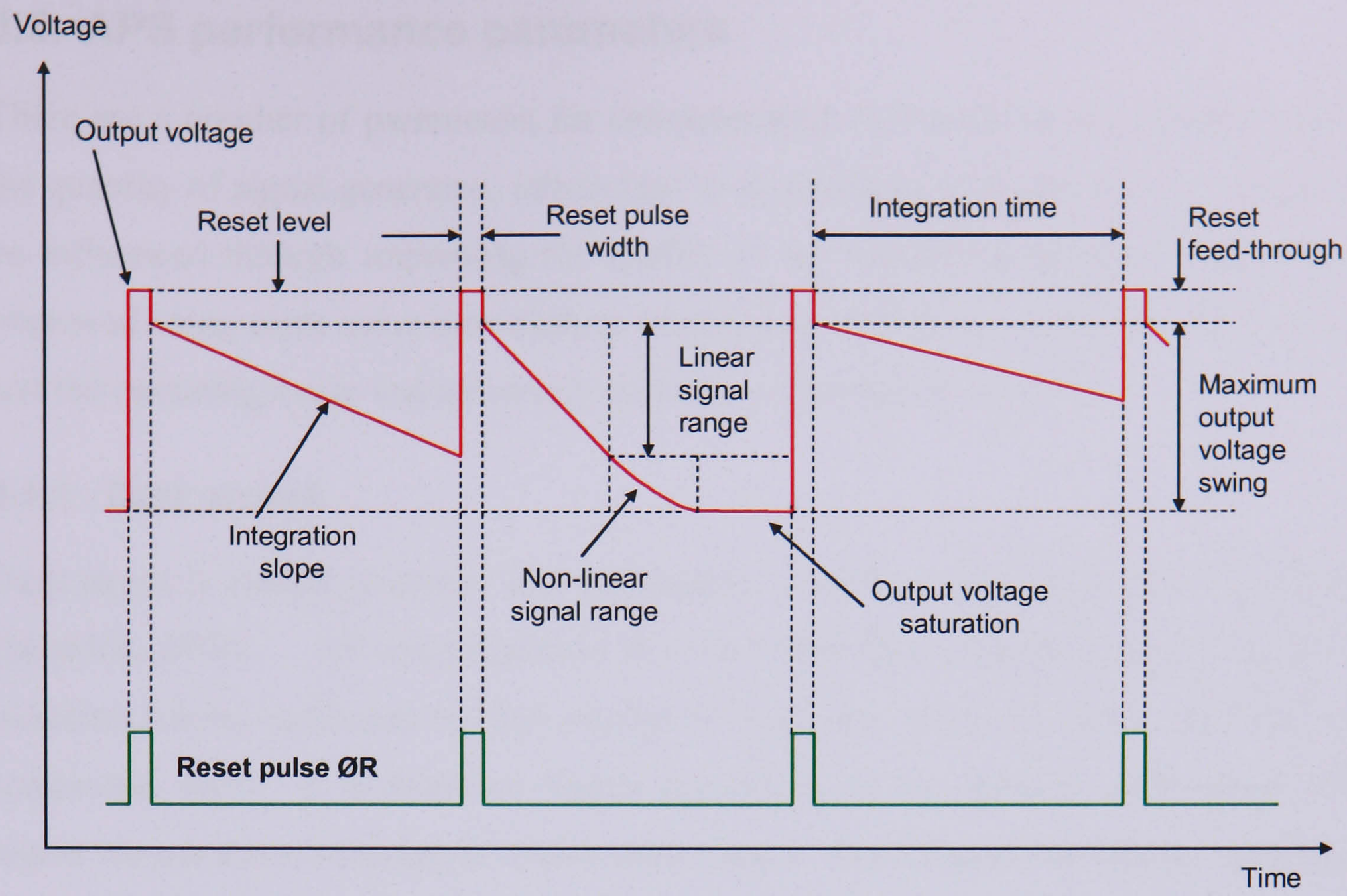


Figure 3.14 Typical operation of a 3T active pixel under varying illumination levels (note the two waveforms are not to the same scale)

3.4.5. Summary

A significant advantage of the three-transistor photodiode pixel is that its main components conform to conventional CMOS fabrication processes, therefore it is simple to produce by out sourcing to an external wafer "foundry". A further benefit is the minimal number of active elements required within the pixel, compared to more advanced designs, results in a higher fill factor and improved quantum efficiency for a given pixel size.

The architecture is incompatible with pixel rate CDS (described in the next section) therefore the read noise is limited by the noise level on the reset transistor. The pixel also has a non-linear response due to variation of photodiode capacitance with signal level, although this can be an advantage if extended dynamic range is required. The photodiode pixel also has major problem with image lag. Image lag occurs when the photodiode is not fully reset to the reset voltage before the next integration and some charge from the previous image remains on the diode. This is a particular problem for video rate applications.

3.5. APS performance parameters

There are a number of parameters for characterising APS performance. Some relate to the quantity of signal generated, others lead to degradation in image quality. Some can be influenced through improving the quality of the fabrication process, some can be improved using extra noise cancellation circuitry and others are intrinsic to the material and the operating mode and ultimately limit the performance of a device.

3.5.1. Dark signal

Dark signal is charge generated and collected by a device under totally dark conditions (Janesick, 2001). All semiconductor devices suffer from leakage currents caused by electrons having sufficient thermal energy to break free from the lattice and enter the conduction band. It is therefore highly dependent on the ambient temperature, with higher temperatures resulting in higher dark signals. Dark signal can double for every 5 - 8 °C increase in temperature. It is also highly dependent on the design of the sensor and the manufacturing process used, especially from localised imperfections in the silicon wafer called generation/recombination centres or "traps". Some of the possible sources of leakage current are:

- Surface states
- Impurities close to the Si-SiO_2 interface
- Impurities in the bulk silicon
- Crystal defects

To compare dark signals obtained from different devices and operating conditions the values are normalised to an effective current per unit area (nA/cm^2), or per pixel. (e^-/pixel/second). Also due to the temperature dependence, results are usually quoted at a given device temperature. Dark signal can vary greatly from pixel to pixel due to the manufacturing process variations. This variation is known as dark signal non-uniformity (DSNU) and is a form of dark fixed pattern noise. Dark current also exhibits shot noise characteristics therefore fluctuation of the signal obeys poissonian statistics and is equal to the square root of the mean level. Mean dark signal can be suppressed by cooling the device. DSNU can be compensated for by the subtraction of a dark reference frame. Dark current shot noise cannot be eliminated and reduction is only possible by suppressing the overall mean level e.g. by reducing the operating

temperature. A more detailed discussion of the factors affecting APS dark signal is given in Chapter 7.

3.5.2. Quantum efficiency

The previous section assumed that all photons incident on the diode produce electron hole pairs. This is not necessarily the case. The important parameter that is used to quantify the conversion efficiency of the diode is the quantum efficiency (QE), η. The quantum efficiency is defined as the fraction of the incident photons that generate useful signal and, for optical wavelengths, this is essentially the mean number of electron-hole pairs, (N_e) generated per incident photon (N_ν):

$$\eta = \frac{N_e}{N_\nu} \tag{3.22}$$

A more useful form of Equation 3.22 in terms of measurable quantities is:

$$\eta = \frac{I_\lambda hc}{q_e \lambda P_\lambda} \tag{3.23}$$

Where I_λ is the current due to the photo generated charge, P_λ is the optical power of the incident radiation, h is Planck's constant and λ is the wavelength of the incident radiation. At shorter UV and X-ray wavelengths the photo-generated carriers are ejected with sufficient energy that additional carriers are generated by impact ionisation, thus more than one electron-hole pair is now generated per incident photon.

There are two main factors affecting the quantum efficiency of a device. Firstly, the interaction of photons with layers above the surface of the photodiode and, secondly, the interaction of photons within the silicon diode itself. At the surface of the photodiode it is possible that incident photons do not enter the silicon due to absorption, reflection or interference effects in the overlying layers. The nature of these effects is highly dependent on their composition, as discussed in more detail later on in this chapter. Thus, assuming a photon reaches the surface of the silicon, the main factor affecting the resulting quantum efficiency is the distance into the silicon at which the photon is absorbed (Dash and Newman, 1955). The absorption process is characterised

in terms of the absorption coefficient α, where variation of the photon flux with distance d into the material is given by:

$$I_d(\lambda, d) = I_0 e^{-\alpha(\lambda)d} \tag{3.24}$$

Where $\alpha(\lambda)$ is the absorption coefficient for a given photon wavelength (λ) and I_0 is the flux measured at d = 0. The absorption coefficient has a very strong dependence on wavelength. The absorption coefficient can be used to calculate the absorption length, which is defined as the depth at which the photon flux is reduced to 1/e of the value at the surface. It is important to note that this is not the depth at which *all* photons are absorbed. It is between this depth and the surface that 63% of the incident photons will be absorbed. A plot of the absorption length versus wavelength for silicon at 77 K and 293 K is shown in **Figure 3.15**.

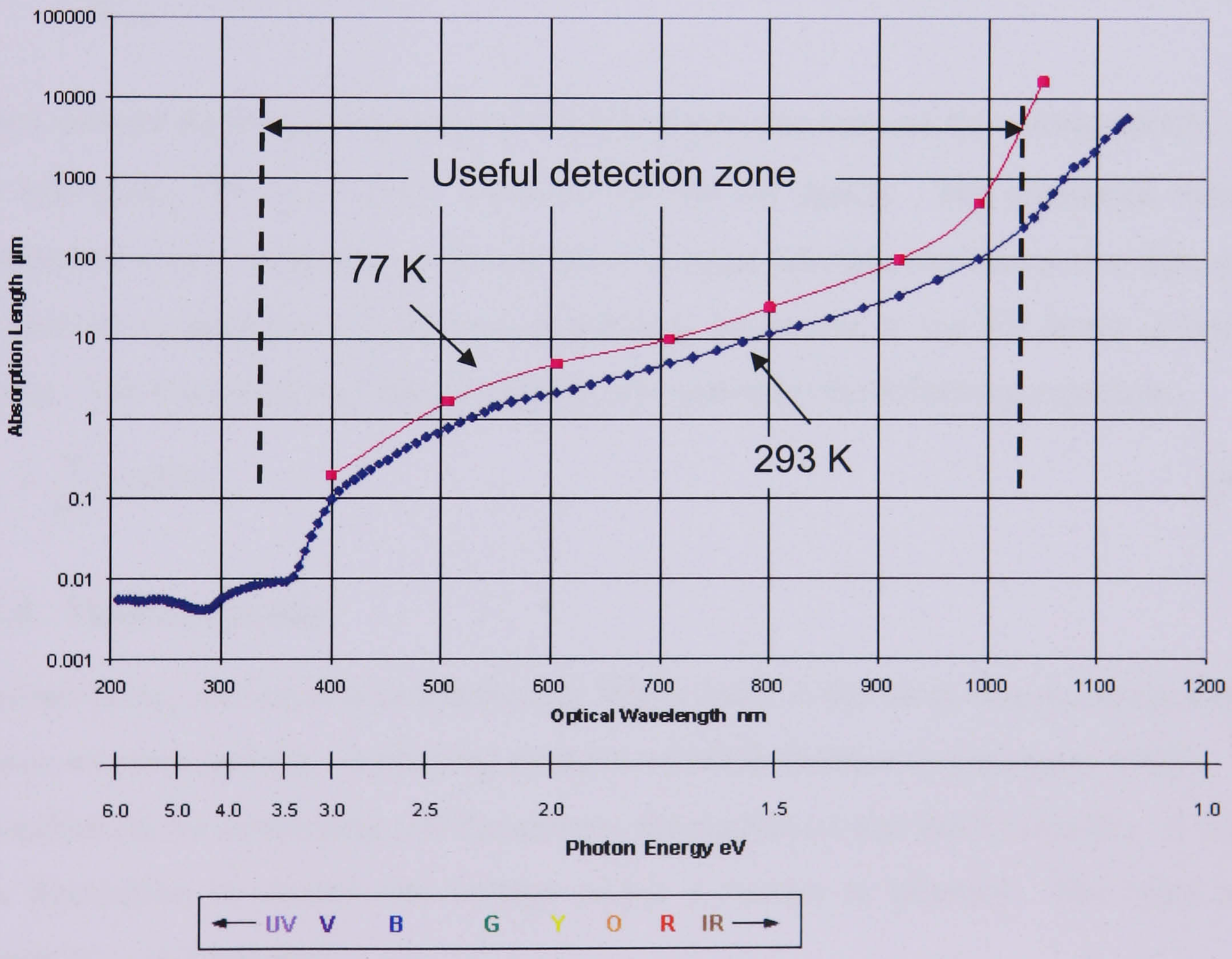


Figure 3.15 Absorption Length of light in silicon for T = 77 K and 293 K and indication of useful detection zone for typical silicon thickness

It can be seen that at wavelengths longer than 1100 nm the absorption length is greater than 1000 µm and the silicon is effectively transparent. This is primarily due to the

photons having insufficient energy to excite electrons across the band gap of silicon (~ 1.1 eV at room temperature). At much shorter wavelengths the absorption coefficient is very high and hence the absorption length is very small. These photons are therefore absorbed very close to the surface of the silicon where the recombination lifetime is short and the carriers recombine before migration to the depletion region. A more detailed discussion of the factors affecting APS quantum efficiency is given in Chapter 8: Electro-optical Characterisation.

3.5.3. Fill factor

A further parameter closely related to quantum efficiency is the fill factor (FF). The fill factor of the image sensor pixel is defined as the ratio of the photosensitive area to the total pixel area.

$$FF = \frac{A_{Photosensitive}}{A_{Pixel}} \times 100\,\% \tag{3.25}$$

When comparing the performance of CMOS pixels one can use the measured QE, η or the interacting QE, η_{int} which accounts for the fill factor. The measured value is appropriate when comparing different pixel designs whereas the interactive figure can be used for comparison of different photodiode structures, if the fill factor is reliably known. The measured and interacting QE are related by the following equation:

$$\eta_{int} = \frac{\eta}{FF} \times 100\% \tag{3.26}$$

3.5.4. Thermal noise

Thermal noise, also known as Johnson or White noise is the noise component generated within resistors and the conducting channel of MOS transistors (Johnson, 1928). It is dependent on the temperature of the system, the resistance and the bandwidth. It results in a fluctuation in current and voltage across a resistor or channel. The r.m.s noise voltage V_{rms} is given by:

$$V_{rms} = \sqrt{4kTBR} \tag{3.27}$$

Where k is the Boltzmann constant, T is the temperature, B is the bandwidth and R is the resistance. Note, however, that T is the temperature of the conduction electrons, which can be considerably higher than the surrounding silicon, as described later.

3.5.5. Reset noise

Reset noise is the fluctuation in voltage level when resetting a capacitance, such as that of a CCD (Hynecek 1990) or active pixel sense node (Tian et al., 1999). The reset operation effectively samples and holds on the capacitance the thermal noise due to any series resistance, R that is present. **Figure 3.16** shows the pixel reset and equivalent circuit.

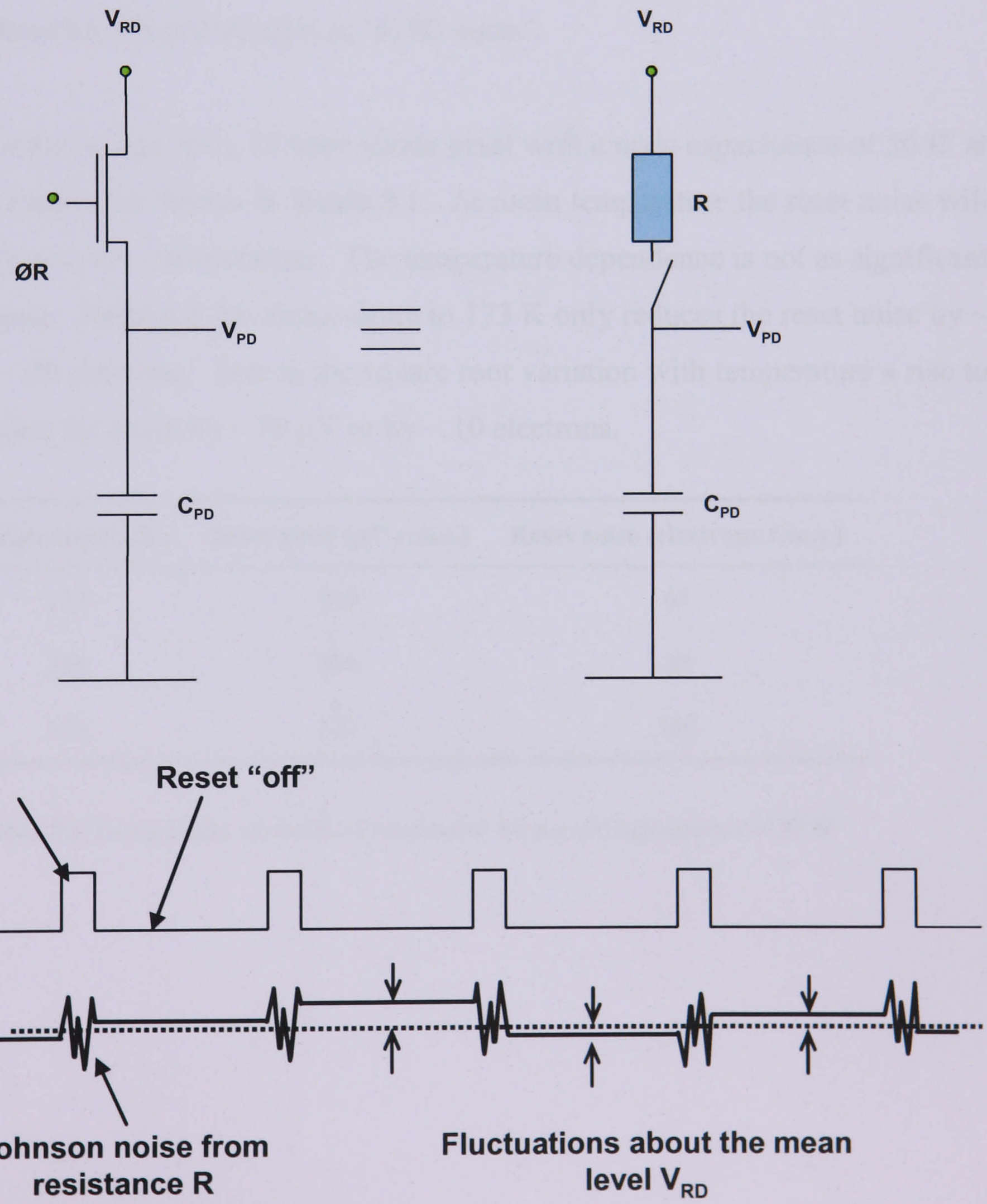


Figure 3.16 Reset noise fluctuations

The r.m.s. fluctuation in the voltage level is then actually independent of the value of the series resistance and is only dependent on the temperature, T in Kelvin, and the value of the capacitance, C, being reset. The fluctuation in volts is given by:

$$V_{n\,rms} = \sqrt{\frac{kT}{C}} \tag{3.28}$$

The fluctuation in terms of electrons is:

$$N_{e\,rms} = \sqrt{\frac{kTC}{q_e^2}} \tag{3.29}$$

The noise is therefore often described as "KTC noise".

Typical reset noise values for a 3T photodiode pixel with a node capacitance of 50 fF at various temperatures are shown in **Table 3.1**. At room temperature the reset noise will be ~ 0.3 mV (r.m.s) or ~ 90 electrons. The temperature dependence is not as significant as for dark signal. Reducing the temperature to 173 K only reduces the reset noise by ~ 70 μV or by ~ 20 electrons. Due to the square root variation with temperature a rise to 373 K only raises the noise by ~ 30 μV or by ~ 10 electrons.

Temperature (K)	Reset noise (μV r.m.s.)	Reset noise (electrons r.m.s.)
173	219	68
300	288	90
373	321	100

Table 3.1 Temperature variation of reset noise for a node capacitance of 50 fF

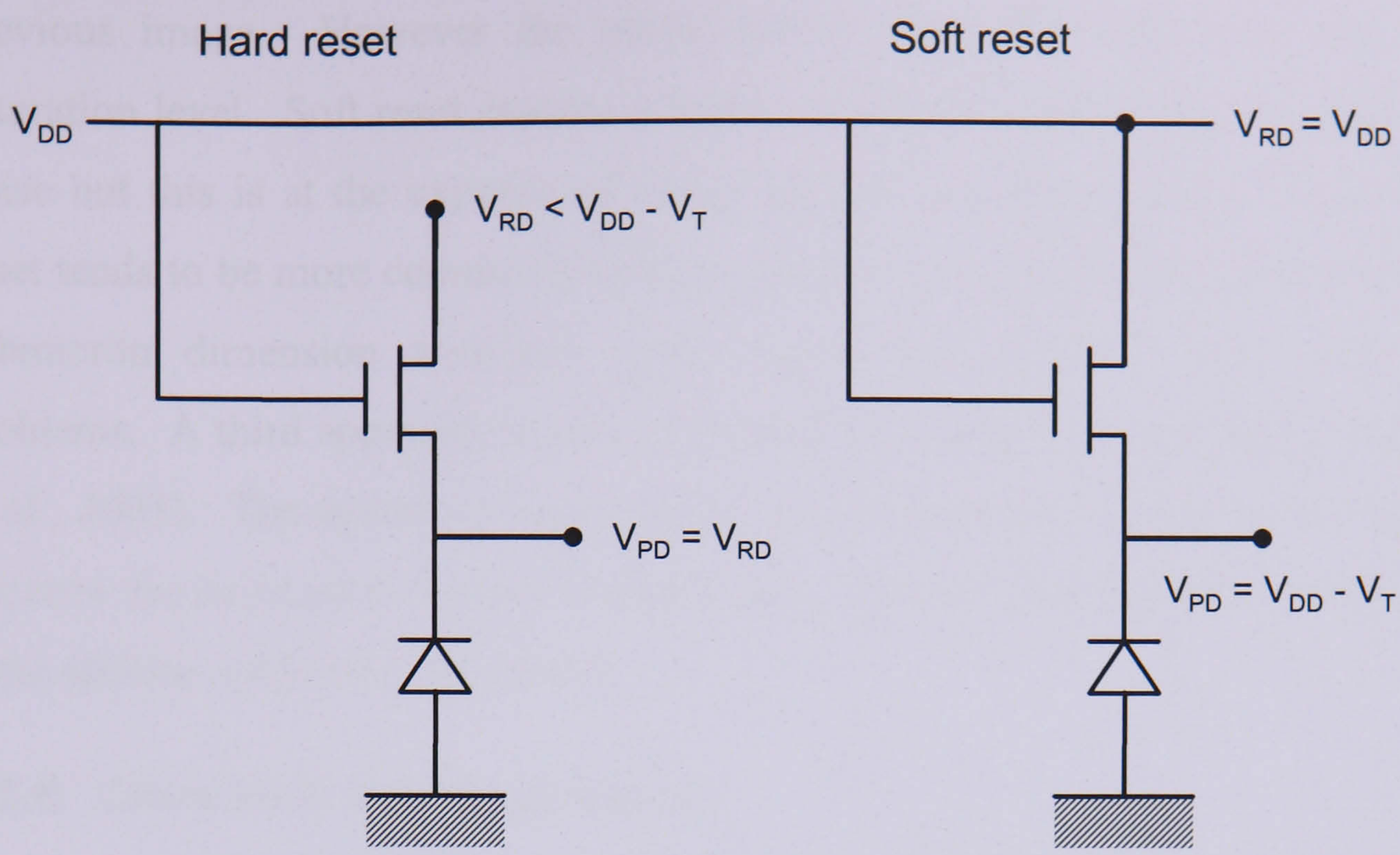


Figure 3.17 Hard reset (left) and soft reset (right) of the photodiode in a CMOS pixel. Hard reset occurs when the diode is reset to a voltage less than $V_{DD} - V_T$. Soft reset occurs when the reset level is connected to V_{DD}

Equations 3.28 and 3.29 only hold true if the reset level is less than the supply voltage by at least the threshold voltage of the reset transistor. This is known as hard reset. **Figure 3.17** illustrates the two possible approaches to resetting the photodiode in a CMOS pixel. During hard reset operation, the reset transistor acts as a low resistance switch, and the voltage on the photodiode will be charged to a level equal to the drain voltage V_{RD}. It is more common to reset the pixel to the supply level V_{DD}, to minimise connections to the device and maximise available voltage swing. This mode of operation is known as soft reset. Under soft reset the photodiode does not reset to a fixed reference level, instead it approaches it asymptotically. The pixel never reaches thermal equilibrium and charges logarithmically beyond V_{DD}-V_T. The voltage on the photodiode will slowly increase past this point as a result of sub-threshold conduction in the reset transistor. The benefit of the soft reset approach is that the noise is less than the value given by Equations 3.28 and 3.29 (Tian et al., 1999). Tian et al's analysis assumes that the time to reset the pixel does not allow the photodiode reset to reach a steady state and the reset noise is approximately half the value given for hard reset.

Each mode of operation has its benefits and drawbacks. Hard reset results in good linearity and no image lag due to residual signal remaining in the pixel from the

previous image. However the mode suffers from full kTC noise and decreased saturation level. Soft reset enables a higher saturation level within the pixel and lower noise but this is at the expense of image lag and low illumination non-linearity. Soft reset tends to be more commonly used in commercial CMOS imagers as overdriving of submicron dimension transistor gates can cause electrical stress and reliability problems. A third approach known as flushed reset, has been developed recently (Pain et al., 2003). The technique uses a hard reset immediately followed by a soft reset to improve the noise performance characteristics. The method requires a small amount of extra address circuitry in the device

3.5.6. Correlated double sampling

It is possible to remove reset noise using a technique known as correlated double sampling (CDS). The principle is illustrated in **Figure 3.18**. In CDS the reset level of the sense node is sampled before signal charge is transferred to it (White et al., 1973). Charge is then transferred giving the signal level. The two levels are then subtracted and as the noise fluctuation remains the same on the reset and signal levels, the noise source is cancelled. Care must be taken that the two samples are made closely in time, otherwise the noise sources may be uncorrelated resulting in a degradation of the noise performance. Correlated double sampling requires a pixel whereby the sense node capacitance is isolated from the photodiode capacitance. In the 3T pixel the photodiode is permanently connected to the sense node and the capacitance is shared so CDS is not possible. More advanced active pixel designs incorporate CCD like charge coupling to enable sampling of the reset level before the output level. Two such designs are the photo-gate and pinned photodiode pixel, and are described in Section 3.6: Other active pixel architectures.

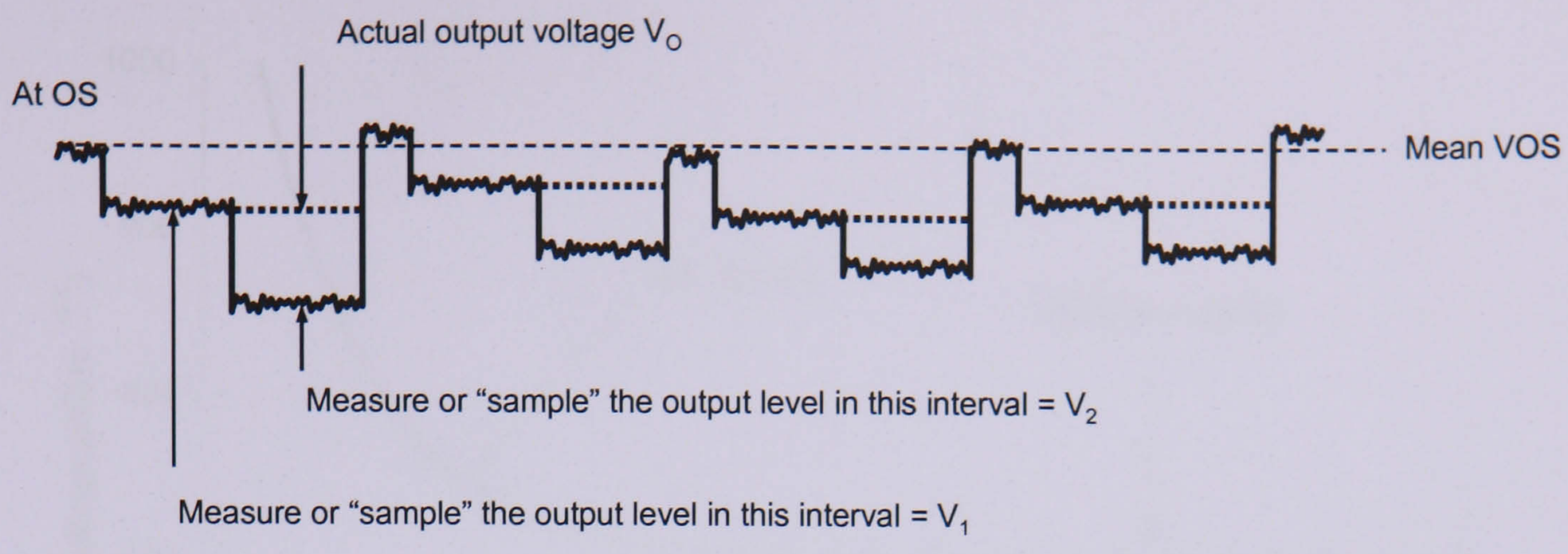


Figure 3.18 Correlated double sampling. The sense node is reset and the reference level sampled before charge is transferred. The output level is then sampled and subtracted from the reset value which cancels the noise associated with both levels

3.5.7. 1/f noise and random telegraph signals

1/f noise is additional low frequency noise associated with MOS transistors (Hung et al., 1990, Chang et al., 1994). The noise power (proportional to the voltage squared) is inversely proportional to the measurement frequency and also inversely proportional to W.L. Increasing the size of the transistor can thus reduce the magnitude, but this is at the expense of higher gate capacitance. 1/f noise is caused by numerous traps in the channel of the transistor capturing and releasing free carriers passing between the drain and the source. This causes the voltage across the device to fluctuate. The noise is also highly process dependent. As the dimensions of the transistor are reduced the number of traps reduces and the most extreme case is where there is one single trap within the channel. This results in the noise voltage switching between two levels as electrons are captured and released. This situation is known as Random Telegraph Signal (RTS) noise and as CMOS feature and pixel sizes reduce, the effect is becoming increasingly significant (Janesick et al., 2006). If CDS is used to eliminate reset level fluctuations, the noise floor of the sensor will typically be set by the 1/f or RTS noise performance of the in-pixel follower transistor. The CDS processing can also suppress the 1/f noise sources if the samples are closely spaced in time. The combination of 1/f noise and white noise is illustrated in **Figure 3.19**.

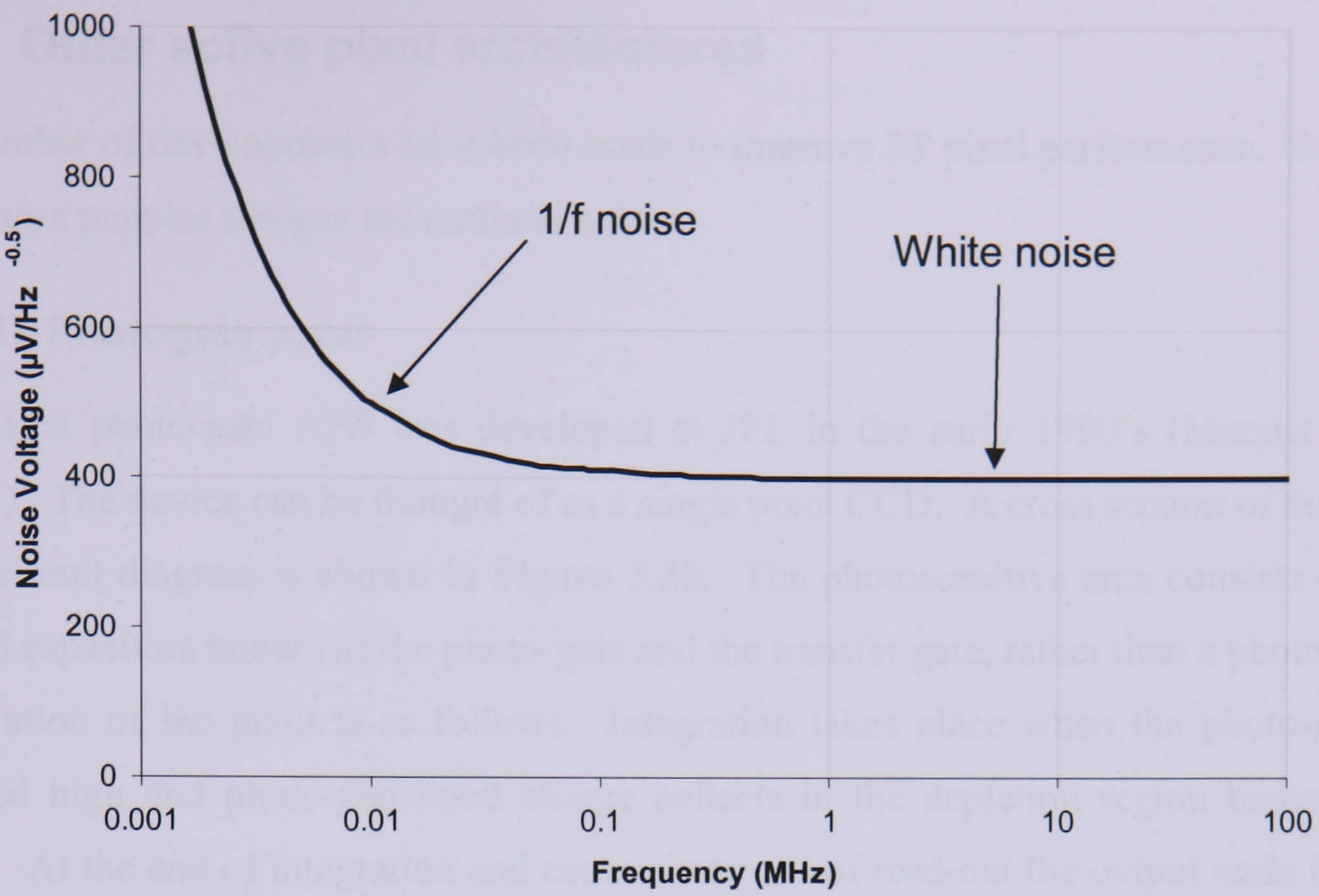


Figure 3.19 Thermal and 1/f noise sources in an MOS transistor. At low frequencies the noise is dominated by the 1/f source and at higher frequencies the noise is frequency independent giving the classical white noise performance

3.5.8. Fixed pattern noise

A further source of image degradation in CMOS pixels is fixed pattern noise (FPN). FPN can be any noise source that varies with a spatial nature. As mentioned earlier, a major source of fixed pattern noise in active pixel sensors is the offset and gain FPN due to the fact that each pixel and column has its own read-out circuit. Small variations in the fabrication process mean that each follower circuit will have a different DC offset and gain characteristics. Other contributors to fixed pattern noise include photo response non-uniformity (PRNU) and dark signal non-uniformity (DSNU) which are determined by the pixel design and the continuity of the fabrication process. There have been more recent attempts to reduce fixed pattern noise sources using special readout techniques (Miyatake et al., 2003), but the best way to reduce the FPN is to improve the uniformity of the manufacturing process.

3.6. Other active pixel architectures

A number of developments have been made to improve 3T pixel performance. Some of the more popular designs are outlined below.

3.6.1. Photogate pixel

The first photo-gate APS was developed at JPL in the early 1990's (Mendis et al., 1994). The device can be thought of as a single pixel CCD. A cross section of the pixel and circuit diagram is shown in **Figure 3.20**. The photosensitive area consists of two MOS capacitors known as the photo-gate and the transfer gate, rather than a photodiode. Operation of the pixel is as follows. Integration takes place when the photo-gate is pulsed high and photo-generated charge collects in the depletion region beneath the gate. At the end of integration and commencement of read-out the output node is reset and the value on the node is sampled. The photo-gate is then pulsed low and charge is transferred through the transfer gate to the sense node. The value on the node is then sampled giving a pixel output. True pixel rate CDS is therefore possible, thus eliminating kTC noise from the reset transistor. The photo-gate is then pulsed high again for the next integration. The transfer gate voltage remains at a fixed level throughout the operation.

The photo-gate pixel requires overlying polysilicon gates (like a CCD structure) for efficient charge transfer. This requires two layers of active polysilicon, which is not always available in the CMOS manufacturing process. If two active layers are not available then a link has to be made with an intermediate diffused node and charge transfer problems can occur, causing image lag effects. The charge capacity of the pixel can be quite high as the storage density of a gate is generally higher than that of a diode. Also the pixel has a more linear response than the 3T pixel because the sense node is decoupled from the photo-gate.

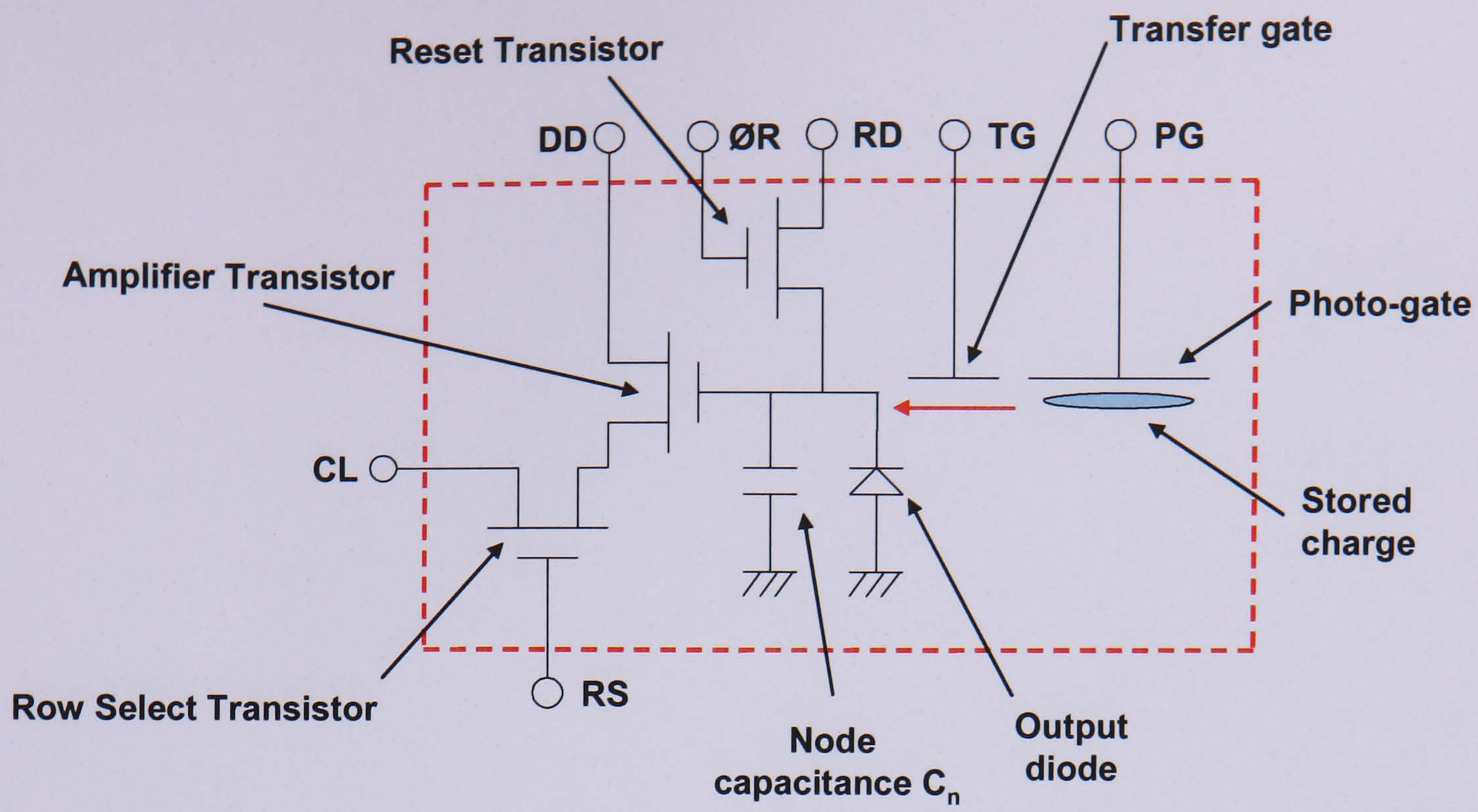


Figure 3.20 Photo-gate pixel schematic. Signal charge is stored in the depletion region underneath the photo-gate. The node is reset and sampled before the charge packet is transferred by pulsing the photo-gate low. The signal is subtracted from the reset level giving the video level and eliminating reset noise

The major disadvantage of the photo-gate structure is a degradation of quantum efficiency (from ~ 50% to 20 % peak QE) compared with the 3T design (Blanksby et al., 1997, Blanksby and Loinaz, 2000). This is due to absorption of light by the extra polysilicon gates on the photosensitive area of the pixel. QE is reduced particularly at blue and UV wavelengths as the polysilicon is strongly absorbing this part of the spectrum. This problem could potentially be eliminated if the device were back thinned and illuminated from the reverse side.

3.6.2. Pinned photodiode pixel

The pinned photodiode pixel improves on the photo-gate design with much higher QE and a much lower dark signal, together with CDS operation. It is therefore a strong candidate for scientific imaging. The first successful implementation was by way of collaboration between Kodak and Motorola in 1997 (Guidash et al., 1997), and examples were also reported by Toshiba (Inoue et al., 1999) and Hyundai. The structure is also referred to as a buried photodiode, or a hole accumulation diode (HAD) in the literature. It builds on the principle of the buried channel CCD (Teranishi, et al 1982, Burkey et al., 1984). A cross section of the device is shown in **Figure 3.21**.

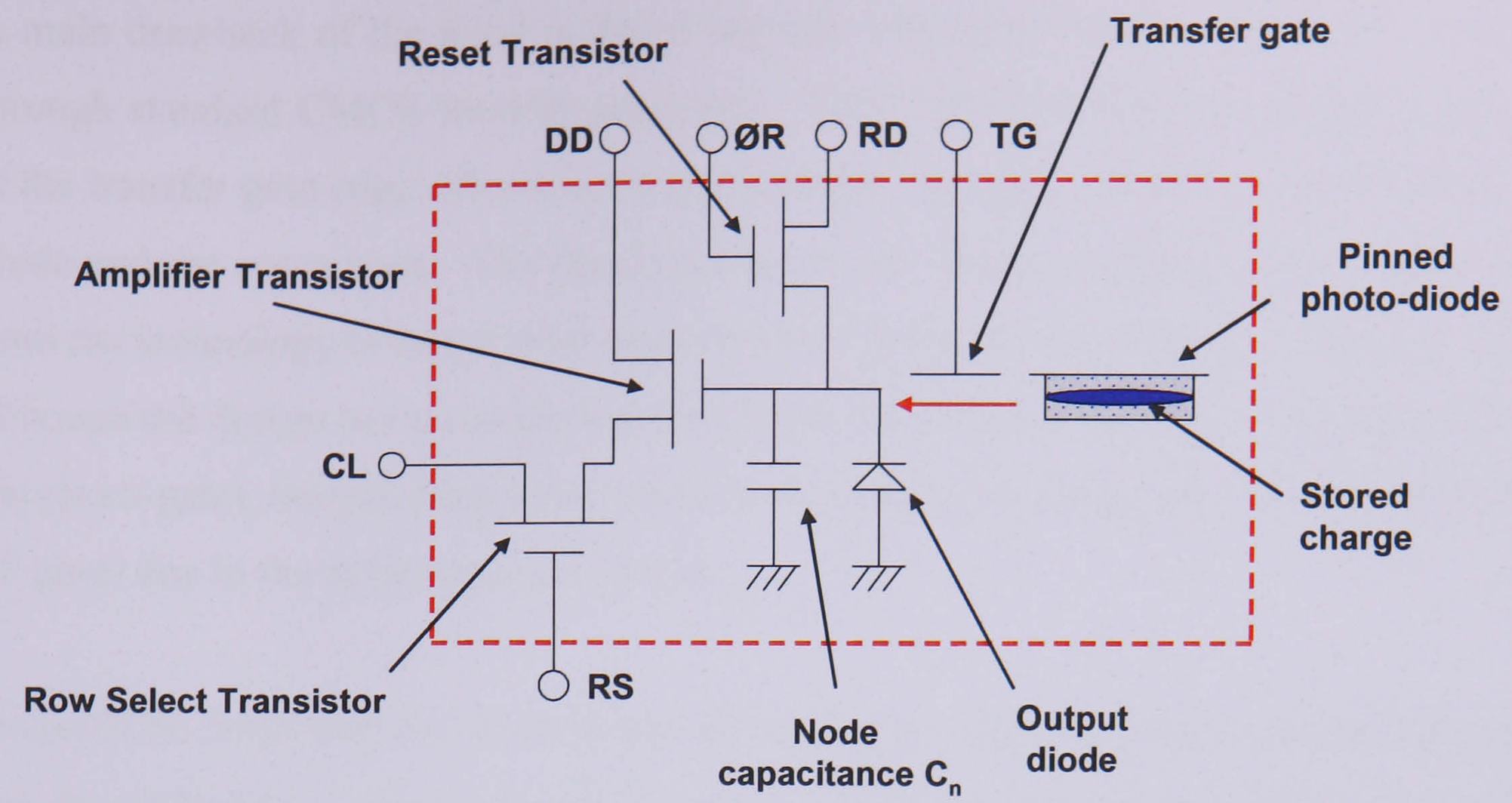


Figure 3.21 Pinned photodiode pixel operation. Signal charge is stored in the depletion region underneath the pinned diode region. The node is reset and sampled before the charge packet is transferred to it by pulsing the transfer gate high. The signal is subtracted from the reset level giving the video level and eliminating reset noise

The architecture has two additional features compared with the standard 3T pixel. Firstly, the signal charge is generated and collected in a "pinned" diode region that is at a fixed potential. This pinned region is created by adding an extra p+ type implant at the surface. The presence of the pinning implant has the effect of suppressing the surface component of dark current generation, as any electrons generated immediately recombine with a hole. This can have the effect of reducing the dark current by a factor of 100-1000 (e.g. from 1 nA/cm^2 to 1 pA/cm^2) compared with the normal n+ implant used in the 3T pixel. In addition to the pinning implant, the photodiode region is isolated from the sense node and the three readout transistors by a transfer gate. Therefore as with the photo-gate pixel, true CDS can be used to eliminate kTC noise due to the reset transistor. When the transfer gate is clocked high, all the charge collected in the pinned region is transferred to the sense node. As there is no charge left in the diode after transfer, there can be no variation in a charge level and therefore no kTC noise. This also means the pixel does not suffer from the usual image lag problems and it can have a linear response due to the sense node being isolated from the photodiode.

A main drawback of the pixel is that it requires two specialised implants not available through standard CMOS foundry processes. These implants must be precisely aligned at the transfer gate edge otherwise charge transfer (or lag) problems occur between the diode and the sense node. The pixel also has a low charge storage capacity, which can limit the technology to larger pixel applications if large dynamic range is required. Also, although the design has no overlying features on the photosensitive area (compared with the photo-gate), the pixel has a somewhat lower fill-factor compared with the equivalent 3T pixel due to the extra transistor present.

It should be noted that the fundamental difference between the pinned photodiode pixel and the photogate is that the potential well is created by the presence of the p+ implant. This implant enables low dark signal and complete charge transfer from the collection region to the node, without an overlying gate structure degrading the QE. It is for these reasons that the pinned photodiode rather than the photogate has been adopted for many consumer applications.

3.6.3. Logarithmic pixel

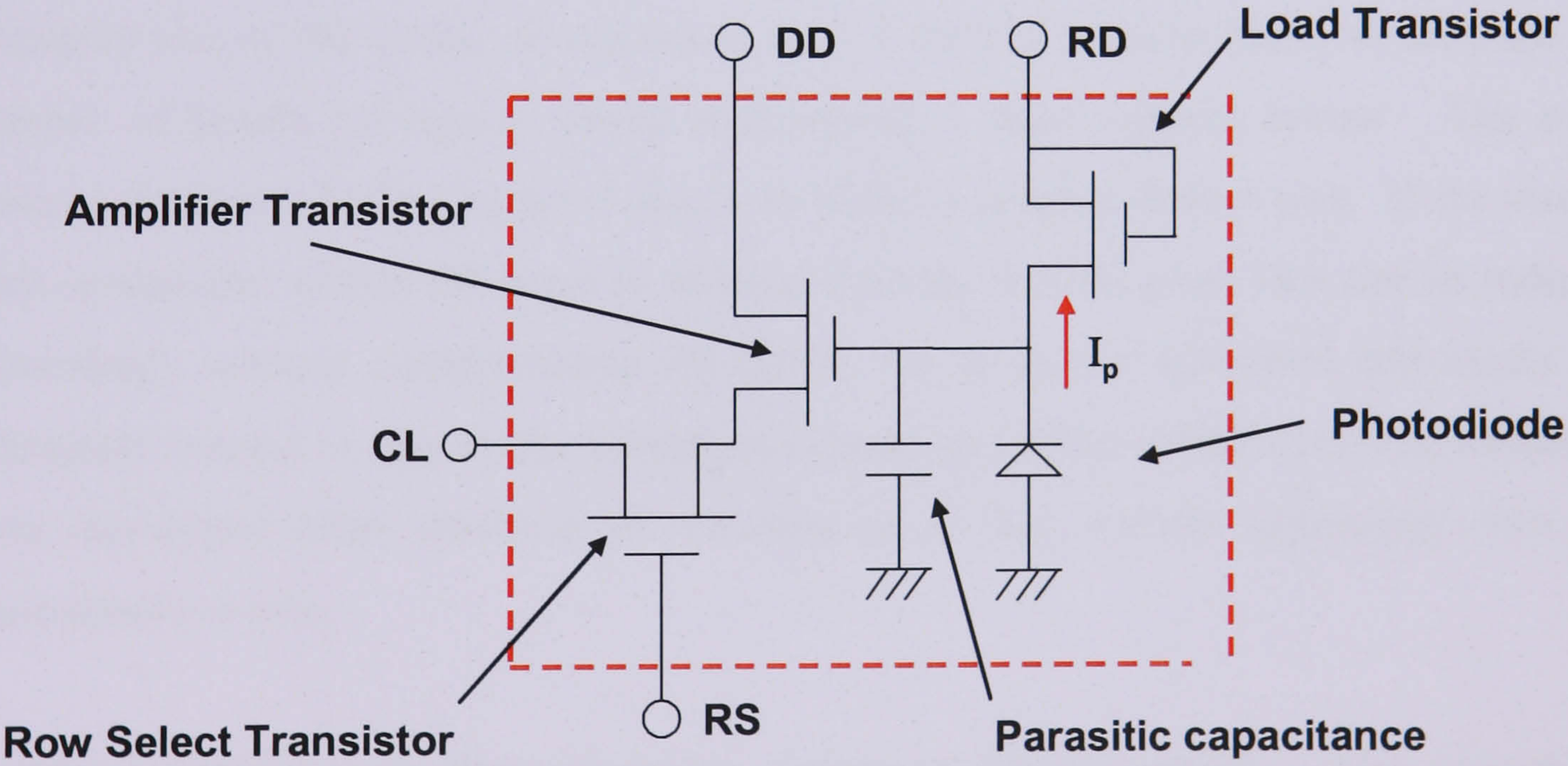


Figure 3.22 The logarithmic pixel. The gate of the rest transistor is tied to the reset level therefore the voltage level at the output is regulated by the instantaneous photocurrent

A less conventional approach to CMOS pixel design is the logarithmic pixel (Ricquier and Dierickx, 1992) shown in **Figure 3.22**. In this design the gate of the reset transistor is tied to the reset drain voltage to create a load device. The pixel therefore does not

operate in an integrating mode, instead the output voltage is related to the photo-current from the diode which flows through the load transistor. The load transistor operates in the sub threshold regime and the voltage across it is given by:

$$V \approx \frac{2.3kT}{q} \log_{10} \frac{I_p}{I_0} \tag{3.30}$$

Where I_0 is a constant and 2.3kT/q is approximately 60 mV. The signal voltage is therefore proportional to the logarithm of the photocurrent and the signal range can span six orders of magnitude or more. The pixel is also well suited to random access as the signal does not depend on integration time. The disadvantages of the approach are that no form of CDS is possible, and also any fixed pattern noise due to the transistors will result in a large variation in the equivalent signal from pixel to pixel. The response time of the pixel can also be very slow because the pixel capacitance is being charged only by the very small photo-current.

3.6.4. Shared transistor pixels

There has been a move towards smaller (< 5 μm) pixels in CMOS imaging. This is primarily due to the desire of consumer digital camera manufacturers to increase the number of pixels per sensor whilst maintaining a small optical format. The most obvious method of reducing pixel size is to utilize a smaller feature size. If the size of each component within the pixel is reduced then the overall pixel size can be reduced accordingly without compromising fill factor. As the pixels described previously are ultimately limited in size by the minimum feature size of the CMOS process, designers have developed other methods of reducing pixel size without impinging onto the photosensitive area.

A new approach is to share transistor functions between pixels. The concept is illustrated in **Figure 3.23**. Researchers at Matsushita (Mori et al., 2004) have developed a 1.75 transistors per pixel sensor with 2.25 × 2.25 μm^2 pixels. This device has a 4T pinned diode configuration but each pixel shares the floating diffusion, reset transistor, follower transistor and select transistor. A group of four pixels requires seven transistors in total therefore there are 1.75 transistors per pixel. This approach eliminates the problem of reduced fill factor in the original pinned diode pixel. The

sharing of transistors requires a special read-out technique. This methodology has been developed further by researchers at Canon (Takahashi et al., 2004) by also removing the row select transistor altogether to produce a 1.5 transistor per pixel device. The design uses the reset transistor to address the pixel, eliminating the need for the shared row select transistor. The shared pixel structure is only possible with a more complex method of read-out compared with the 3T pixel, which can only be performed with charge transfer pixels such as the pinned diode and photo-gate designs. The shared pixel architecture also has a lower responsivity as the pixel has a larger capacitance due to the sharing of the sense node between pixels and it also suffers from increased fixed pattern noise (Theuwissen, 2007).

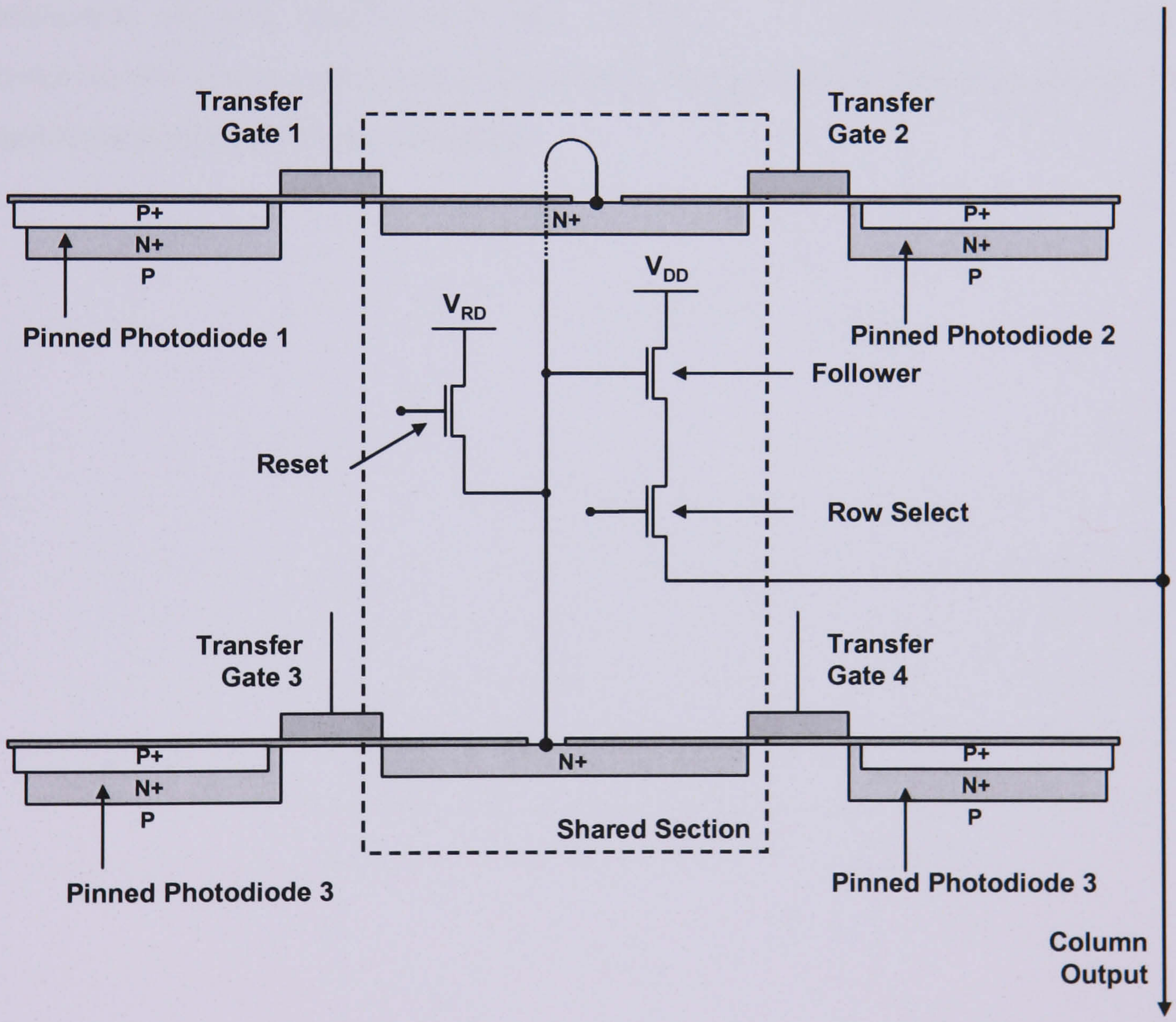


Figure 3.23 The shared transistor pixel. The conventional 3T readout circuit is shared between four adjacent pixels reducing the number of components per pixel enabling smaller pixels for a given feature size.

3.7. Summary

Chapter 3 has provided a more detailed description of the components that are used to form an active pixel sensor. The chapter described the operation of the p-n junction and the MOS capacitor and explained how the two structures were used to form the photodiode and the MOS transistor and how these more complex devices are further combined to form the three transistor plus photodiode pixel (3T) pixel. A detailed description of the operation of the pixel was given including the range of noise sources and performance parameters used to characterise image sensor behaviour. The next chapter describes the CMOS manufacturing process and explains how it is utilised to produce the three transistor active pixel. The TS50 CMOS process, selected to manufacture the Test Structures, is also described. The remainder of the chapter focuses on the issues considered in the sensor design process including the electrical simulations performed by the designers.

Chapter 4: Device design and pixel modelling

Chapter 4 begins with a description of mainstream CMOS manufacturing processes and explains how they are utilised to produce the three transistor active pixel. The TS50 CMOS process, selected to manufacture the Test Structures, is also described. The remainder of the chapter focuses on the electrical simulations performed as part of the design process.

4.1. Introduction

The significant developments in CMOS manufacturing technology over the last forty years have recently enabled the realisation of active pixel sensors. Since 1965 the number of transistors on a given silicon wafer has increased at a rapid rate according to the famous predictions made by Gordon Moore of Intel (Moore, 1965). The minimum transistor dimensions have now become small enough to allow the creation of an imaging device with active transistor circuitry within the photosensitive area of the device. CMOS technology was not originally intended to manufacture image sensors therefore the processes are in general not optimised for the purpose.

The first section of Chapter 4 discusses the methods used to manufacture complementary MOS transistors for high speed integrated circuits and explains the considerations which must be taken into account when producing a an imaging device using a modern twin-well CMOS manufacturing process. The second half of Chapter 4 considers the Test Structure design process. This includes a description of the TS50 0.5 μm, 5V process, selected to manufacture the Test Structures and also outlines the electrical simulations performed by the designers using the SPICE (Simulation Program with Integrated Circuit Emphasis) software.

4.2. CMOS active pixel fabrication

Before complementary MOS manufacturing existed, there were nMOS and pMOS fabrication processes (Glasser and Dopperbuhl, 1985). An nMOS process consists of only n-channel transistors implemented on a p-type substrate and a pMOS process consists of p-channel transistors implemented on an n-type substrate. The disadvantage of these approaches is that when they are used to create logic circuits they dissipate large amounts of power under static conditions and operation is susceptible to noise

sources (Rabaey et al., 2003). To counteract this problem a complementary MOS process was developed whereby n- and p-channel transistors could be implemented on the same substrate (Wanlass, 1963). The main advantage of the CMOS approach is that the static power consumption is dramatically reduced, by as much as six orders of magnitude compared with uni-polar MOS processes, and it is also much simpler to produce the types of logic circuits such as the inverter, NAND or NOR gates which are the building blocks of all digital integrated circuits.

4.2.1. Basic CMOS processes

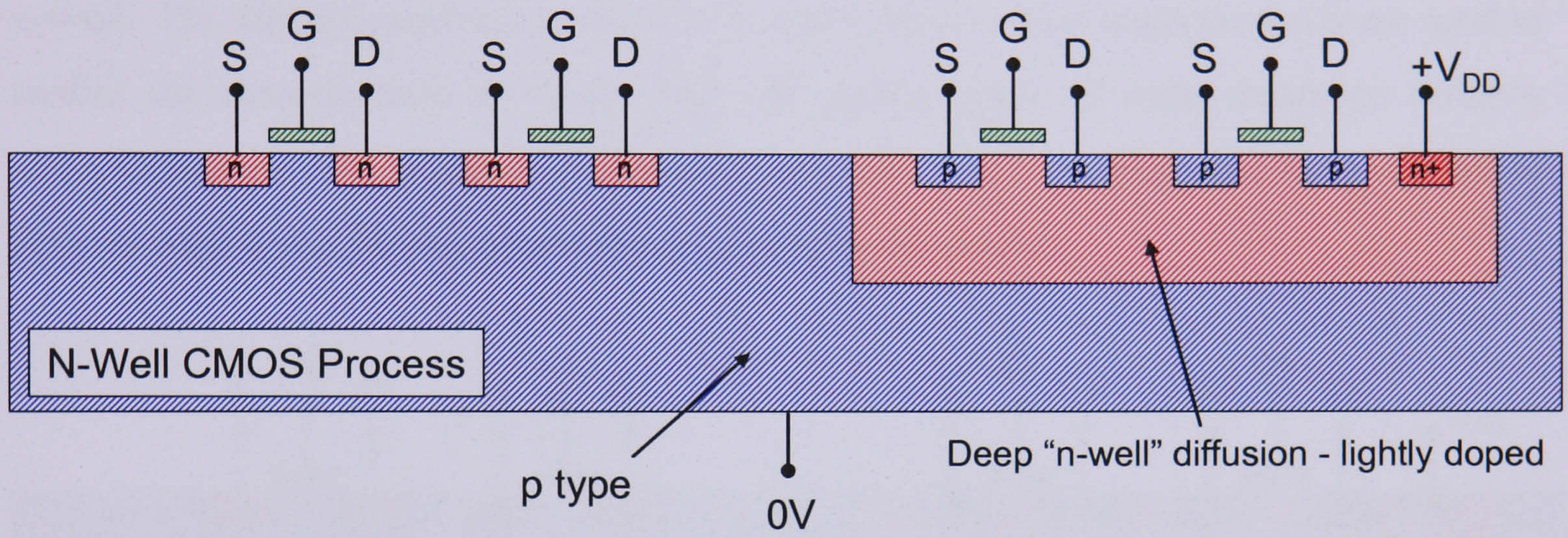


Figure 4.1 n- and p-well CMOS process cross sections (S = Source, G = Gate, D = Drain)

The underlying principle of CMOS processing is to form a small region or “well” of one doping type on the wafer of the opposite doping type, and then manufacture transistors of the opposite polarity within this well. It is therefore possible to form complementary pairs of transistors within the same substrate. There are three fundamental types of CMOS processing: n-well, p-well and twin-well. The n-well process is shown in **Figure 4.1**. It consists of n-channel transistors on a p-type substrate and p-channel

transistors sitting in an n-type well. There is an extra connection to the n-well to bias it to a positive voltage ($+V_{DD}$). The p-well CMOS process is also shown in **Figure 4.1**. The process consists of p-channel transistors on an n-type substrate and n-channel transistors sitting in a p-type well. There is an extra connection to the p-well to bias it to a negative or zero voltage.

4.2.2. Twin-well process and fabrication

The more advanced twin-well process is shown in **Figure 4.2**. The process uses n-channel transistors in a lightly doped p-well and p-channel transistors in a lightly doped n-well. The starting material can be n- or p-type silicon. Two separate wells are used to enable the manufacturer to finely tune the performance of each transistor polarity independently of the other. The twin-well process is the most popular kind of CMOS process used today for the manufacture of integrated circuits.

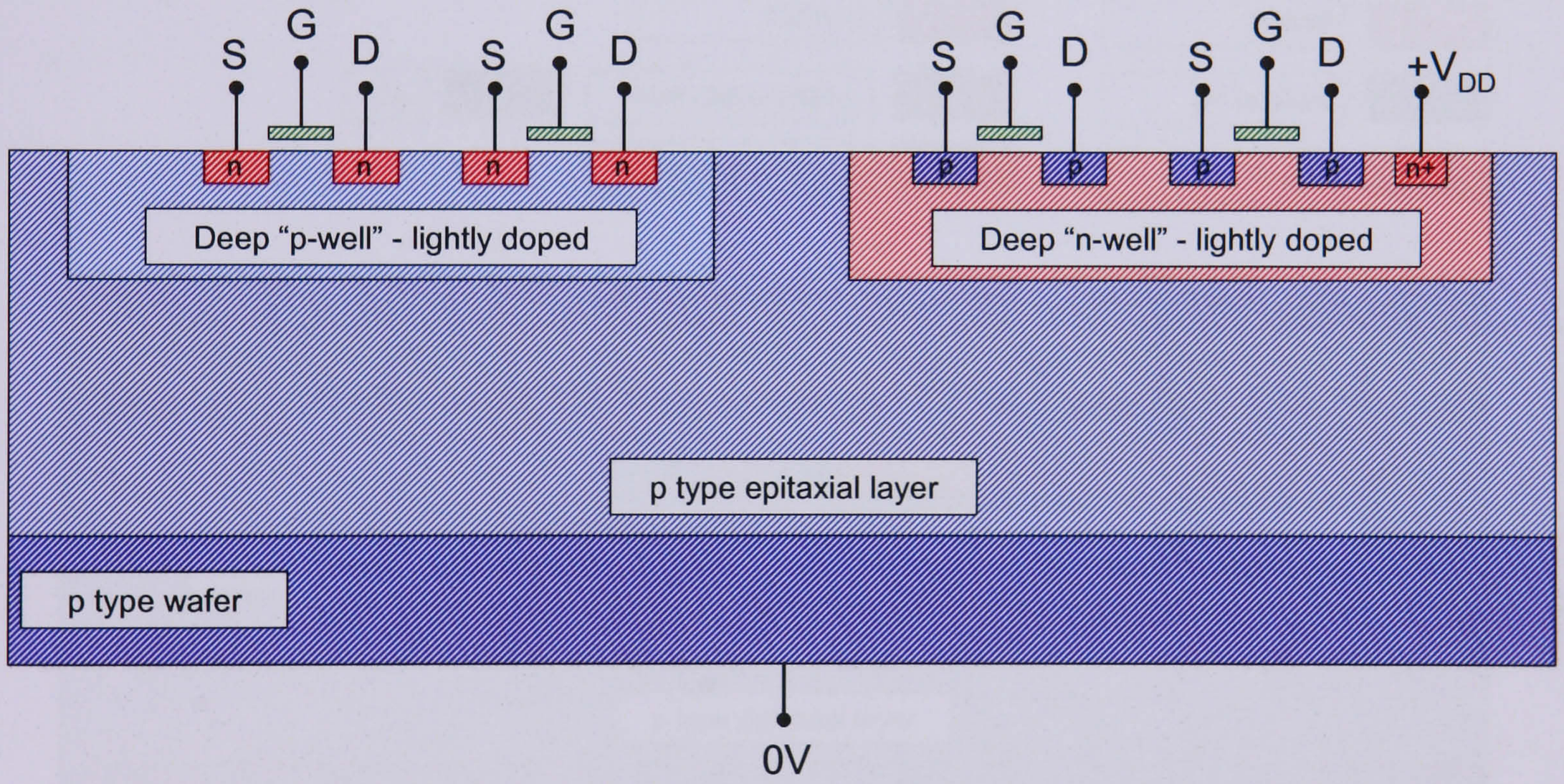


Figure 4.2 Twin-well CMOS process cross section (S = Source, G = Gate, D = Drain)

Note that it is usual for the silicon wafers to be of "epitaxial" format, somewhat similar to a chocolate digestive biscuit. The biscuit is silicon of high doping concentration, often referred to as the substrate, and the chocolate is a thin "epitaxial layer" of silicon having the lower doping concentration required for the active elements of the device. The advantage of this approach is that the substrate provides a low resistivity ground plane beneath the active components.

A more detailed cross section of a twin-well CMOS process manufactured on a p-type wafer is shown in **Figure 4.3**. The first stage of manufacture is to grow a layer of high quality silicon dioxide (SiO_2) by placing the wafer in an oxidation furnace. This layer is known as a stress relief oxide or buffer layer. The next step is to define the n-well region. This is done by spinning on a layer of photo-resist and exposing to a mask that defines the n-well active area. The n-well is then created using an ion implantation or diffusion. This step is repeated to form the p-well region. The next stage is to then deposit a thin layer of silicon nitride (Si_3N_4). If the buffer layer were not used the Si_3N_4 would cause surface state problems in the device.

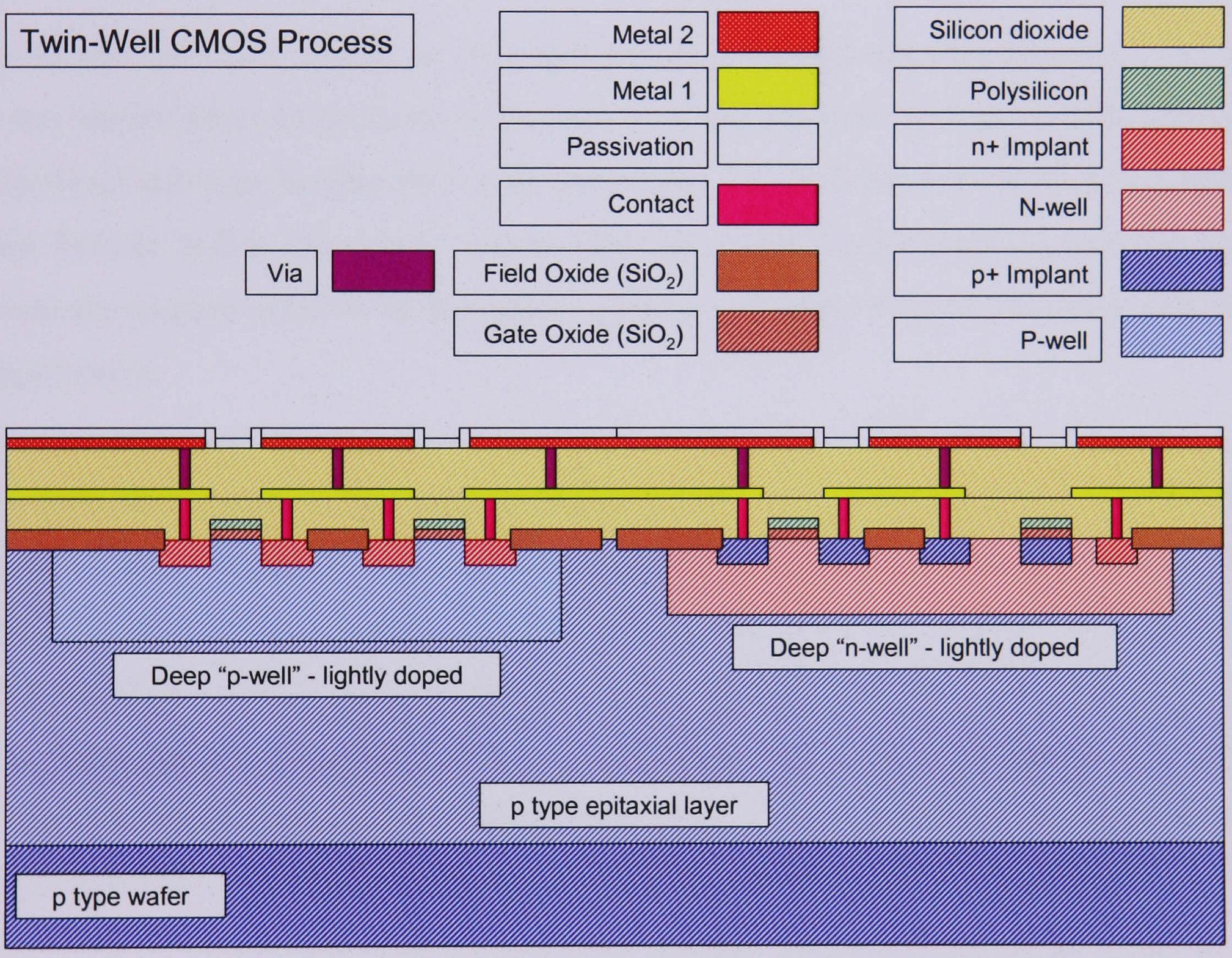


Figure 4.3 Single poly, double metal (1P2M), twin-well CMOS process cross section

The next step is to use another stage of photo-resist to pattern the silicon nitride and grow a thick "field oxide" to isolate adjacent transistors. The technique is known as localised oxidation of silicon (LOCOS). The resulting efficient isolation enables the creation of a high density of transistors without parasitic transistors being created. A

more recently developed technique to isolate adjacent transistors is the box isolation technique also known as shallow trench isolation (STI). In this method a hole is etched into the surface of the silicon wafer and then filled in with silicon dioxide.

The next step is to grow the thin gate oxide for the transistors. The doping of the n- and p-wells is then adjusted by extra ion implantation steps. This adjustment is made to tune the threshold voltages of the n- and pMOS transistors to the required values. Next a chemical vapour deposition process (CVD) is used to deposit a layer of polysilicon to form the transistor gate. The polysilicon is patterned with the use of a special photo-resist mask.

The source and drain regions of the n and pMOS transistors are then formed by n+ and p+ ion implantation using photo-resist masks. These implants are also used to dope the polysilicon and significantly reduce its resistivity. The fact that the polysilicon gate has been formed before this stage ensures that the n+/p+ source/drain regions are very accurately aligned relative to the gate. This is very important to minimise parasitic capacitances.

The penultimate step of the manufacturing process is to form the metal interconnect layers to make the appropriate conduction paths/connections between components. An insulating layer of SiO_2 is deposited onto the surface. Contact holes to the polysilicon gates and n+/p+ source/drain regions are then etched through the SiO_2. Aluminium is then deposited on the surface using a sputtering technique to create a connection between the surface and the metal layer known as a contact. The metal is patterned onto the surface with a metal masking technique and unwanted metal is etched away.

These steps can be repeated to construct multiple layers of metal and insulating SiO_2 to fabricate all the required connections of a complex integrated circuit. Adjacent layers are connected using a hole between two layers which is filled with a metal such as tungsten and known as a 'via'. It is important to note that as each subsequent layer is built up it is necessary to continuously planarise the surface before beginning the new layer. If this is not done then the new layer will not form properly. The planarisation is performed using a technique called chemical mechanical polishing (CMP). When all layers have been produced, the final step is to passivate the top surface of the structure

by chemical vapour deposition of SiO_2 or with a nitride coating. Etching through to the bonding pads to enable connection of the bond wires completes the structure.

4.2.3. Device technology scaling

The need for integrated circuits with a higher density of transistors and a faster speed of operation to realise devices such as microprocessors and memories has driven the ongoing reduction in CMOS feature sizes. The increase in the density of CMOS circuits has lead to reductions in four key process parameters:

- Minimum feature size
- Junction depth
- Gate oxide thickness
- Supply voltage V_{DD}

The effects of these developments on the characteristics of CMOS APS were investigated in the mid 1990's by researchers at IBM (Wong, 1996). The advancements made in CMOS manufacturing have a range of benefits when considering the production of active pixel sensors. The obvious advantage of the reduction in minimum feature size is that using smaller transistors can reduce the area within the pixel that is required for the active circuitry. Therefore, for a given pixel area, the proportion of photo-sensitive area or fill factor can be increased, or the actual pixel area can be reduced without sacrificing fill factor. A further benefit of using the more advanced processes is that the threshold voltages are more uniform, thereby reducing the variation from pixel to pixel, so the fixed pattern noise due to source-follower DC offset variations is minimised. The reduction in feature size can also be used to reduce parasitic capacitances, and this has the benefit of increasing the responsivity of the pixel and reducing reset noise.

Unfortunately the reduction in the above parameters has some major negative effects on the performance of active pixel sensors. The increased circuit density can require a larger number of metal interconnects between devices, for which a larger number of metal layers are necessary. This increases the depth of the overlying layers on the pixel (as illustrated in **Figure 4.3**) and produces a more complex optical path for incident light to navigate before entering the photodiode. Some attempts have been made to reduce the thickness of each metal layer by using copper interconnects. This effect on

QE and pixel to pixel cross-talk is discussed in more detail in Chapter 8. The shallower junction depths used result in a much shallower photodiode depletion depth. This degrades the quantum efficiency for longer wavelengths, which are absorbed deeper in the silicon. The shallower junction depth and the thinner gate oxides also tend to increase leakage current levels due to increased electric field strength. The use of shallow trench isolation as opposed to LOCOS also introduces increased mechanical stress into the wafer, which can further increase the overall leakage current. Finally, the lower supply voltages used decrease the overall voltage swing available to collect generated signal and thus the saturation level, although to a certain extent this is countered by the reduction in threshold voltage with the more advanced processes. The overall effect is to degrade the dynamic range of the sensor.

4.2.4. 3T pixel fabrication

A cross section of a typical 3T pixel manufactured using a standard CMOS process is shown in **Figure 4.4** and a plan view of the layout is shown in **Figure 4.5**. The design requires a minimum of one layer of polysilicon and two layers of metal (1P2M). The pixel requires five metal connections between each pixel cell. These are the two bias lines V_{DD} and V_{RD}, the column line and the two clock lines ØRS and ØR. The V_{RD} connection from pixel to pixel can be eliminated by connecting the drain of the reset transistor to V_{DD} but this will limit the pixel to a soft reset mode of operation. There is also scope for eliminating the separate ØRS connection by taking the ØR clock line from the row above or below and using the same clock to reset the adjacent row. This means the pixel will have a raster scan style reset and a global reset to all pixels simultaneously will not be possible.

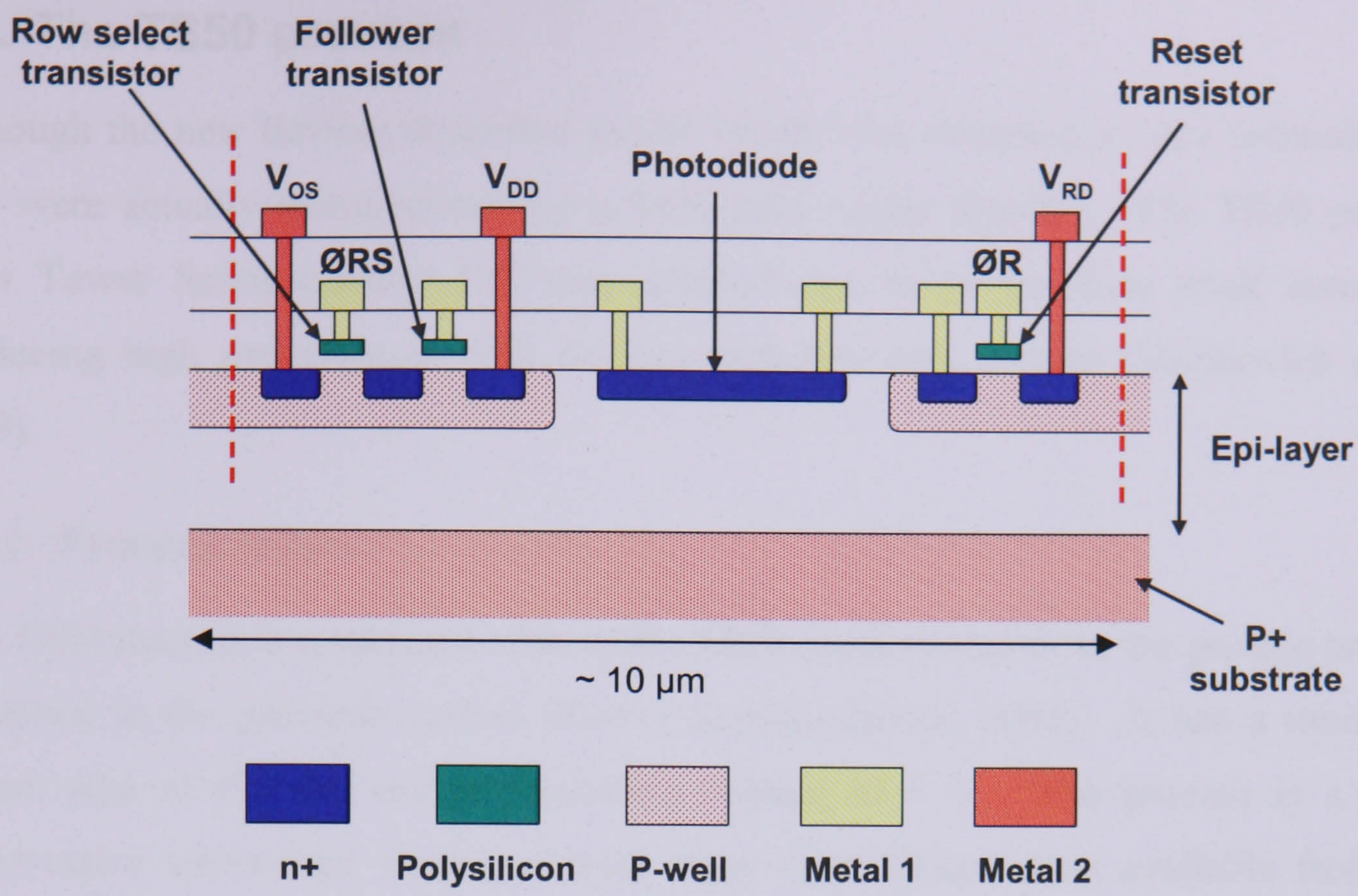


Figure 4.4 3T photodiode pixel cross section

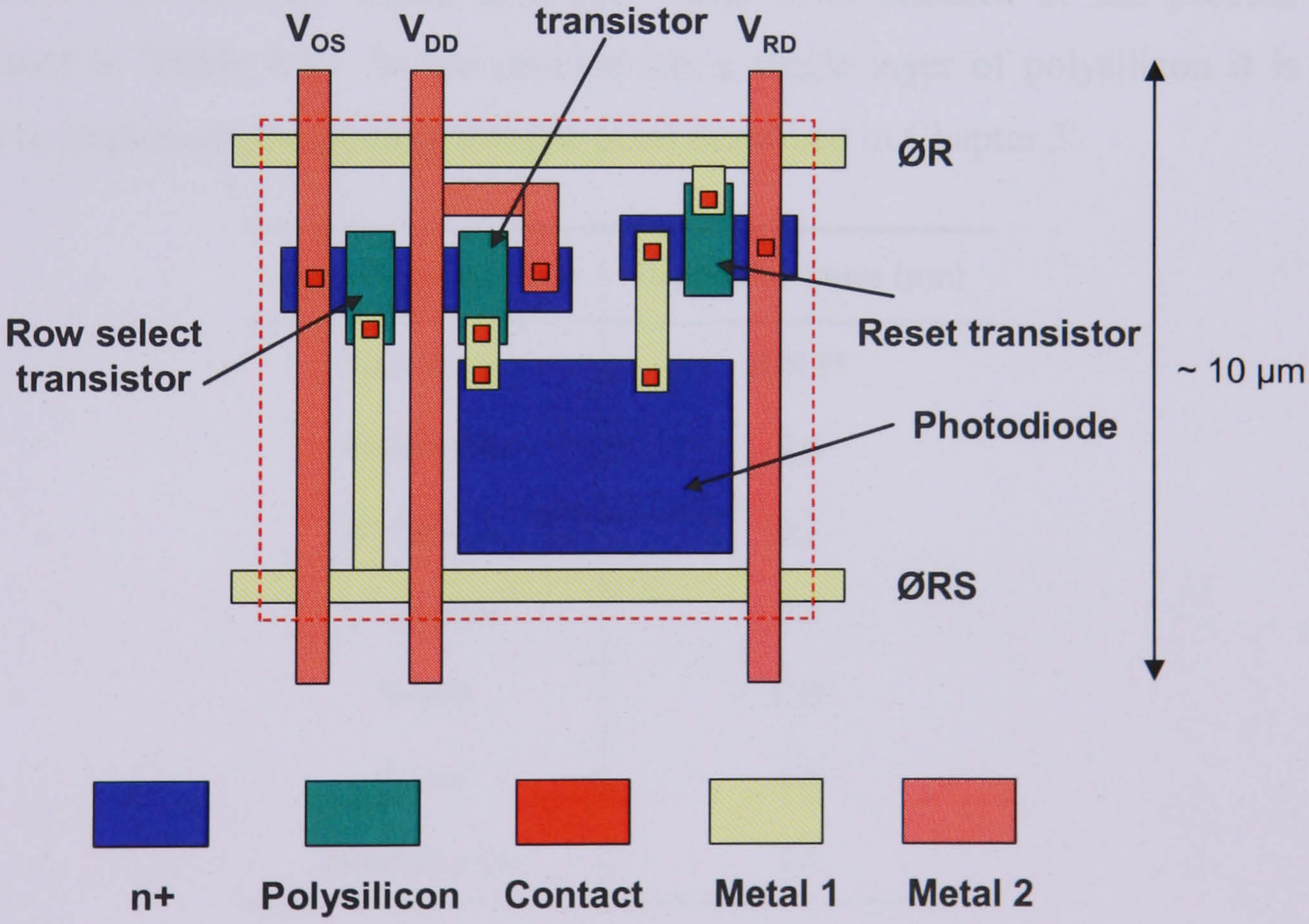


Figure 4.5 Plan view of a typical 3T pixel layout. A minimum of one layer of polysilicon and two layers of metal are required to make the necessary connections

4.3. The TS50 process

Although the new devices described in this thesis were designed by e2v technologies, they were actually manufactured by a third party wafer foundry. The TS50 process from Tower Semiconductor Ltd was selected due to its previous track record of producing high performance APS devices with low dark current (Malinovich et al., 1999).

4.3.1. Process layers

The TS50 process is a standard twin-well CMOS process similar to the generic process described in the previous section (Tower Semiconductor, 2007). It has a minimum feature size of 0.5 μm and an operating voltage of 5 V. The process is a more conservative technology compared with other finer feature sizes available from the same manufacturer. It uses LOCOS isolation as opposed to the more recently developed shallow trench isolation and has two layers of metal interconnect and one layer of polysilicon. The starting material is p-type, with an epitaxial layer of thickness 5.5 µm on a p+ heavily doped substrate. The main features of the process are summarised in **Table 4.1**. As the process has a single layer of polysilicon it is not possible to implement the photo-gate type pixel described in Chapter 3.

Layer/Implant/Well	Depth/Thickness (μm)
Gate oxide	0.0115
Field oxide	0.6
n+ implant	0.3
p+ implant	0.3
N-well	1.15
P-well	1.6
Epitaxial layer	5.5

Table 4.1 Tower Semiconductor TS50 standard fabrication process summary

4.3.2. Photodiode structures

The features of the TS50 process enable the production of two types of photodiode. A cross section of each variety is shown in **Figure 4.6**. The two structures are referred to as the n+ in p-well diode and the n-well on p-type substrate diode. From this point onwards the two diodes will be referred to as the n+/p-well and n-well/p-sub diodes. It is not possible to produce the pinned photodiode described in the Chapter 3, as this requires a further specialised p+ implant not available with the TS50 process.

The n+/p-well photodiode consists of an n+ implant sitting in a p-type well. It is essentially the same structure as the source and drain regions of an n-channel transistor. The n+ implant is 0.3 μm deep and the depth of the p-well is 1.6 μm.

The n-well/p-sub diode is a simpler construction than the n+/p-well. It consists of an n-type well 1.15 μm deep sitting in the epitaxial layer, therefore it will have a deeper associated depletion depth than the other diode.

Figure 4.6 TS50 photodiode cross sections

4.4. SPICE electrical simulations

During the design phase of the project, many aspects of the pixel operation were simulated using a CAD package combined with models provided by Tower Semiconductor. These simulations were performed by Steve Bowring at e2v technologies using Eldo from Mentor Graphics and HSPICE from Synopsys. The key results and analysis of these simulations are described in the following sections.

4.4.1. Pixel reset

The first stage of the electrical simulations involved modelling the pixel reset behaviour. There are essentially two design options for this. One can use either an n- or p-channel reset transistor as the switch to connect the photodiode to the reset level V_{RD}. The advantage of using the n-channel reset is that it eliminates the need for any n-well regions within the pixel. This means that the pixel layout can be more compact. The disadvantage is that the signal swing will be reduced as n-channel reset can only be 'hard' up to a value equal to $V_{RD} = V_{DD} - V_T$, as explained previously in Chapter 3. The reset gate could possibly be driven at a level above V_{DD}, if the process allows, ensuring hard reset to 5 V. However this would only be suitable for a sensor with a global reset connection. Overdriving of the reset gate would not be possible with raster scan style whereby the reset signal is derived from the select line of the vertical scanning register which would use the chip supply voltage V_{DD}. The alternative is to use a p-channel reset transistor. The disadvantage of this solution is that the device requires an extra n-well for the p+ source/drain regions. This means that the pixel layout is less compact and the size of the photosensitive site may be compromised. A further drawback of the p-channel reset solution is that the sense of the reset clock is opposite to that of the n-channel as the device is switched on when the gate is clocked low. This complicates the raster scan architecture as the reset pulse must be the opposite sense to the row select pulse. The p-channel reset pixel would therefore better suit a global reset option.

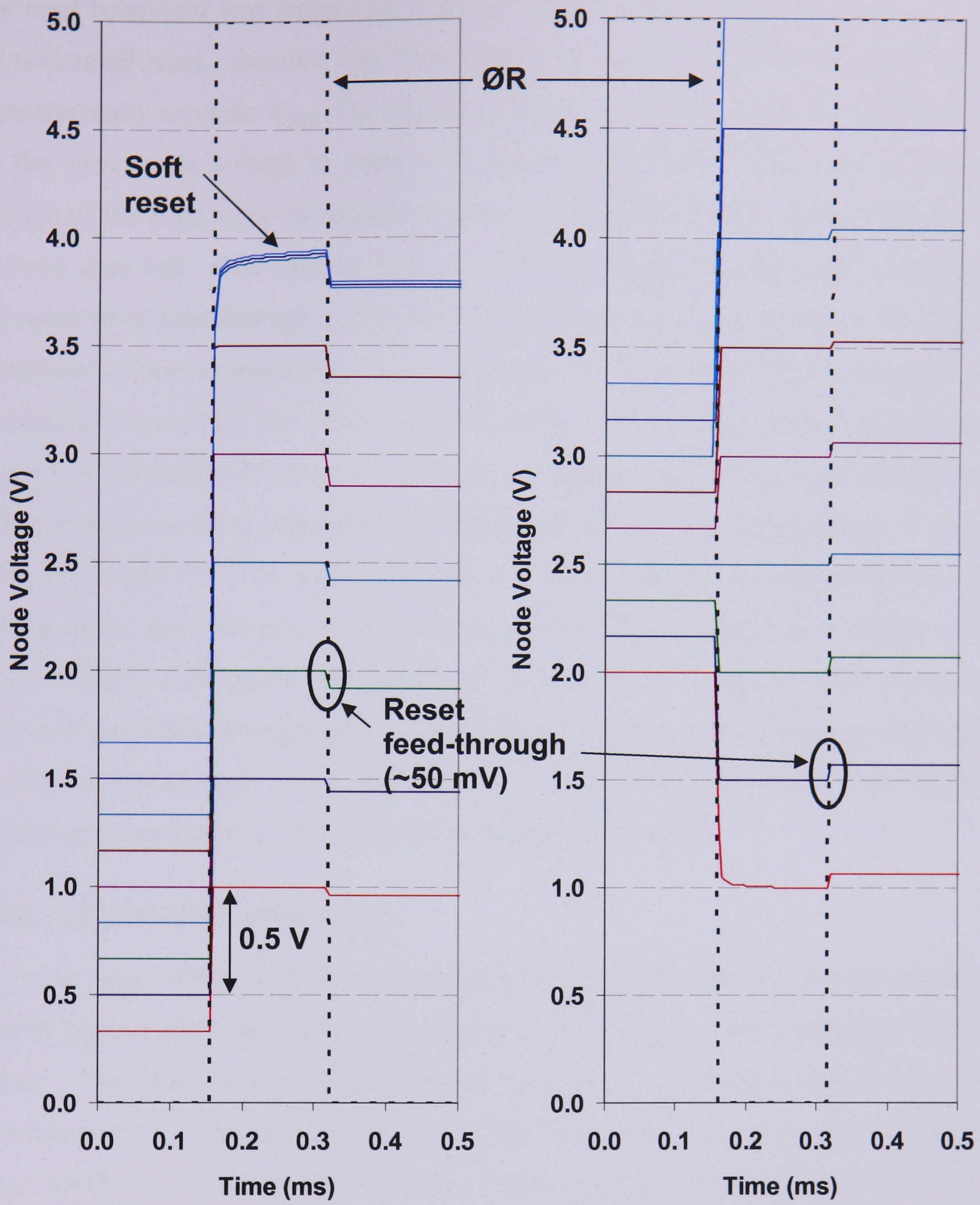


Figure 4.7 N- channel (left) and p-channel (right) reset simulation for a range of reset drain voltages

Figure 4.7 shows the simulation for the n- and p-channel reset solutions. V_{DD} was fixed at 5 V and V_{RD} was varied from 1 to 5 V in 0.5 V steps. For the n-channel reset $ØR_N$ was normally low at 0 V and then clocked high to 5 V to connect the sense node to V_{RD}. For the p-channel reset $ØR_P$ was normally high at 5 V and was clocked low to 0 V to reset the sense node. The reset pulse width for both polarities was 150 µs.

The reset behaviour was correct up to a reset drain voltage of approximately 3.5 V for the n-channel reset. Beyond this level reset was clearly 'soft' and the pixel charged logarithmically towards V_{RD}. The characteristic behaviour immediately after reset was for the sense node voltage to relax to a slightly lower level. This was due to feed-through of the reset pulse by capacitive coupling between the reset gate and the node as the reset goes low. One can see that the reset feed-through increases as V_{RD} increases. Increased reset feed-through will reduce available signal swing, therefore this must be considered when determining bias conditions for the chip. The p-channel reset simulation shows that the node resets correctly for all reset drain voltages up to V_{RD} = 5 V. Therefore it would be possible to common V_{RD} to V_{DD}. One can also see a further benefit of the p-channel reset solution where the reset feed-through is positive rather than negative. This means that after reset feed-through the node settles to a value slightly above the reset level, V_{RD}. This means that the pixel will have a larger voltage swing available at the node. For subsequent simulations the n-channel reset solution was used as it simplified the operation of the address circuitry for the larger scanned arrays. As the n-channel reset was correct up to V_{RD} = 3.5 V, this value was fixed for subsequent simulations to maximise the working signal range.

4.4.2. Column load simulation

The next stage of the simulation study involved modelling the column load transistor used as part of the source follower circuit to buffer the sense node voltage to the array output. The basic source follower circuit consists of the in-pixel follower transistor connected to the column load transistor. The two devices are connected via the row select transistor. The magnitude of the current flowing though the in-pixel follower when the row select transistor is enabled is determined by the channel dimensions of the column load and the gate voltage V_{LG}. In the first simulation the load current variation with channel length, L and gate voltage V_{LG} was investigated. The gate length vas varied from 10 to 50 μm in 10 μm increments and V_{LG} was varied from 1 to 3 V in 0.5 V steps. **Figure 4.8** shows the simulation results. One can see that for a fixed load gate voltage the current decreases as the gate length increases and is proportional to 1/L, as predicted by the transistor equations in Chapter 3. A simulation was also performed to calculate the current flowing through the photo-site when the enable transistor is off. It was found that the photo-site off current increases as gate length increases and

decreases as load gate voltage increases. The amount of current flowing was approximately 2 pA, so it is insignificant compared with the photo-site on current.

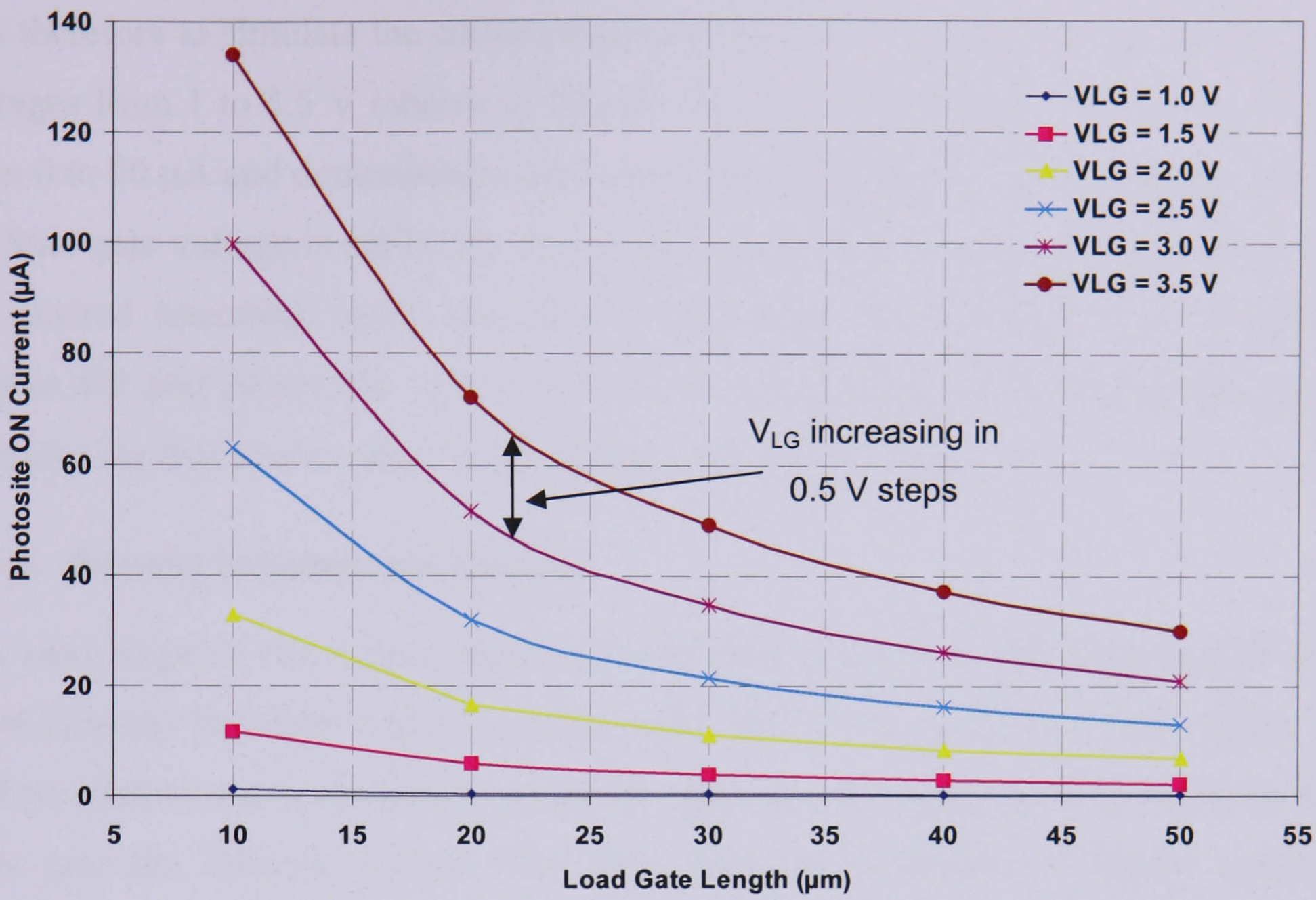


Figure 4.8 Photo-site ON current vs. load gate length for a range of gate voltages

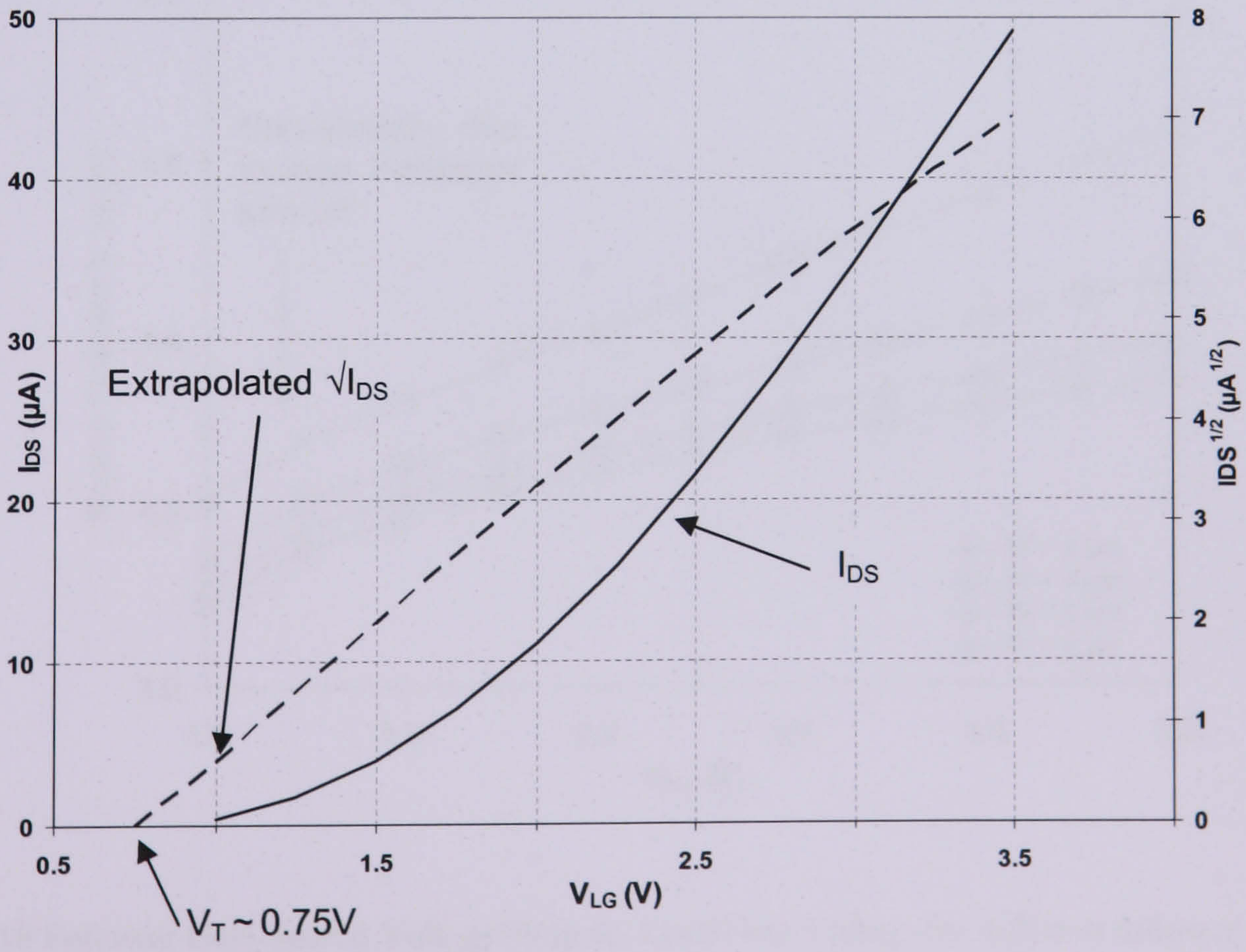


Figure 4.9 Load current variation with V_{LG} for a 5 × 30 μm load transistor

From the previous results the load gate length and width were set at 5 μm and 30 μm, respectively, for further simulation. These dimensions enable each column load transistor to reside comfortably within the chosen pixel pitch of 20 μm. The next step was therefore to simulate the current supplied by the 5 × 30 μm load for a range of gate voltages from 1 to 3.5 V (shown in **Figure 4.9**). Over this range the current increases from 0 to 50 μA and demonstrates the classic quadratic dependence. The final value for the load gate voltage is set by the drive requirement to the column line capacitance for the desired operating speed and also by the need to minimise power dissipation. **Figure 4.9** also shows the square root of the load current and the extrapolated curve indicates the threshold voltage of the transistor to be ~ 0.75 V.

4.4.3. Source follower simulation

The next stage of the output circuit analysis was to simulate the behaviour of the in pixel follower transistor which forms the other half of the source follower circuit. The first simulation was performed to predict the gate-source voltage drop between the sense node and the follower source. The drop must be minimised to ensure maximum analogue voltage swing at the output. It is particularly important to minimise this drop in a design with an n-channel reset as the available signal swing is already limited.

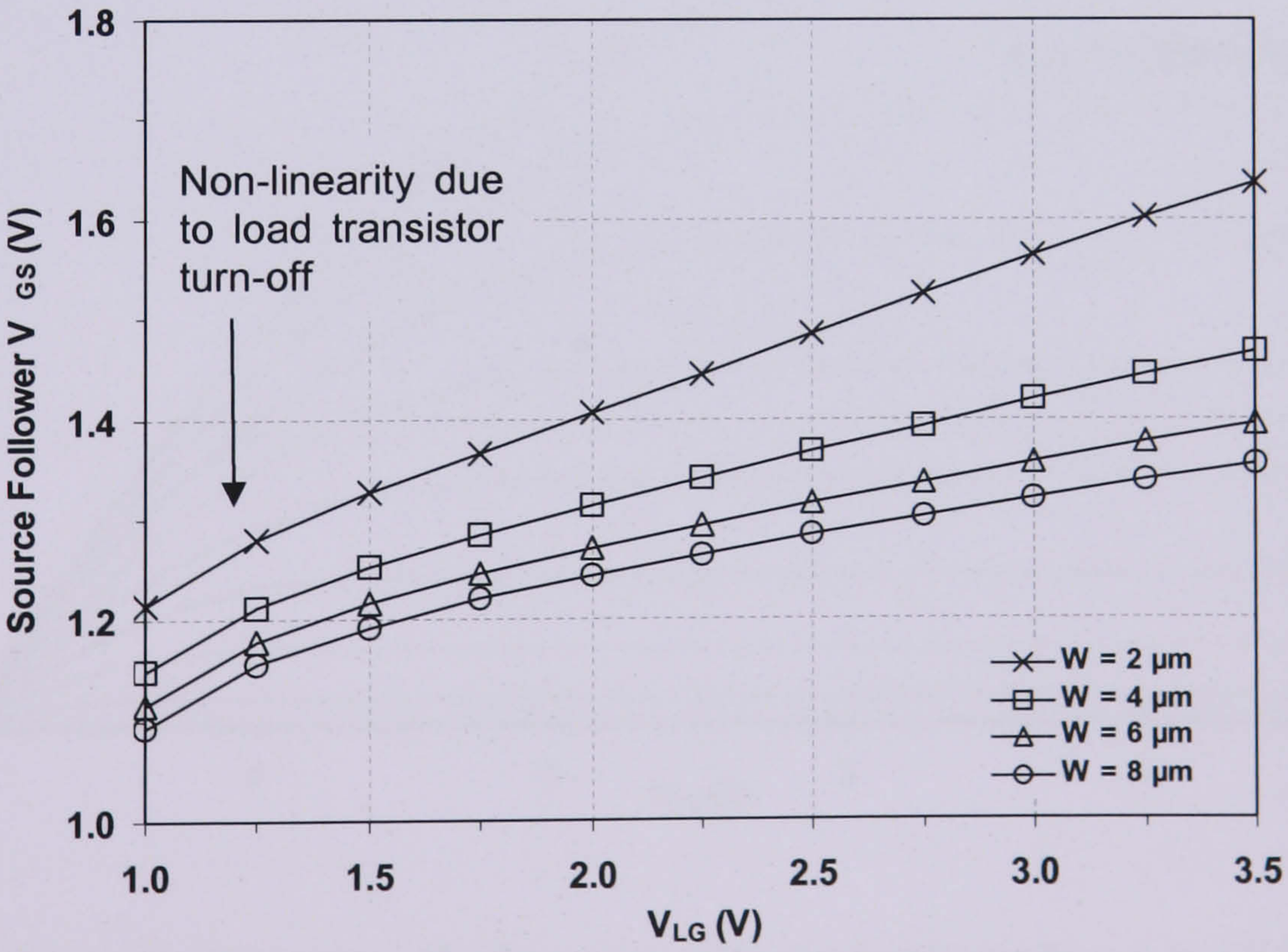


Figure 4.10 Follower Gate-Source Voltage Drop vs. Load Gate Voltage for different follower gate width

Two factors, the column load transistor current and the source follower gate width, primarily influence the gate-source drop. The row select transistor was constantly enabled and the load gate voltage was varied from 1.0 to 3.5 V. Four gate widths were used from 2 to 8 μm in 2 μm steps. **Figure 4.10** shows the result of the simulation. One can see that the drop increases with working current for a fixed gate width but decreases with follower gate width for a fixed working current. It is therefore desirable to minimise the load gate voltage and current but maximise follower gate width. Obviously there is a trade off with pixel layout as a larger follower transistor will encroach into any potential photosensitive area. Also, the variation of V_{GS} drop becomes non-linear for gate voltages less than 1.5 V (load current < 5 μA). This implies that the load is beginning to turn off below this level and this was shown previously in the simulation in **Figure 4.9**. From these simulations the follower gate width was provisionally set to 6 μm and the working current for all further simulations was set to 11 μA, which is equivalent to a load gate voltage of 2 V. The follower gate width also affects the V/V gain of the follower, the sense node responsivity and noise, therefore it was not finalised until those three factors were investigated further.

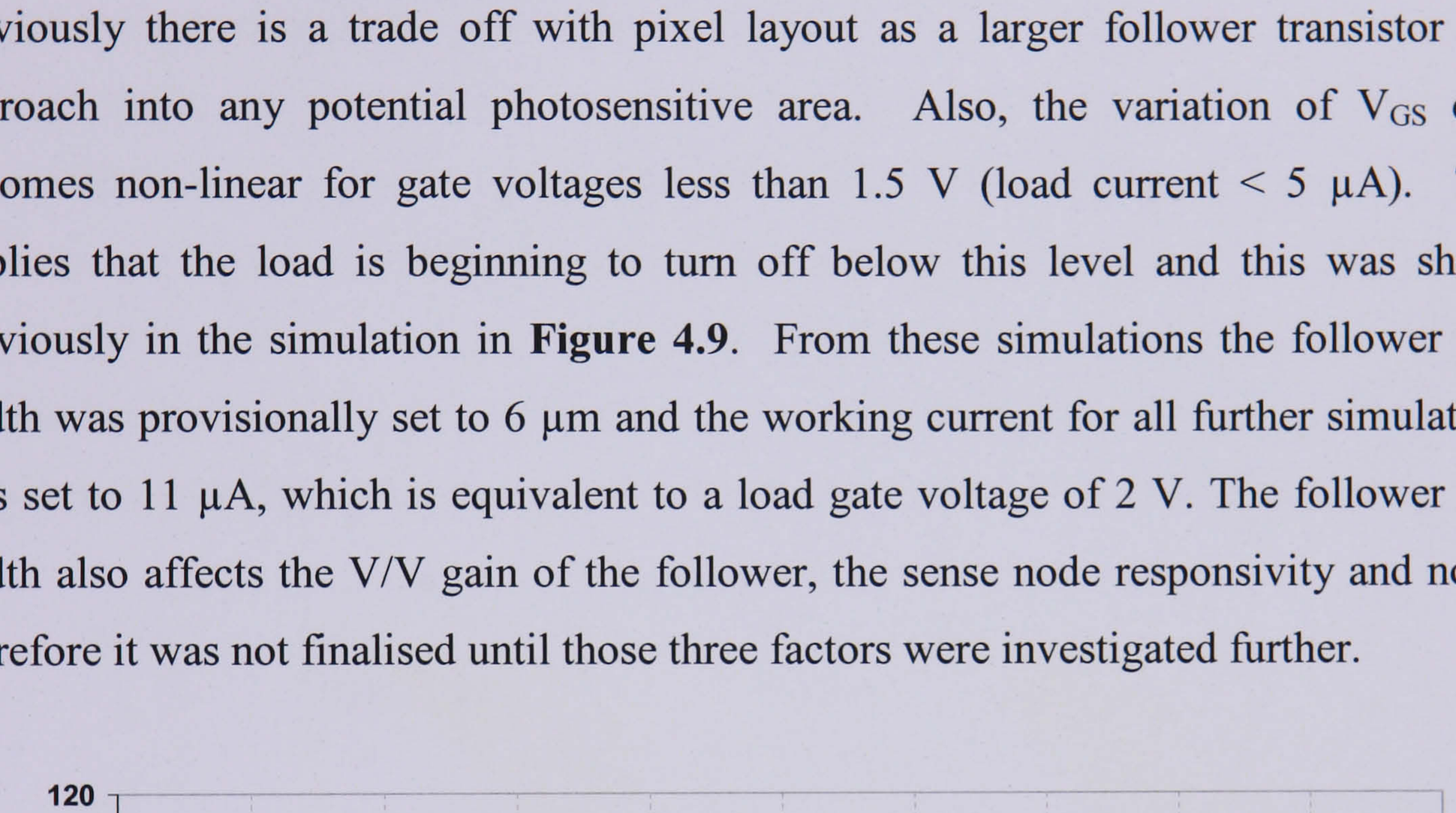


Figure 4.11 Column load current vs. V_{DS} for a range of load gate voltages from 1 to 5 V in 0.5 V steps

Further effects of various bias conditions on the load transistor were simulated. For the source follower to operate with linear characteristics the load transistor must operate in

the saturation region. The follower will function with the load operating outside of the saturation region but it will introduce an additional source of non-linearity to the output circuit. The variation of source-drain current with drain-source voltage V_{DS} was simulated for a 5 × 30 μm² load transistor for a range of load gate voltages. The results of the simulation are shown in **Figure 4.11**. If the load gate voltage is set at 2 V any signal swing at the node will take the transistor into the linear/triode region and introduce an additional source of non-linearity. One can see that if the load is set to higher voltage/current, the 'knee' moves outwards such that the node never acts as a current source. For the case of $V_{LG} = 2$ V the knee is at approximately 1 V. The source of the follower never reaches a voltage greater than 2.5 V (if the node is reset to 3.5 V) therefore, if the source of the follower swings downwards greater than 1.5 V, the V_{DS} of the load will go below 1 V and the load transistor will operate outside of the saturation region (in the triode region). The voltage up to the knee can be reduced using other design solutions but there are knock-on consequences that are not considered here.

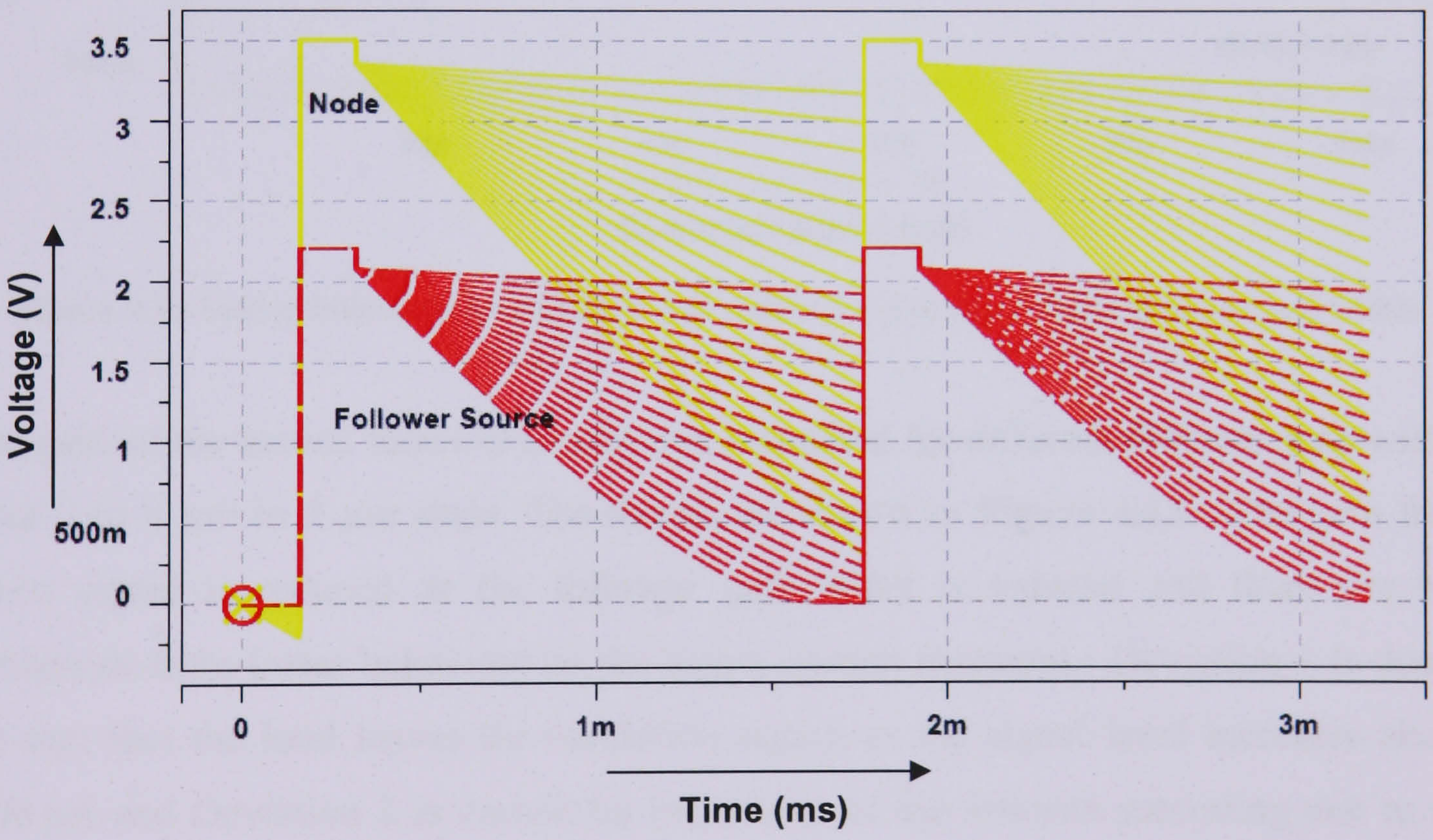


Figure 4.12 Node and source of follower waveforms for a sweep of signal currents from 5 to 100 pA

For the next stage of the analysis the signal behaviour of the source follower circuit was simulated by applying a timed current to the sense node (i.e. equivalent to a photo-generated current) and investigating the linearity, responsivity and gain. The row select transistor is switched on. The duration between samples was 1.43 ms, therefore a current of 10 pA equates to ~ 90 ke^- collected on the node. **Figure 4.12** shows the

signal output at the sense node and the follower for a sweep of signal currents from 0 to 100 pA in steps of 5 pA. It can be seen that although the signal at the sense node does not saturate before the next reset, the output at the follower source does saturate because of the large gate-source voltage drop. One can also see that the rate of change of the output is less at the follower source than at the sense node due to the less than unity gain of the follower circuit.

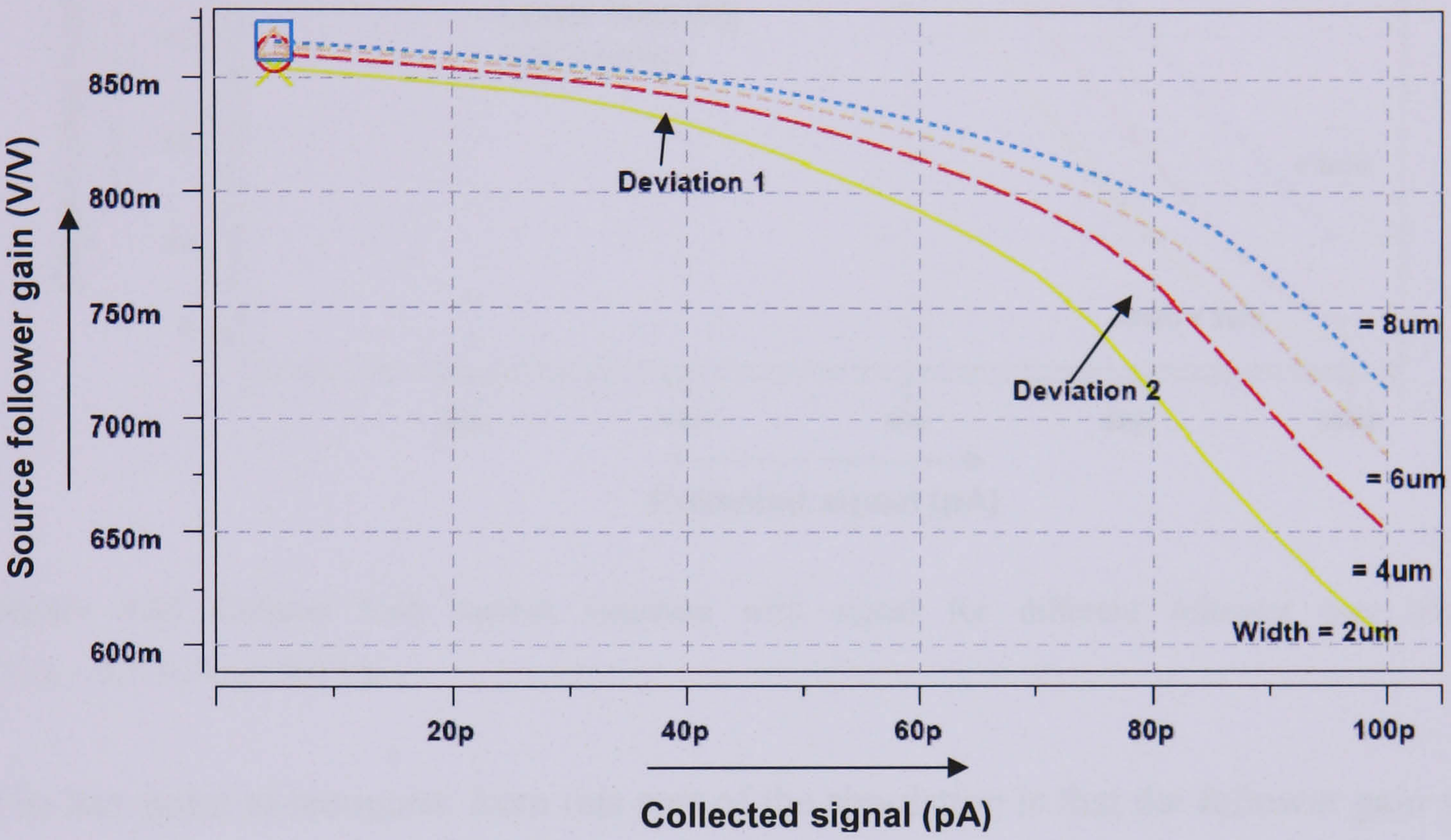


Figure 4.13 Source follower gain variation with collected signal for different follower gate widths

The gain of the source follower circuit was simulated for different follower gate widths from 2 to 8 μm in 2 μm steps. The results are shown in **Figure 4.13**. The gain for a given signal is reduced as the follower gate width is reduced and there are two deviations from linear behaviour as the signal current increases. Deviation 1 is due to the fact that the load leaves the saturation region as the signal level increases above ~ 30 pA and Deviation 2 is caused by the source of the follower saturating due to the gate-source voltage drop.

The point at which the load leaves the saturation region was investigated in more detail by simulating the variation of current through the load for different follower gate widths as the sense node collects signal. The results are shown in **Figure 4.14**. It can be seen that the load leaves the saturation region when the signal goes above 30 - 50 pA depending on the gate width. It should also be noted that there is a small decrease in

gain in the saturation region, which is due to second order effects beyond the scope of this thesis.

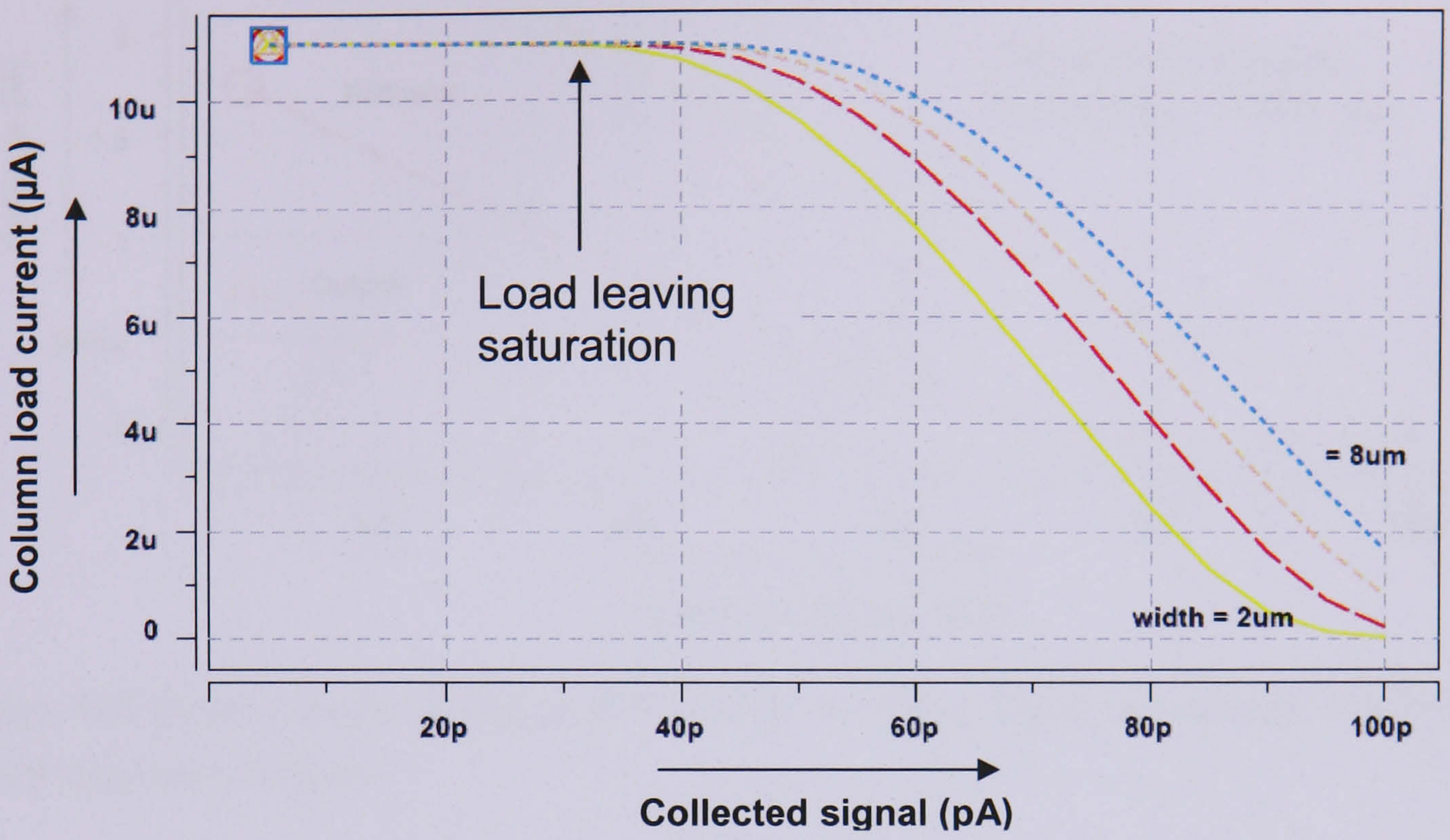


Figure 4.14 Column load current variation with signal for different follower gate widths (V_{RD} = 3.5 V, V_{LG}= 2.0 V)

The key point to recognise from this part of the simulation is that the follower gain will increase if a wider follower transistor is used. There is also less voltage drop across the follower when a wider gate width is used, and this therefore gives more signal swing before the follower source saturates and the load enters the triode region. The drawback of using a wider follower transistor is it will have an increased contribution to the node capacitance, thereby reducing responsivity, and it will require increased layout space reducing the potential photosensitive area. For the subsequent analysis the follower gate width was somewhat arbitrarily set to 6 μm. Simulations were also performed on the row select transistor and the dimensions were not found to be critical.

4.4.4. Output buffer

The next step in the read-out path of the device is to add a further switch to sample the column output onto the video output line and also to add an additional output source follower that is sufficient to drive an off-chip load.

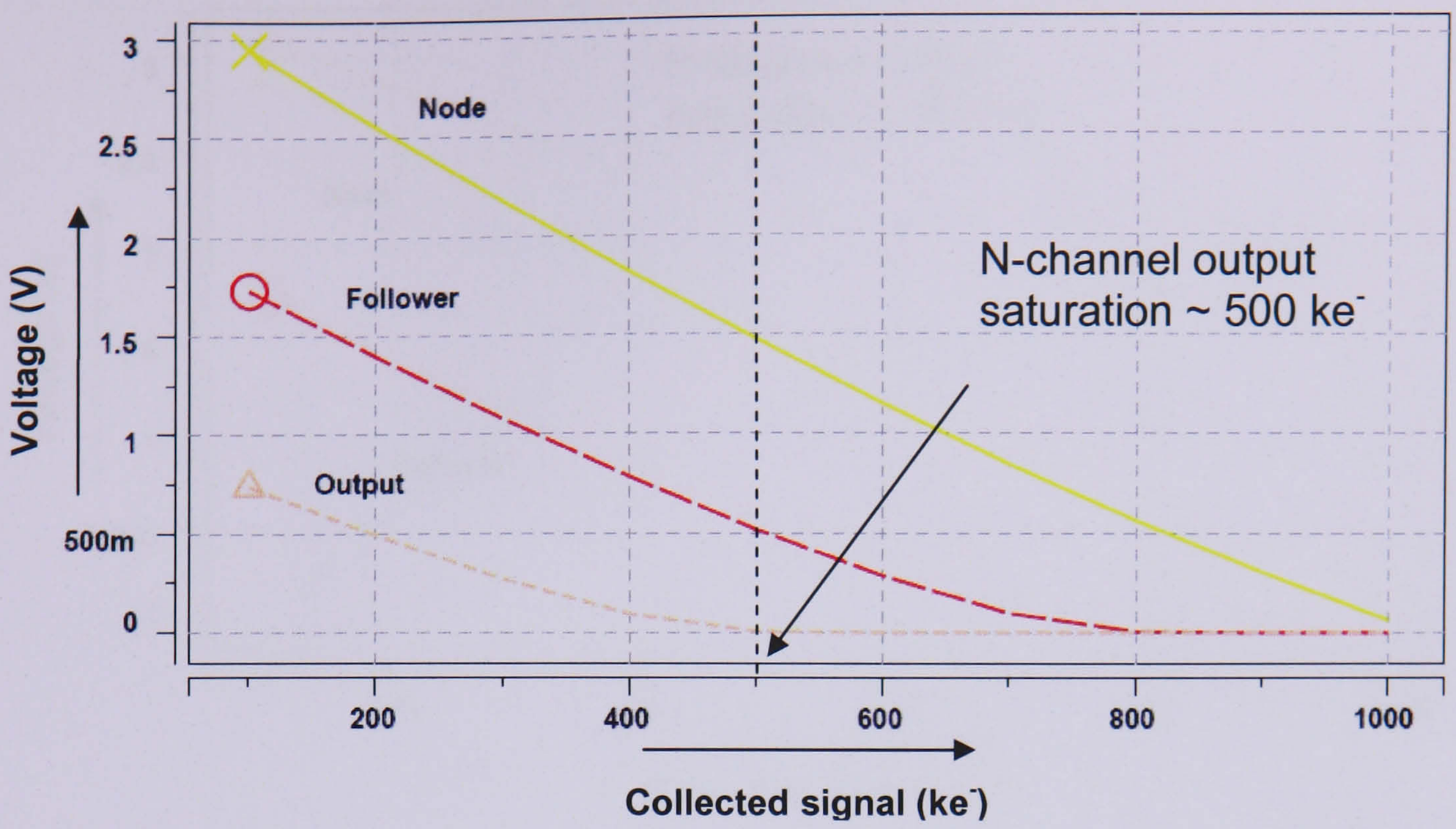


Figure 4.15 Signal voltages through readout path for increasing signal level at node with n-channel second stage output follower

Initially an n-channel device was considered. **Figure 4.15** shows the node, source follower and output waveforms for increasing signal in electrons up to 1000 ke$^-$. One can see that the output voltage range is further reduced due to the extra gate-source voltage drop across the second stage follower transistor. Although there is sufficient voltage swing to collect 800 ke$^-$ at the node, the output source saturates after 500 ke$^-$ have been collected. The extra n-channel output follower is therefore a poor solution if large signal handling capacity is required. Therefore a p-channel second stage output follower was simulated. The node, source follower and p-channel output waveforms are shown in **Figure 4.16**. The use of the p-channel follower introduces a positive DC offset to the signal restoring the device saturation to 800 ke$^-$, which is a saturation level similar to that originally determined by the first stage source follower.

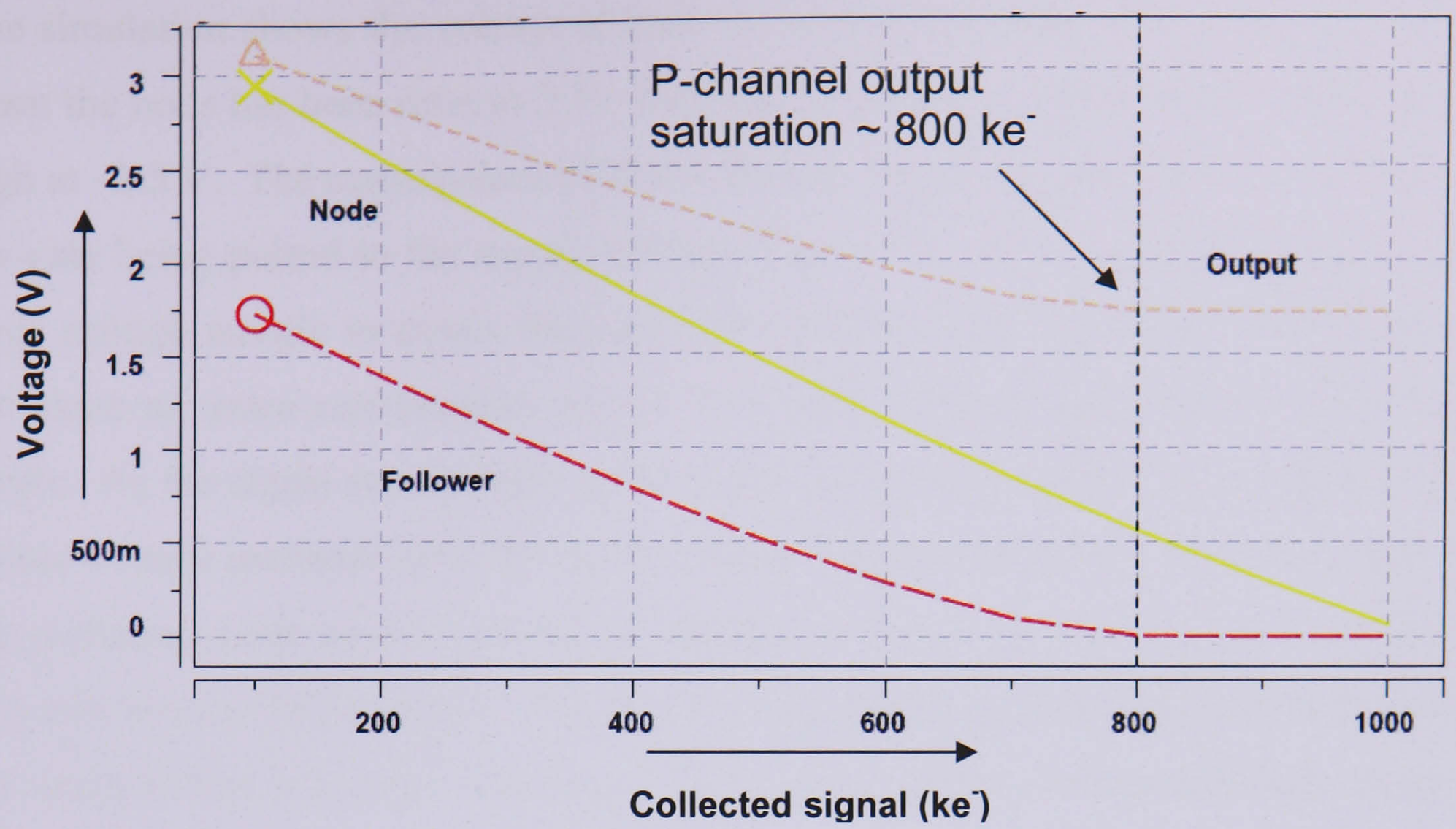


Figure 4.16 Signal voltages through readout path for increasing signal level at node with p-channel second stage output follower

The final part of the pixel output circuit simulation was to investigate the effect of using a p-channel reset transistor on the output circuit behaviour. Recall that a p-channel reset enables correct reset of the node to a value of 5 V. The problem with resetting the node to such a high voltage is that it affects correct operation of the row select transistor as a low resistance switch. The problem is illustrated by the simulation shown in **Figure 4.17**.

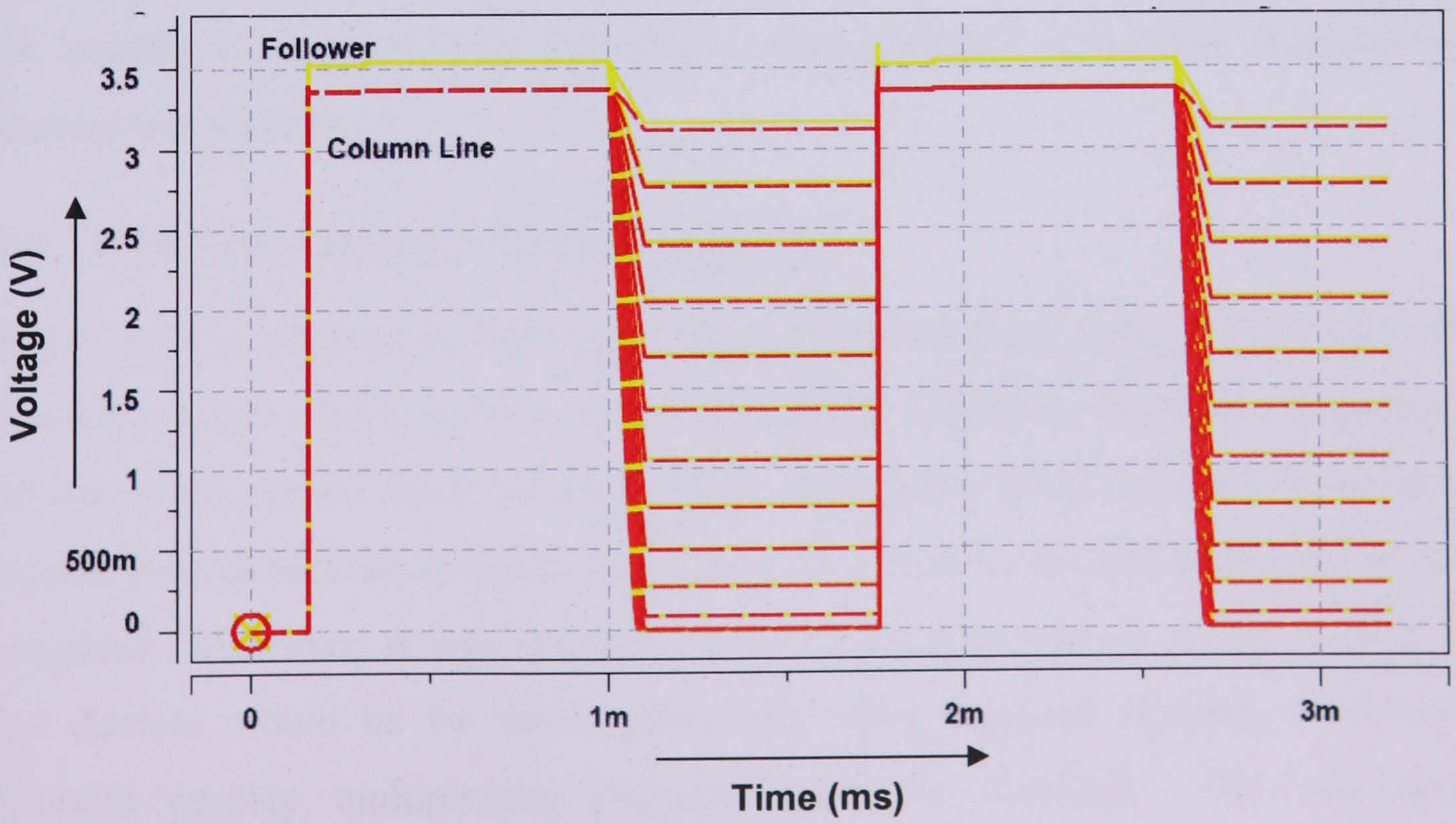


Figure 4.17 Voltage levels at the source and drain of the enable transistor for a sweep of signals, $V_{RD} = 5$ V

The simulation shows the voltage at both the source and drain of the enable transistor when the node has been reset to 5 V. One can see that the voltage at the source is quite high at ~3.5 V. The consequence of this is that the V_{GS} of the transistor is ~1.5 V due to the gate being pulsed to the supply voltage V_{DD} = 5 V. V_{GS} does not exceed V_T by a large enough margin to ensure the correct behaviour of the transistor. The effect is to introduce an extra non-linearity in the V/V gain of the output circuit at low signal levels. As the signal accumulates at the node, the source voltage reduces and the gate-source voltage increases such that the transistor operates correctly. This is not seen with the n-channel reset as the node never charges to a high enough voltage to reduce the V_{GS} into the non-linear region. The non-linearity can be partially reduced by increasing the width of the row select transistor. However a small reduction does not justify the large increase in transistor area, which takes up valuable layout space for the photodiode. The obvious solution to the problem is to reduce V_{RD}. With an n-channel second stage output this reduces the signal capacity by 100 ke^- for each 0.5 V reduction in V_{RD}. The signal loss can be regained by utilising the p-channel second stage output mentioned previously. The problem with reducing V_{RD} below V_{DD} is that separate connections are required and these must be tracked with metal across the chip with loss of fill-factor. The other possible solution to the non-linearity problem is to use a p-channel row select transistor. This would be useful for a p-channel raster scan reset type design. However the p-channel transistor suffers from the same problem when the source approaches V_{SS} as when the n-channel source approaches the gate voltage V_{DD}. This introduces a further non- linearity, so the p-channel row select is probably an inappropriate solution

4.4.5. Row and column scanning circuitry

Address logic is required for the larger arrays to provide clock pulses for the reset (ØR), the column select (ØCS) and the row select (ØRS) functions, to thereby sequence the read-out of the device. Such arrays would contain many more rows and columns than available pin connections to the device, therefore a form of on-chip multiplexing circuit is required. However, it was decided for simplicity that read-out of the smaller Test Pixel devices would be by direct addressing using external circuitry, therefore no additional on-chip multiplexing circuitry would be required. The two options considered for the larger arrays were a static shift register or a counter decoder. The static shift register solution was to propagate a logic '1' through a number of stages

equal to the number of rows or columns. This would provide sequential enabling of the rows and columns to establish a serial readout of the device. The row (Y) register could also be used to supply raster scan reset by using the same row select line to reset the previously read out line. The second solution for column and row addressing was to implement a counter-decoder. The counter-decoder design required more space on the sensor die but it would enable true random pixel access and facilitate Region of Interest (ROI) readout. Both address solutions were simulated and evaluated and the static shift register was selected due to it being a simpler design.

4.4.6. Power dissipation

The static power dissipated by a single pixel when enabled (P_{Pixel}) is determined by the column load current (I_{Pixel}) and the supply voltage (V_{DD}). It is given by:

$$P_{Pixel} = I_{Pixel} V_{DD} \tag{4.1}$$

Therefore assuming a supply current of 11 μA (V_{LG} = 2 V) and V_{DD} 5 V, a single pixel will dissipate ~ 55 μW. The array is addressed by enabling an entire row in sequence therefore only one row dissipates power at a time. Therefore the row power consumption is equal to the array power consumption and the total power will be independent of operating frequency assuming a 50 % duty cycle. The total static power dissipation from the pixel array is therefore given by:

$$P_{Array} = P_{Pixel} N_{Cols} \tag{4.2}$$

The power consumed by a 128 × 128 pixel array will therefore be ~ 7 mW.

Additional static power ~ 0.8 mW is dissipated in the final output source follower.

Extra dynamic power (P_D) will be dissipated by the vertical and horizontal shift registers. The dynamic power dissipated by digital circuitry is given by:

$$P_D = CV^2 f \tag{4.3}$$

Where C is the total capacitance being driven by the circuitry, V is the supply voltage and f is the operating frequency. Total power consumption for the horizontal and vertical registers ($P_{H,V}$) will thus be:

$$P_{H,V} = V^2(C_H f_H + C_V f_V) \tag{4.4}$$

The readout frequency is determined by the horizontal shift register frequency (f_H). The vertical shift register frequency divided by the number columns is f_H/N_{Cols}. Equation 4.4 therefore can be simplified to:

$$P_{H,V} = V^2 f_H(C_H + \frac{C_V}{N_{Cols}}) \tag{4.5}$$

The dynamic power dissipated is strongly dependent on the parasitic capacitances being driven. Simulations showed that the horizontal shift register running at a frequency of 1 MHz dissipates ~ 20 μW per column/stage. Therefore the register will dissipate ~ 2.6 mW, assuming 128 columns/stages. The two extra input circuits to the register dissipate an additional 300 μW giving a total of ~ 2.9 mW for the horizontal register. The vertical register runs at a lower frequency and was found to dissipate a total of ~ 2 mW including all components. The total power dissipated by a 128 × 128 pixel array and associated circuitry is therefore ~ 13 mW. Further simulations showed that a sensor with 1000 × 1000 pixels would consume ~ 95 mW. The increase does not scale proportionally with pixel dimensions because of the extra drive capacitance introduced by the longer row and column tracks. It should be noted that these power dissipation values are not dissimilar with comparable CCD sensors of similar size and readout speed.

4.4.7. Summary

The finalised dimensions of the in-pixel and output circuit transistors, as determined by the electrical simulations, are summarised in **Table 4.2**. These dimensions guided the physical layout of the pixel described in the next section.

Transistor	W (µm)	L (µm)
n-channel reset	2.0	0.5
p-channel reset	2.0	0.5
Source follower	6.0	0.5
Enable/Select	3.0	0.5
Column load	5.0	30.0
P-channel output follower	40.0	0.5
Multiplexer	6.0	0.5

Table 4.2 Finalised transistor dimensions

4.5. Pixel layout considerations

The physical layout of the test structures was designed by Steve Bowring at e2v using a suite of tools within the Mentor Graphics CAD environment. The circuit schematic entry used Design Architect IC and the physical layout used IC Station. The available layers in the TS50 process are summarised in **Table 4.3** and the use of these is illustrated in **Figure 4.18**, which shows a typical layout for the majority of the Test Structures. Specific detail on each of the finalised designs for the Test Pixels and the Imaging Arrays is given in Chapter 5. The in-pixel transistors were laid out within a 20 µm × 20 µm square (i.e. the pixel pitch) and combined with the metal interconnects and photodiode to create a single 3T pixel cell. Layout of the transistors within the pixel is as follows. The follower and row select transistors are connected back-to-back to minimise space. Metal layer 1 is used for the ØRS and ØR clock lines and metal layer 2 is used for the V_{OS}, V_{DD} and V_{RD} connections. Metal layer 1 is also used to connect the drain of the reset transistor to the vertical V_{RD} line and to connect the photodiode (sense node) to the gate of the follower transistor. This general arrangement was used for all pixel designs with some variation depending on the type of pixel.

Layer	Description
n+ implant	n-type implant
p+ implant	p-type implant
n well	n-type well
Composite	Gate Oxide definition of the Source/Drain regions n+ composite are source/drain regions which receive an n+ implant p+ composite are source/drain regions which receive a p+ implant
Poly	Polysilicon gate
Contact	Connection between M1 and Poly and M1 and n+/p+ source/drain regions
Metal 1 (M1)	Lower interconnect level
Via	Connection between M1 and M2
Metal 2 (M2)	Upper metal interconnect level

Table 4.3 TS50 layer description

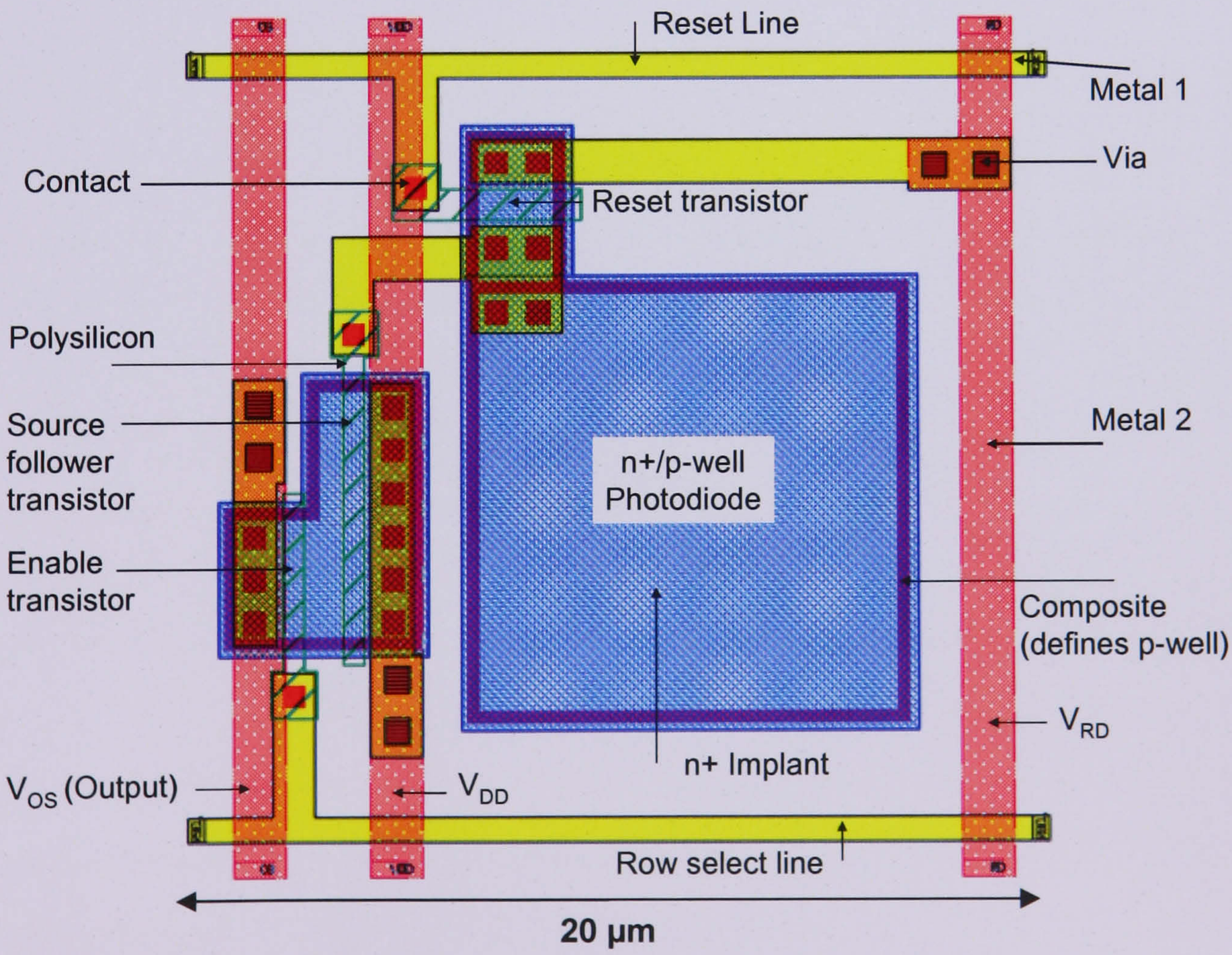


Figure 4.18 CMOS Pixel CAD Schematic

4.6. Summary

This chapter has described CMOS manufacturing processes and explained how they are used to produce the three transistor active pixel. The TS50 CMOS process, selected to manufacture the Test Structures, was also described. The remainder of the chapter focussed on the issues considered in the sensor design process including the electrical simulations performed by the designers. The next chapter gives a detailed description of the finalised designs and the range of test equipment developed for characterisation of the new devices.

Chapter 5: The e2v Test Structures and characterisation equipment

Chapter 5 gives a detailed description of the finalised Test Pixels and Imaging Arrays. The chapter also outlines the range of drive electronics and test equipment that were developed to enable characterisation of the different designs.

5.1. Introduction

The aim of this thesis was to set in place a series of design rules and processes that could be utilised in future projects to produce high performance sensors for a given scientific application. The main objectives of the work were to:

- Produce a fully functioning imaging device
- Explore pixel design optimisation for a given scientific application
- Demonstrate scalability of pixel designs
- Develop a range of APS characterisation techniques
- Quantify foundry dependent parameters of dark signal and quantum efficiency
- Relate simulated layout-dependent parameters to measured values

To meet these objectives a range of different prototype sensors were implemented using the TS50 process. A series of small scale 10 × 10 pixel arrays known as the 'Test Pixels' were used to produce a wide range of pixel designs and relate simulated layout dependent parameters to measured quantities. In addition to the Test Pixels two larger format 128 × 128 pixel 'Imaging Arrays' with on-chip scanning circuitry were produced to demonstrate scalability of pixel designs and fully functioning imaging devices. A detailed characterisation of the manufactured devices was then required to verify the design principles. Therefore a range of drive electronics was developed to supply bias voltages and digital sequencing, sample analogue data and perform analogue to digital conversion. The chapter is organised as follows. The first section describes the three different devices known as the Test Pixels. The general architecture is outlined along with the sequencing requirements and the specific layout of each device. The system developed to characterise the devices, based around a digital signal processor (DSP) and analogue to digital converter (ADC), is then described. The method used to program the DSP to output sequencing pulses to the APS is explained and also the incorporation of the DSP into a complete drive and acquisition system used to control the Test Pixels

is outlined. The second half of Chapter 5 describes the architecture and sequencing requirements of the Imaging Arrays. The system used to control the Imaging Arrays, based around a high-speed digital input/output (I/O) card and frame-grabber, is then described. A further drive electronics system developed to investigate performance of the Imaging Arrays at low temperatures (-100 °C), under high vacuum conditions is then outlined. The chapter closes with a description of the equipment used to perform the electro-optical characterisation, such as the mean-variance technique and quantum efficiency which is described in Chapters 6 and 8.

5.2. CMOS Test Pixels

The CMOS Test Pixels are small-scale 10 × 10 pixel arrays designed for purposes of investigating how different aspects of a pixel affect its performance. This is done by varying different parameters such as component dimensions, layout or diode structure. The use of small-scale arrays enables many types of structure to be implemented on the same device (Yang et al., 1996). Therefore considerable design effort was put into producing a range of test structures with direct access to the analogue output of each column line, to enable characterisation of various performance parameters. Direct access to the raw column output would not be possible with large arrays as any package has a finite number of connections to it and die surface is limited. If no scanning circuitry is used, pin connections are quickly filled. Three varieties of chip were fabricated named Test Pixels 1, 2, and 3.

5.2.1. General architecture

Each test chip consists of a 10 × 10 array of active pixel test structures. The floor plan of Test Pixels 1 is illustrated in **Figure 5.1**. The array is sub-divided into four quadrants A, B, C and D, each of 5 × 5 pixels.

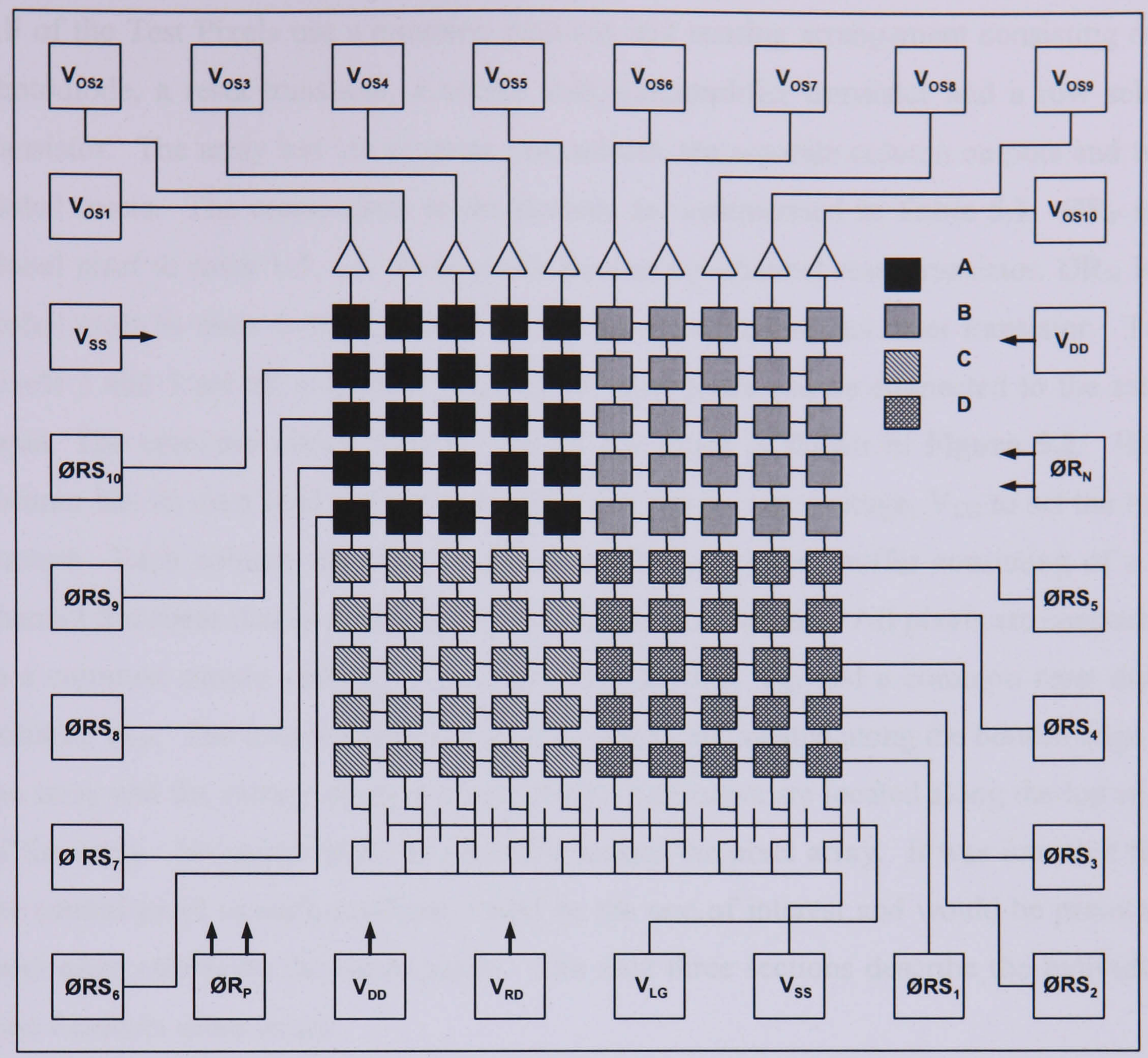


Figure 5.1 CMOS Test Pixels floor plan

Connection	Description
$ØRS_{1\text{-}10}$	Row select 1 to 10
$ØR_N$	Global reset to rows 6 to 10
$ØR_P$	Global reset to rows 1 to 5
$V_{OS1\text{-}10}$	Output voltage (V_{out}) 1 to 10
V_{DD}	Supply voltage
V_{LG}	Column load gate voltage
V_{RD}	Reset drain voltage
V_{SS}	Substrate voltage

Table 5.1 Test Pixels pin connection descriptions

All of the Test Pixels use a common read-out and sensing arrangement consisting of a photodiode, a reset transistor, a source follower/amplifier transistor and a row select transistor. The array has ten separate row selects, ten separate column outputs and two global resets. The connections to the devices are summarised in **Table 5.1**. $ØR_P$ is a global reset to rows 1-5, i.e. those pixels having a p-channel reset transistor. $ØR_N$ is a global reset to rows 6-10, i.e. those pixels having an n-channel reset transistor. Test Pixels 2 and 3 are all n-channel reset so the reset pulse can be connected to the same input. The common circuit diagram for all test chips is shown in **Figure 5.2**. Each column has its own load transistor that has a common gate voltage, V_{LG} to set the bias current. Each column also has its own second stage output buffer consisting of a p-channel transistor that is connected to an external load resistor. All pixels are connected to a common supply voltage, V_{DD}, a common ground, V_{SS} and a common reset drain voltage, V_{RD}. The load transistors for each column are located along the bottom edge of the array and the extra p-channel output buffer transistors are located along the top edge of the array. No guard rings are included around the pixel array. It was intended that the central pixel in each quadrant would be the one of interest and would be protected from edge effects by the outer pixels. The next three sections describe the individual Test Pixels in more detail.

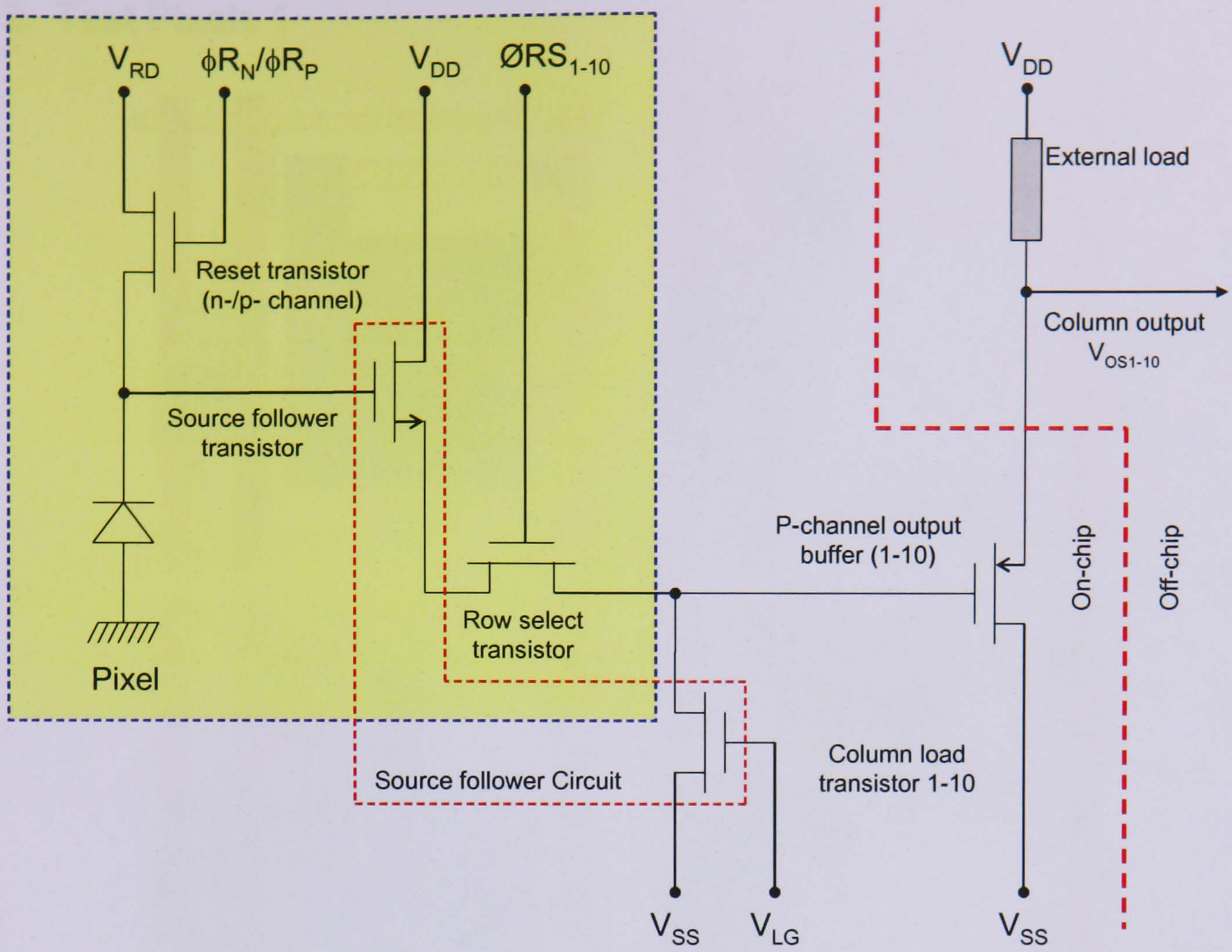


Figure 5.2 Test Pixels circuit diagram

5.2.2. Test Pixels 1

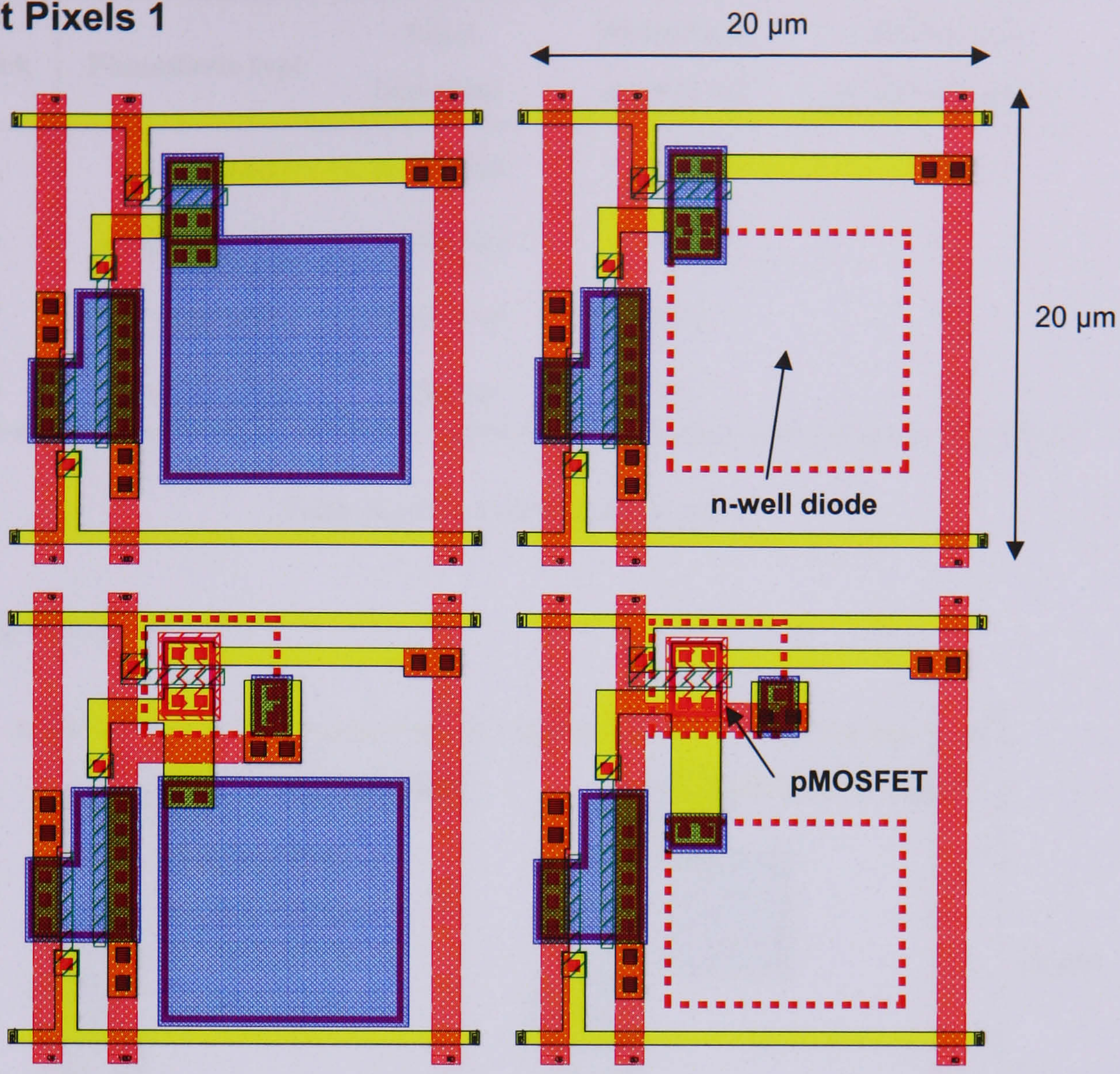


Figure 5.3 CAD schematic of the pixel design in each quadrant of Test Pixels 1. The device was intended to investigate the effect of reset transistor polarity and photodiode structure

Test Pixels 1 was intended to compare the performance of the n+/p-well and n-well/p-sub diodes and the effects on n-channel or p-channel reset. The pixel layout is shown in **Figure 5.3** and the pixel design for each quadrant is summarised in **Table 5.2**. Each design has an n- or p-channel reset transistor, and an n+ in p-well or n-well in p-type substrate photodiode. All pixels have a pitch of 20 µm and all photodiodes within each pixel have a surface area of 100 μm^2 except the bottom right quadrant, which has an area of 80 μm^2. The two p-channel reset transistor designs require an extra n-well that is biased to V_{DD}.

Block	Photodiode type	Reset transistor	Photodiode area (μm^2)	Photodiode perimeter (μm)
A	n+ in p-well	n-channel	100	40
B	n-well in p-sub	n-channel	100	40
C	n+ in p-well	p-channel	100	40
D	n-well in p-sub	p-channel	80	36

Table 5.2 Test Pixels 1 parameters

5.2.3. Test Pixels 2

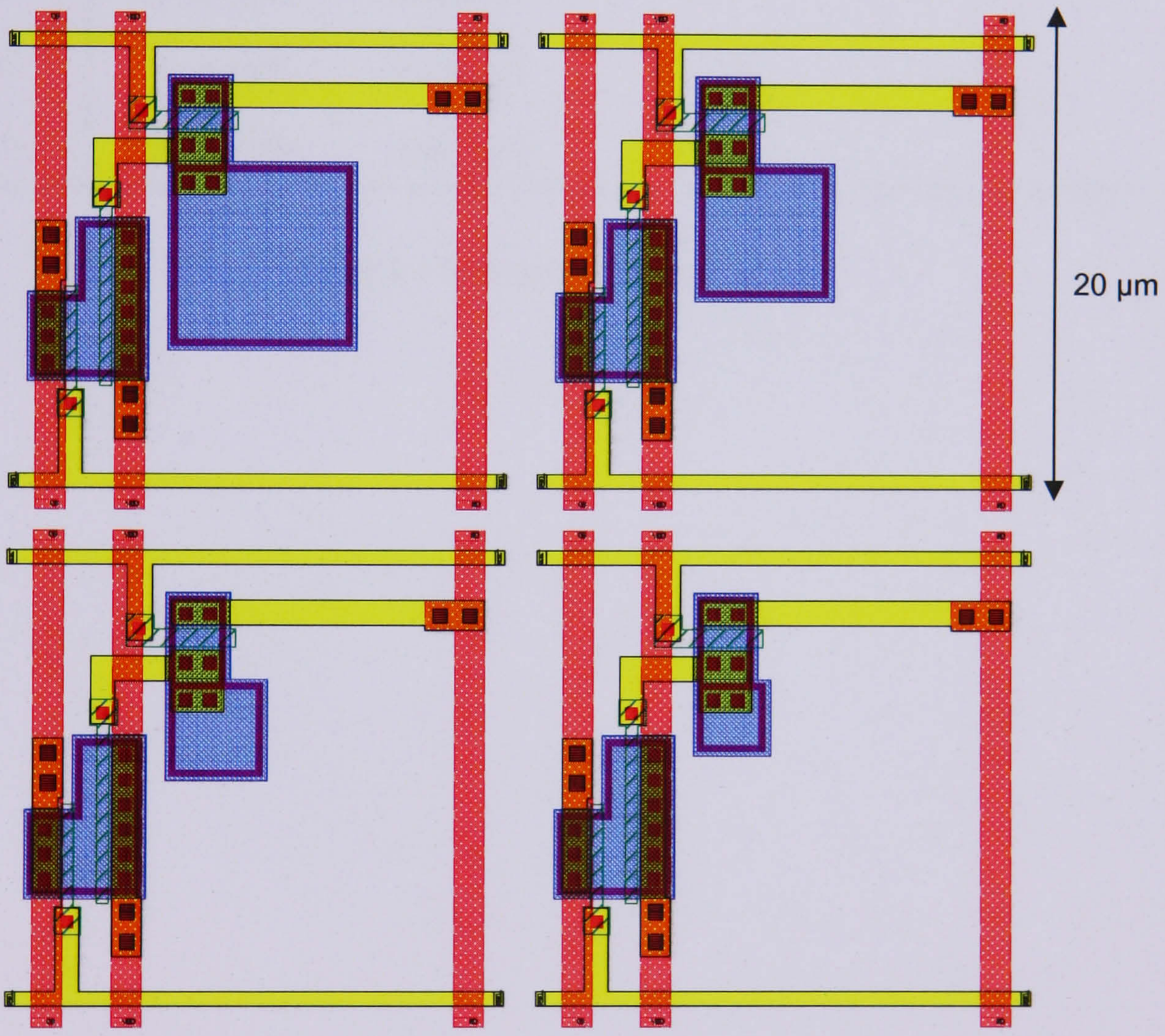


Figure 5.4 CAD schematic of the pixel design in each quadrant of Test Pixels 2. The device was intended to investigate the effect of photodiode size

Test Pixels 2 was designed to compare the performance between diodes of different sizes. It consists of four 5 × 5 pixel arrays all with n+ in p-well photodiodes and n-channel reset transistors, but each array has a different size photodiode, as shown in **Figure 5.4**. The details of each array are outlined in **Table 5.3**. Each diode is square

and the connection to the diode is made via the top left corner. So as the diode size is reduced the centre point moves away from the centre of the pixel. In this way the remaining pixel layout is preserved keeping any parasitic capacitances constant. A version of Test Pixels 2 (2a) was produced without gate protection structures to allow overdriving of the global reset above V_{DD}, and enable investigation of hard reset to V_{DD} = 5 V with the n-channel reset devices.

Block	Photodiode type	Reset transistor	Photodiode area (μm^2)	Photodiode perimeter (μm)
A	n+/p-well	n-channel	49	28
B	n+/p-well	n-channel	25	20
C	n+/p-well	n-channel	12.25	14
D	n+/p-well	n-channel	6.25	10

Table 5.3 Test Pixels 2 Parameters

5.2.4. Test Pixels 3

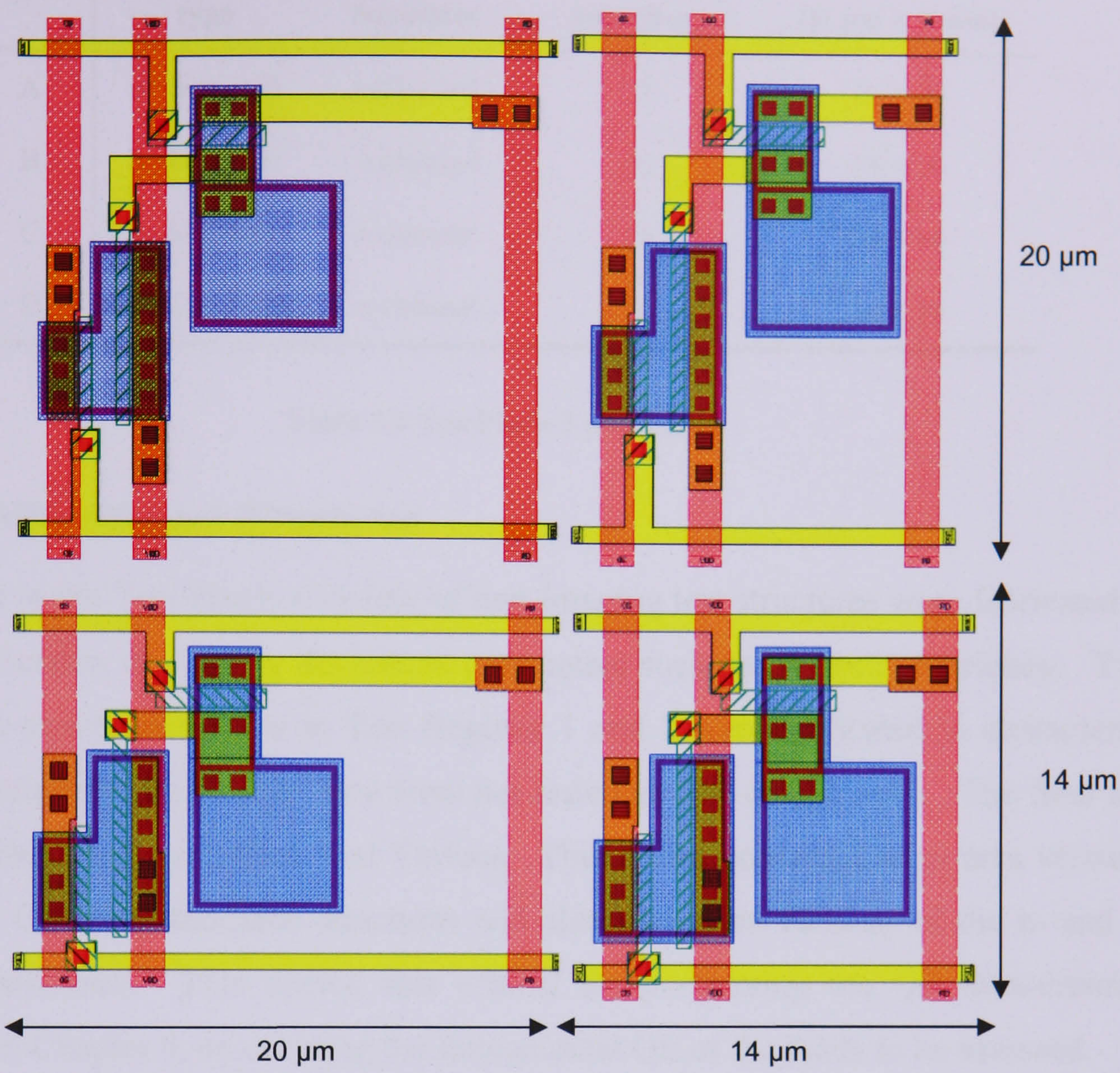


Figure 5.5 CAD schematic of the pixel design in each quadrant of Test Pixels 3. The device was intended to investigate the effect of pixel shape and size

Test Pixels 3 was designed to investigate the effects of changing the shape of the pixel. It consists of four 5 × 5 pixel arrays with different pixel dimensions, as shown in **Figure 5.5**. All pixels have n+/p-well photodiodes and n-channel reset transistors, and a 25 μm^2 photodiode. The details of each array are outlined in **Table 5.4** below. The change in dimensions requires the layout of the readout circuit to be adjusted slightly. Only a minimal amount of characterisation of Test Pixels 3 was performed due to the direction the experimental work took. A description of the device is included here for completeness.

Block	Photodiode type	Reset transistor	Photodiode area (μm^2)	Pixel dimensions (H μm × V μm)
A	n+ in p-well	n-channel	25	20 × 20
B	n+ in p-well	n-channel	25	14 × 20
C	n+ in p-well	n-channel	25	20 × 14
D	n+ in p-well	n-channel	25	14 × 14

Table 5.4 Test Pixels 3 parameters

5.2.5. Additional Test Structures

In addition to the Test Pixels a variety of non-imaging test structures were fabricated to aid quantification of foundry dependent parameters such as quantum efficiency. Two further test structures known as Test Register 1 and 2 were fabricated to characterise digital circuit performance but they were not tested as part of this work. The final test structure fabricated was called Test Various. This device contained large area versions of the two CMOS photodiode structures and also large area versions of the n- and p-channel transistors. This device was critical for performing the QE measurement described in Chapter 8, by enabling the fundamental QE of the diode to be assessed.

5.3. Test Pixels drive electronics

Operation of the CMOS Test Pixels required a system of drive electronics to provide timing signals, bias voltages and analogue data capture. A drive electronics board previously developed for real-time CCD data processing was adapted for this purpose. Test Pixels 1, 2, and 3 can be operated in a relatively simple fashion. The timing diagram for operation is shown in **Figure 5.6**. The device is powered by a single 5 V supply, V_{DD} with R-C filtering. The three other biases required are, V_{SS}, V_{RD} and V_{LG}. Once these biases are initialised, a global reset pulse is applied to either the n-channel reset arrays via $ØR_N$, or to the p-channel reset arrays via $ØR_P$. The n-channel reset pixels are reset by pulsing $ØR_N$ high (5 V) and the p-channel reset pixels are reset by pulsing $ØR_P$ low (0 V). When the reset pulse is applied all pixels are connected to V_{RD} and the photodiodes within each pixel are charged to the reset level. When the reset pulse is released the pixels will discharge due to leakage current and illumination until the next reset is applied. There are two approaches to allow sampling of the output.

The entire reset and integration process for a row of pixels can be sampled onto the column outputs (V_{OS1-10}) by holding row select ($ØRS_{1-10}$) high (5 V) for a particular row for the duration of the operation. In this way it is possible to observe the charging and discharging of each pixel individually and compare the behaviour of each pixel during this process in particular when using an oscilloscope for data acquisition. Alternatively the row select can be pulsed. There are advantages and disadvantages to both approaches, which are described in more detail in Chapters 6 and 7.

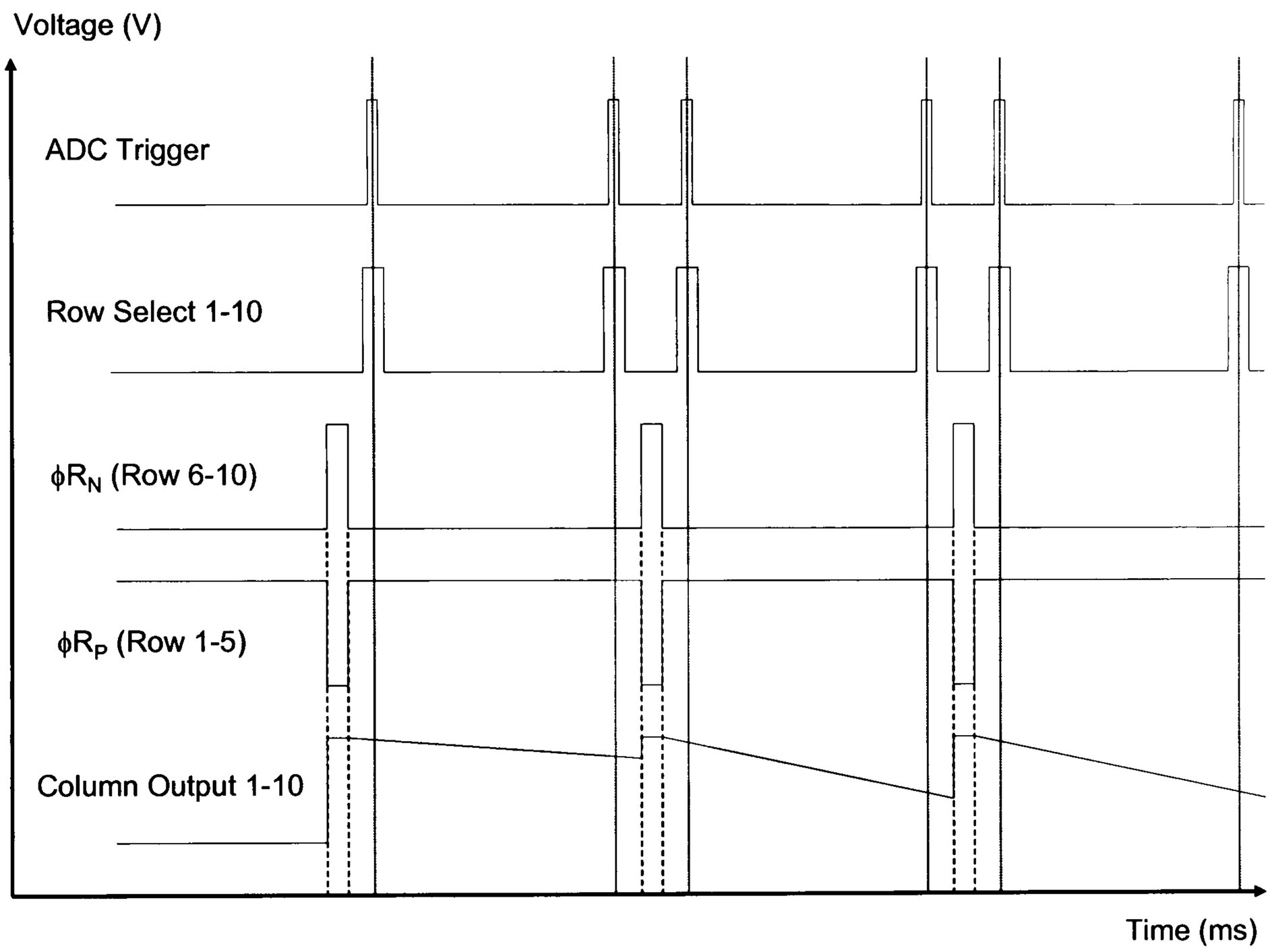


Figure 5.6 Test Pixels timing diagram. The basic timing signal required is the global reset pulse, $ØR_N$ for the n-channel pixels and $ØR_P$ for the p-channel reset pixels

5.3.1. Headboard

A headboard is required to interface the Test Pixels to the drive electronics system. A custom printed circuit board (PCB) was designed and manufactured for this purpose, and shown in **Figure 5.7**. A block diagram of the headboard is shown in **Figure 5.8**. The headboard consists of a 28 pin zero-insertion-force dual-inline-package (ZIF DIP) socket for easy insertion and removal of test devices, to reduce the possibility of damage to pins. Row selection pulses are passed to the APS using a 16-channel analogue multiplexer with four address inputs and sixteen independent outputs. This

reduces the number of row select signals required from the DSP from ten to four, and simplifies the programming process. Row selection pulses are controlled by a four bit binary code. It is only possible to select one row at a time with this configuration. The biases V_{DD}, V_{SS}, V_{LG} and V_{RD} to the APS are directly connected from the headboard to standard lab power supplies. Decoupling capacitors are used to filter the supply. The other inputs to the APS from the headboard are the two global reset pulses. All ten outputs from the APS ($V_{OS1\text{-}10}$) have their own individual gain stages to enable simultaneous sampling of multiple outputs into an oscilloscope or multi channel ADC card. From the output onwards, two different headboards were produced. The first version had no further signal processing so that the raw output could be observed directly with an oscilloscope. The second headboard had three amplifying stages. Each output was first connected to an ac coupling capacitor. After this there was a digitally controlled clamp to clamp the output to ground. The first gain stage was then implemented after this. The first gain stage consisted of an AD829 low noise video operational amplifier configured to provide a gain of 3. The second gain stage also used an AD829 op amp but was digitally programmable from the DSP through the use of a 4-channel analogue multiplexer. This enabled a gain of 1, 2, 4 or 8 to be set. The final gain stage also consisted of an AD829 op amp to provide an inverting gain of 2 and also an offset adjust. The inverting gain was used so that the output from the pixel ramps up rather than down. The offset adjust was used to tune the output range so that it was aligned with the 0 to 2.5 V input range of the ADC.

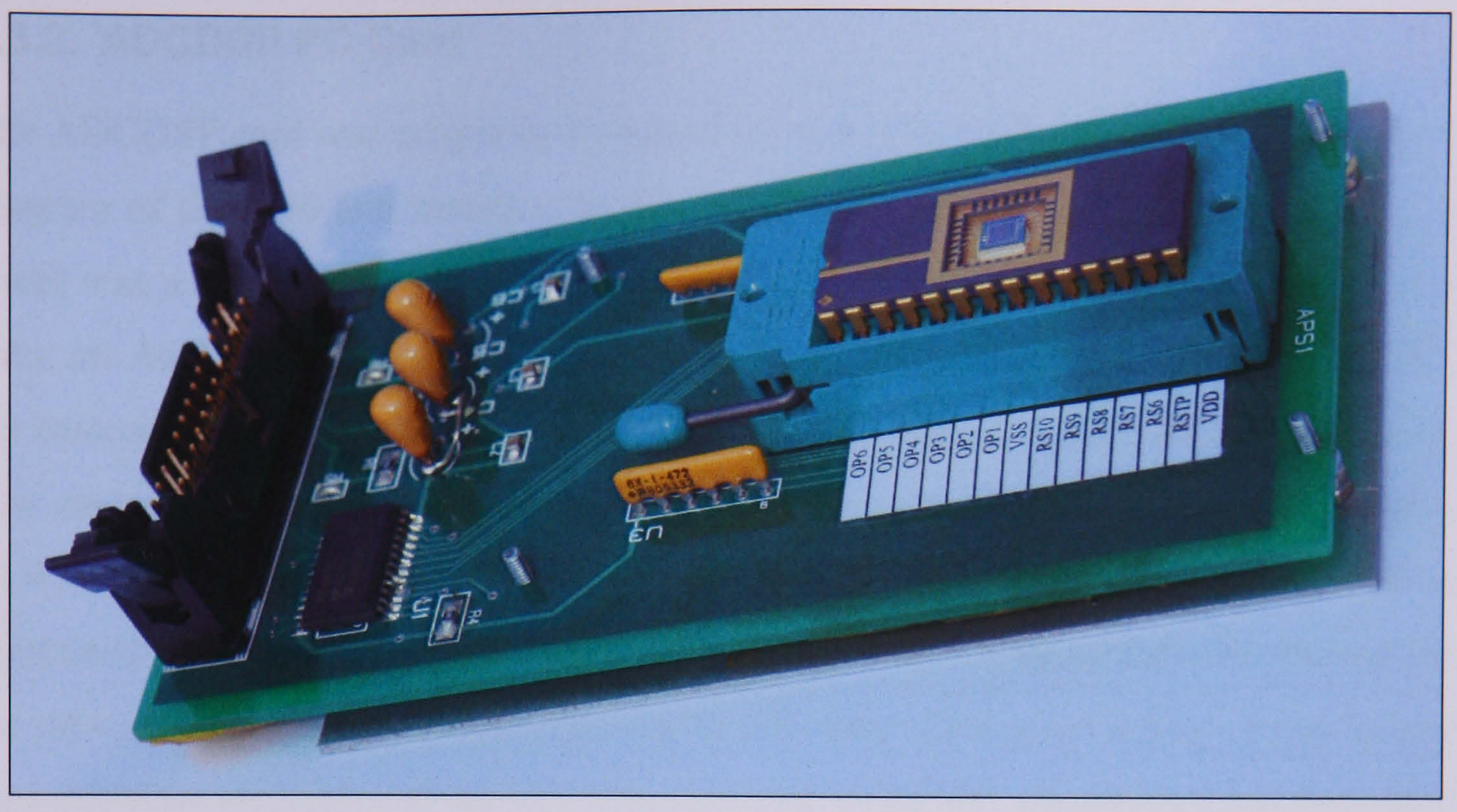
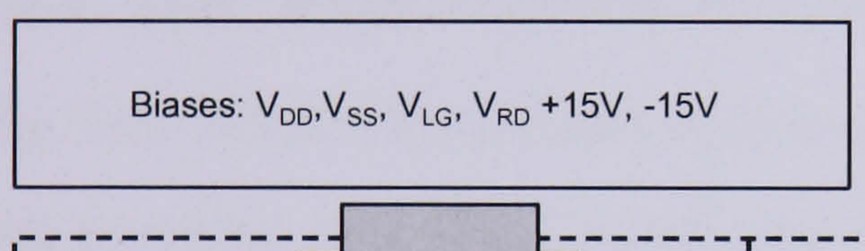


Figure 5.7 Test Pixels headboard



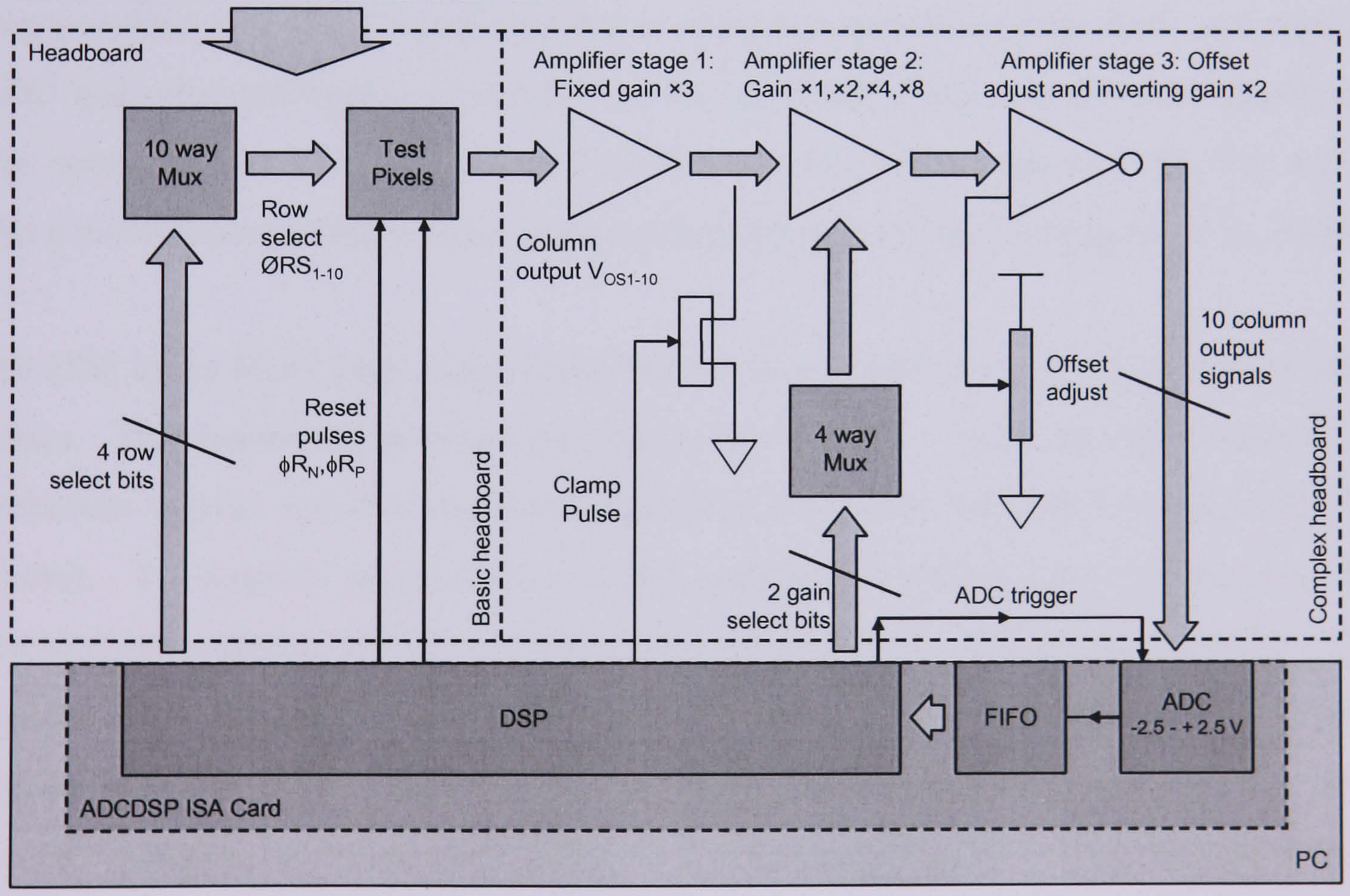


Figure 5.8 Test Pixels headboard block diagram showing versions with and without signal processing

5.3.2. ADCDSP PC Card

The ADCDSP card was originally designed for real time CCD data processing. A block diagram of the card and interface to the APS headboard is shown in **Figure 5.8**. The board was a 16-bit PC ISA bus expansion card. The primary components on the board were an Analog Devices ADSP2181 DSP (Analog Devices, 1998) operating at 50 ns per instruction and an Analog Devices AD1671 1.25 MHz 12-bit ADC. Analogue data was captured by the ADC, which was triggered by the DSP. The input range of the ADC was restricted to 0 - 2.5 V uni-polar input or ± 2.5 V bi-polar input, which was selectable with a jumper switch on the expansion board. Digitised data was passed from the ADC to the DSP data memory via a 12-bit wide 4096 word FIFO. From here the data could be processed by the DSP, or retrieved by the PC via the ISA bus through the use of a simple Visual Basic program.

5.3.3. DSP programming and sequencing

The Test Pixels drive electronics system was built around the ADSP2181 DSP. This chip provided all control signal required to sequence operation of the APS, and also the ADC and other interfacing electronics on the ADCDSP board and the APS headboard. The operation of the DSP was controlled by sequence files written as a .dsp file, which was a text file containing a series of programming instructions (Analog Devices, 2004).

The DSP had a 16-bit high-speed digital output port which was used to output 5 V logic pulses. The desired bit pattern was obtained by writing a 16-bit binary number to an arithmetic register and then instructed this bit-pattern to be passed to the output port, IO (Port0). To simplify programming of the register the patterns were written in 4-bit hexadecimal number and then converted by the DSP into a 16-bit binary code. The register AY0 was used to record the series of "bits" to be turned on. The arithmetic register was then used to combine this bit pattern with any previous pattern. By using the OR function, no other bit is turned off. This is demonstrated by the sub-routine named "resetnhigh" shown below:

```
resetnhigh:AY0=0x0008;          {Sets the N-channel reset to HIGH level}
AR=AX0 OR AY0;
IO(Port0)=AR;
AX0=AR;
RTS;                                        {Return to main program}
```

A similar principle was used to turn a given bit off, without affecting any other bits on the output port. In this case the AND function was used in conjunction with the inverse of the bit pattern which was required to be turned off. This is demonstrated by the following sub-routine named resetnlow:

```
resetnlow:AY0=0xFFF7;          {Sets the N-channel reset to LOW level}
AR=AX0 AND AY0;
IO(Port0)=AR;
AX0=AR;
RTS;                           {Return to main program}
```

This method was used to generate a sub-routine to turn individual bits on or off. If no further instructions were received by the DSP then the output port would remain in that state. If a delay was required in order to hold a given bit pattern for a certain time period, a no operation (NOP) was used in conjunction with a counter loop to generate a timer delay. As the clock speed of the DSP is 20MHz, the number of required NOPs for a given delay time must be in multiples of 50 ns. The subroutines generated to create a reset pulse width delay and integration time delay are shown below:

```
delaywid: CNTR=DM(ddelaywid);  {Reset Pulse Width Delay}
DO loop3 UNTIL CE;
    loop3:NOP;
RTS;

delayint: CNTR=DM(ointloop);   {Outer Integration Time Delay loop}
DO intloop1 UNTIL CE;
        CNTR=DM(iintloop);     {Inner Integration Time Delay loop}
        DO intloop2 UNTIL CE;
        intloop2:NOP;
intloop1:NOP;
RTS;
```

The counter values ddelaywid, ointloop and iintloop were stored in the memory of the DSP. A function was written in the VB code to receive a real time delay (in µs, ms, s etc) from the user and convert it into the correct parameters and write those values to the DSP memory to give the correct delay time. The above subroutines were then called in a further series of loops to create the required pattern to control readout of the device. An example DSP program, to recreate the sequence and data acquisition previously illustrated in **Figure 5.6**, is shown below:

```
resetloop: NOP;                {Main loop to read in APS data}

CALL resetnhigh;               {Switch on n-channel reset}
CALL delaywid;                 {Call pulse width delay}
```

```
CALL resetnlow;                {Switch off n-channel reset}
CALL trighigh;                 {Switch on ADC trigger ADC}
CALL triglow;                  {Switch off ADC trigger}
CALL delayint;                 {Integration time delay}
CALL trighigh;                 {Switch on ADC trigger ADC}
CALL triglow;                  {Switch off ADC trigger}
CALL delay;                    {Short delay before next reset}

JUMP resetloop;
```

This .dsp file was then compiled into a .dex file machine code. When operation of the DSP was required, the .dex file was loaded into the DSP's internal memory by the PC using a dynamic link up library (.dll) called by a Visual Basic program. Once the DSP was loaded it ran autonomously and required no attention from the host PC. Action was only required when data acquisition was necessary.

5.3.4. Oscilloscope data acquisition

In addition to the previously described data acquisition methods, two oscilloscopes were used to characterise the output voltage waveforms from the Test Structures. The two devices used were a Tektronix TDS2014 and a LeCroy Waverunner 6050. These oscilloscopes were used to perform some of the measurements described in Chapters 6 and 7.

5.4. CMOS Imaging Arrays

In order to characterise the imaging performance of a larger scale device, two medium sized imaging chips were fabricated, known as CMOS001 and CMOS002.

5.4.1. General architecture

Both devices feature an array of 144 × 144 pixels in total, of which the central 128 × 128 pixels are photosensitive. These dimensions were primarily set by the fact that the existing set of design tools could only produce designs of ~ 100k transistors. A floor plan of the sensors is shown in **Figure 5.9** and a circuit schematic is shown in **Figure 5.10**. The total imaging area is area 2.56 × 2.56 mm. The devices were packaged in a 28 pin, 0.6" pitch, dual-inline (DIL) ceramic package. Each pixel in the imaging area is the same 3T read-out and sensing arrangement used in the Test Pixels. Each pixel is 20 μm × 20 μm and contains a square photodiode with a surface area of 100 μm^2 to maximise the pixel fill factor. The non-photosensitive pixels are provided for dark reference purposes and have no photodiode or reset transistor. The gate of the source follower transistor is permanently connected to the V_{RD} level. The arrays are addressed with reset and readout controlled by horizontal and vertical shift registers described in Chapter 4. The connections to the devices are summarised in **Table 5.5** and the specific details of each imaging array are given in the following sub sections.

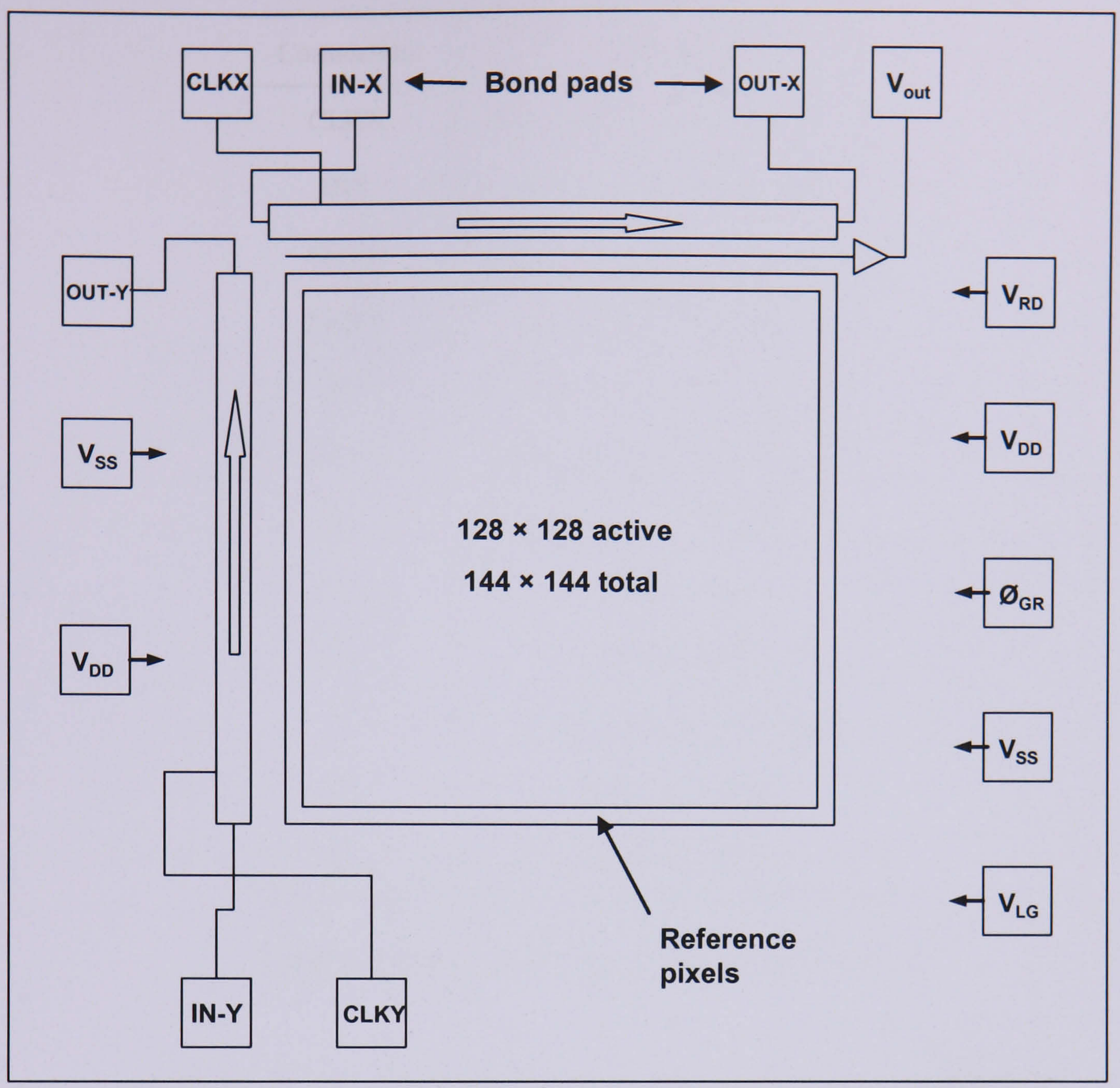


Figure 5.9 Imaging Arrays sensor floor plan

Connection	Description
CLKX	Horizontal (X) shift register clock
INX	Horizontal (X) shift register input
OUTX	Horizontal (X) shift register output
CLKY	Vertical (Y) shift register clock
INY	Vertical (Y) shift register input
OUTY	Vertical (Y) shift register output
$Ø_{GR}$	Global reset (for CMOS002)
V_{out}	Array output
V_{DD}	Supply voltage
V_{LG}	Column load gate voltage
V_{RD}	Reset drain voltage
V_{SS}	Substrate voltage

Table 5.5 Imaging Arrays pin connection descriptions

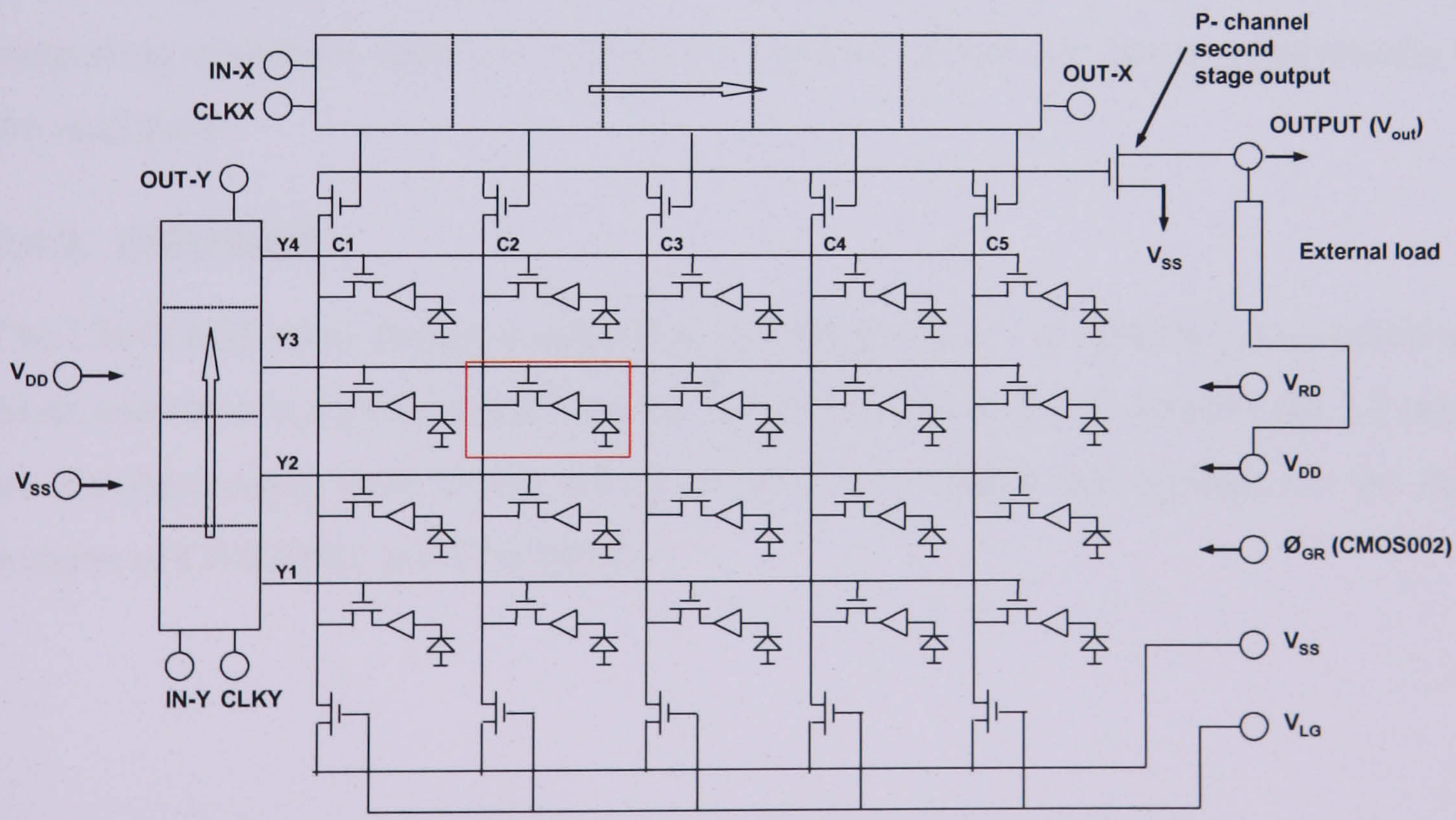


Figure 5.10 Imaging Arrays circuit schematic (reference pixels not shown)

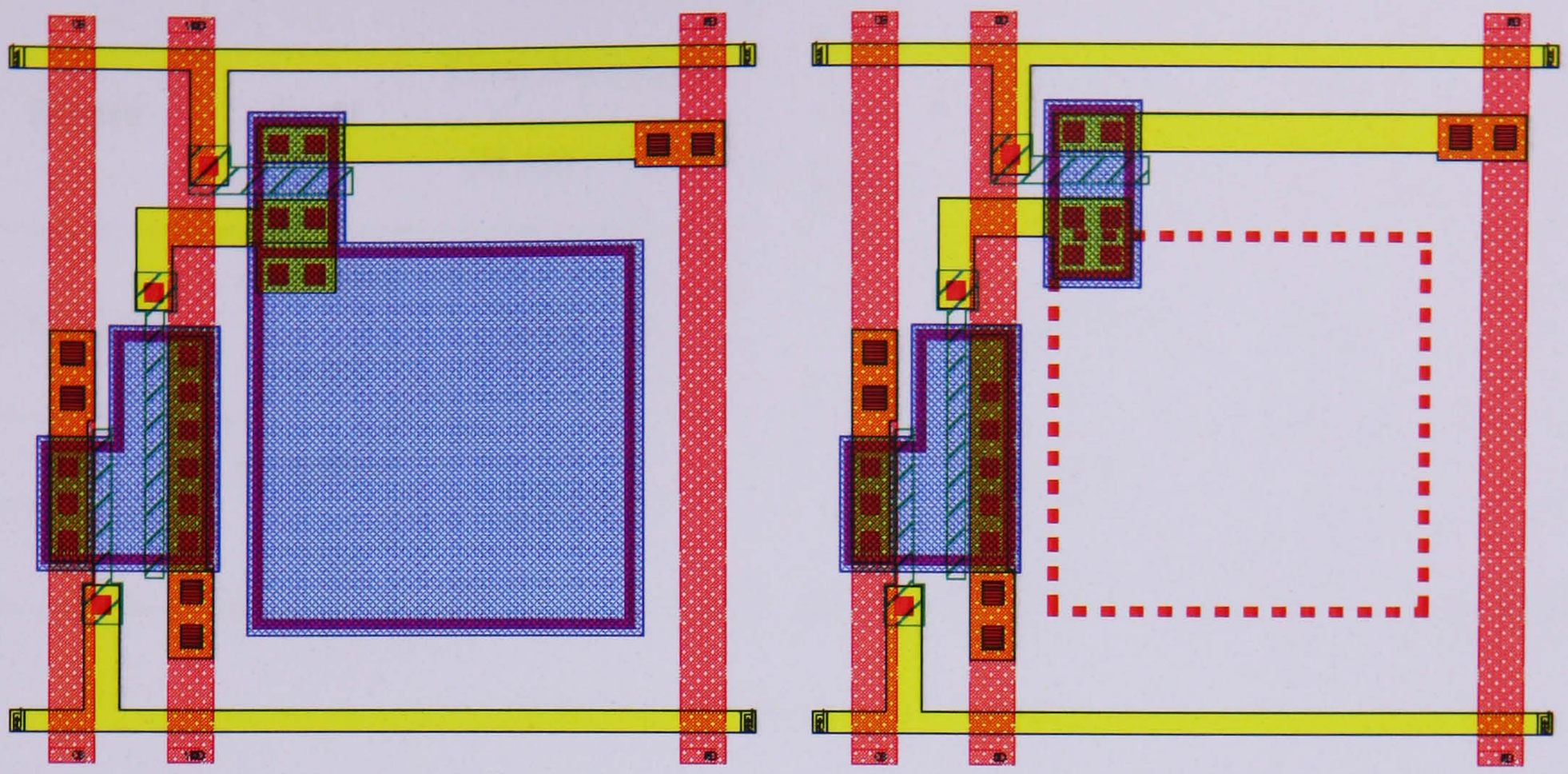


Figure 5.11 CAD schematic of CMOS001 pixel (left) and 002 pixel (right)

5.4.2. CMOS001

The main features of the CMOS001 pixel are illustrated in **Figure 5.11**. The device has an n+ in p-well photodiode in each pixel and is operated in a raster scan reset fashion. The reset transistors in each row are connected to the row select shift register of the row below. Therefore, as an individual row is selected the previous one is reset and integrating whilst the next row is read-out. This simplifies the layout requirements for the reset pulse.

5.4.3. CMOS002

The CMOS002 pixel design is also shown in **Figure 5.11**. It contains an n-well/p-sub diode and there is a global reset function. Therefore when $Ø_{GR}$ is pulsed high, all pixels are simultaneously reset to the reference level V_{RD}. **Table 5.6** summarises the main features of CMOS001 and CMOS002.

Device	Reset	Pixel dimensions (H µm × V µm)	Pixel area (μm^2)	Photodiode type	Photodiode area (μm^2)	Fill factor (%)
CMOS001	n-channel raster	20 × 20	400	n+/p-well	100	25
CMOS002	n-channel global	20 × 20	400	n-well/p-sub	100	25

Table 5.6 Imaging Arrays summary

5.4.4. Sequencing requirements

The sequence required for the imaging arrays is more complex than for the Test Pixels. A timing diagram for the devices is shown in **Figure 5.12**. Each shift register requires a clock input that is converted to a two-phase clock onboard the chip, and a trigger signal to commence readout of each row/line. For each shift in the vertical (Y) shift register, the horizontal (X) shift register must shift 144 times to read out the entire row. Therefore, the master clock (nominally 1MHz) should be input to CLKX. OUT-X can potentially be used as the trigger for IN-Y.

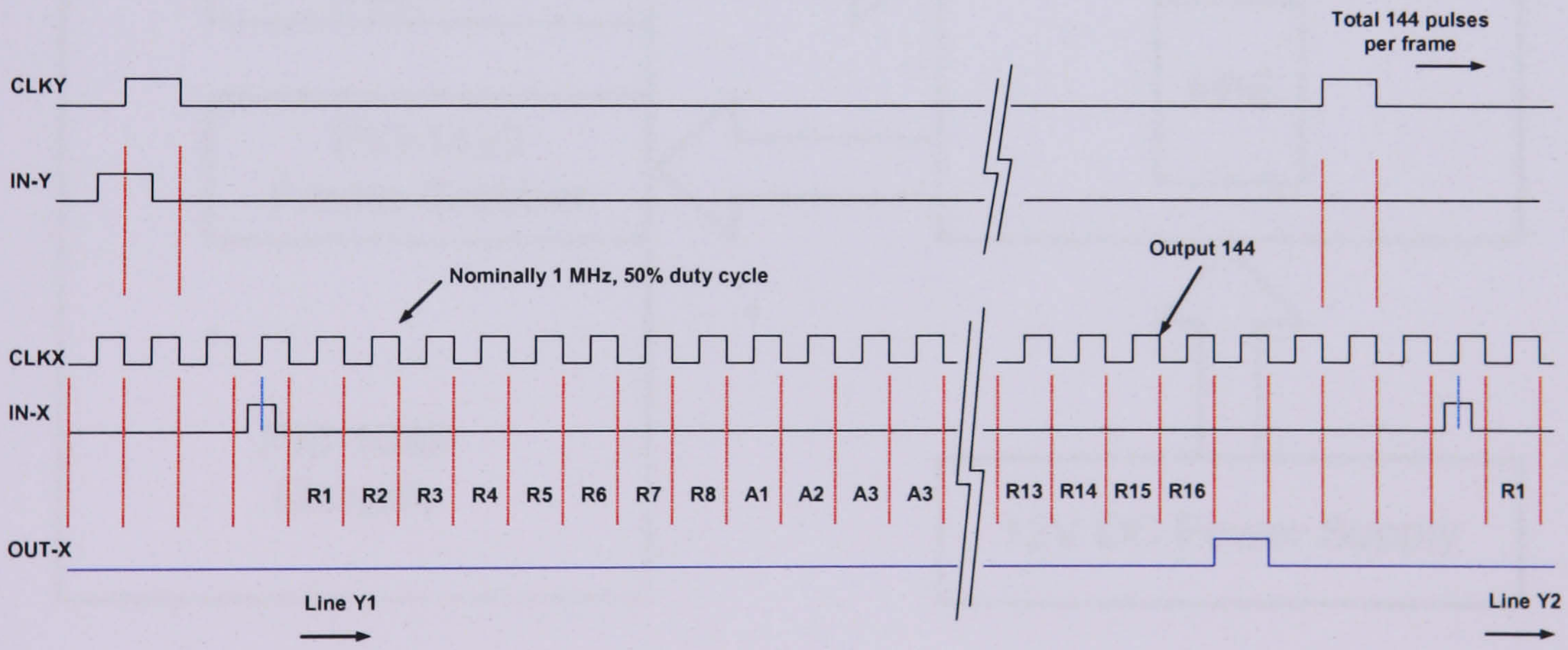


Figure 5.12 Imaging Arrays timing diagram. All pulses are 5V CMOS levels. (Note CMOS002 requires an extra single global reset at the beginning of the frame integration)

5.5. Imaging Arrays drive electronics

Engineers at e2v technologies developed the Imaging Arrays drive system. It comprises three components and is shown in **Figure 5.13** below. The system consisted of a

Microsoft Windows based PC, a National Instruments PXI-1042 chassis, power supply and the APS headboard PCB. The PXI 1042 chassis acted as an expansion of the PCI bus of the PC. Data was passed from the PC to the chassis via a high-speed copper connector. The PXI-1042 chassis contained three expansion cards, an MXI-4 communications module to facilitate communication between the chassis and the PC, a PXI-6561 high-speed digital I/O card to sequence the device, and a PXI-1422 frame-grabber to acquire image data from the APS headboard. The three cards were controlled using National Instruments LabView software. The high- speed digital I/O card and frame grabber were used to transmit and receive low voltage differential signals (LVDS). LVDS signals are used to enable accurate data transmission over long cable lengths.

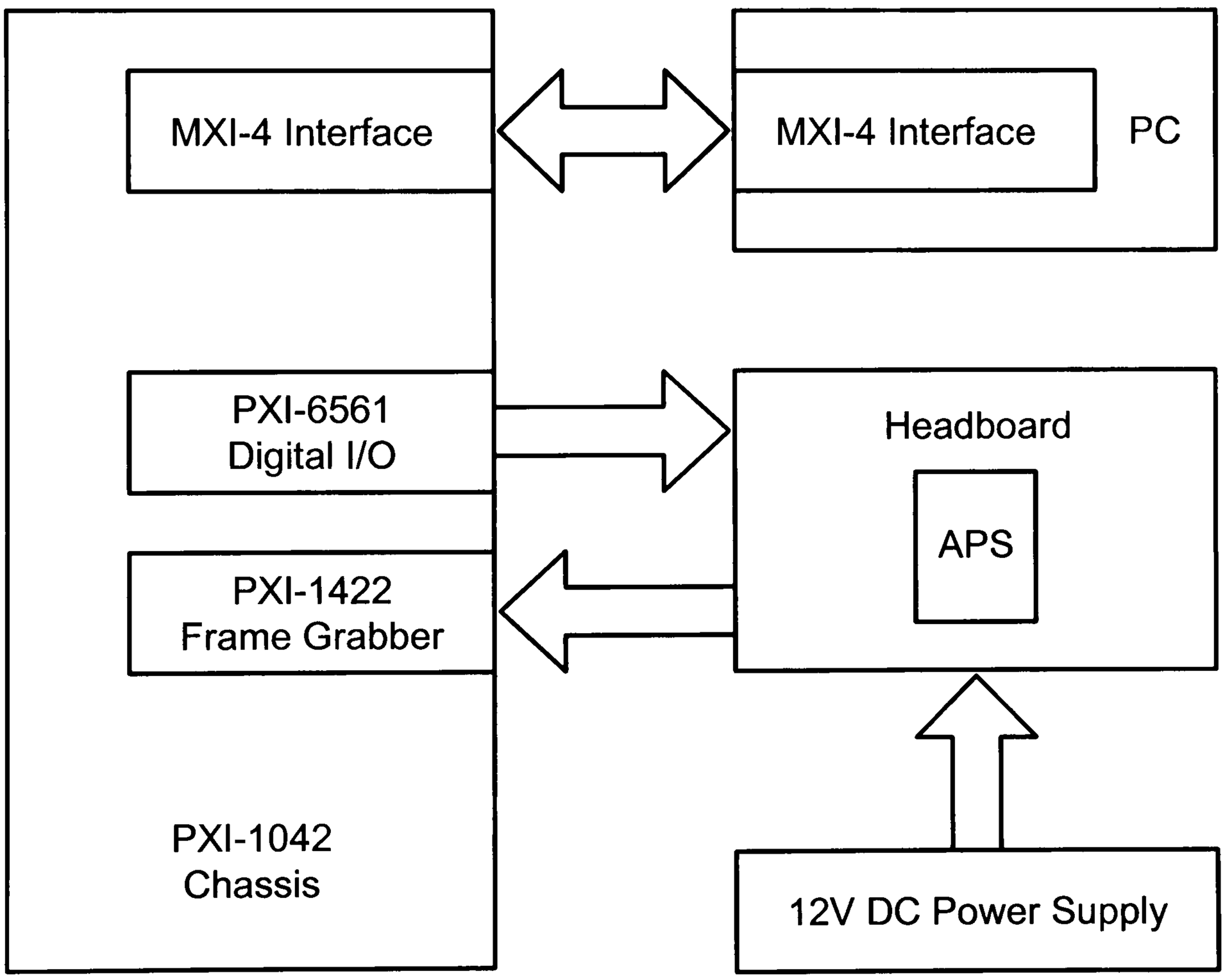


Figure 5.13 Block diagram of the Imaging Arrays drive electronics

5.5.1. Headboard

A block diagram of the Imaging Arrays headboard is shown in **Figure 5.14**. A photo of the headboard is shown in **Figure 5.15**. The bias supplies to the APS are derived from a single 12 V power supply. Control signals to sequence the APS are transmitted from

the high speed digital I/O as LVDS signals. After the headboard connector, the signals are converted by quad CMOS differential line receivers to the TTL/CMOS logic signals that are suitable for the headboard components. Signals are then routed to the various components on the headboard. The analogue output from the APS is AC coupled to a switchable ×2/×10 gain operational amplifier stage. This is AC coupled to a further low noise op-amp stage, then to a low noise voltage feedback-clamping amplifier. The final stage is a differential amplifier that converts the single ended signal to a differential signal suitable for input to the ADC. The analogue signal output from the fourth stage is converted to a digital number using a Texas Instruments 16-bit 1.25 MHz differential input ADC with an 8 V input range. A CMOS Differential Line Driver then converts back the TTL/CMOS logic signal output from the ADC to an LVDS signal for transmission to the National Instruments frame grabber.

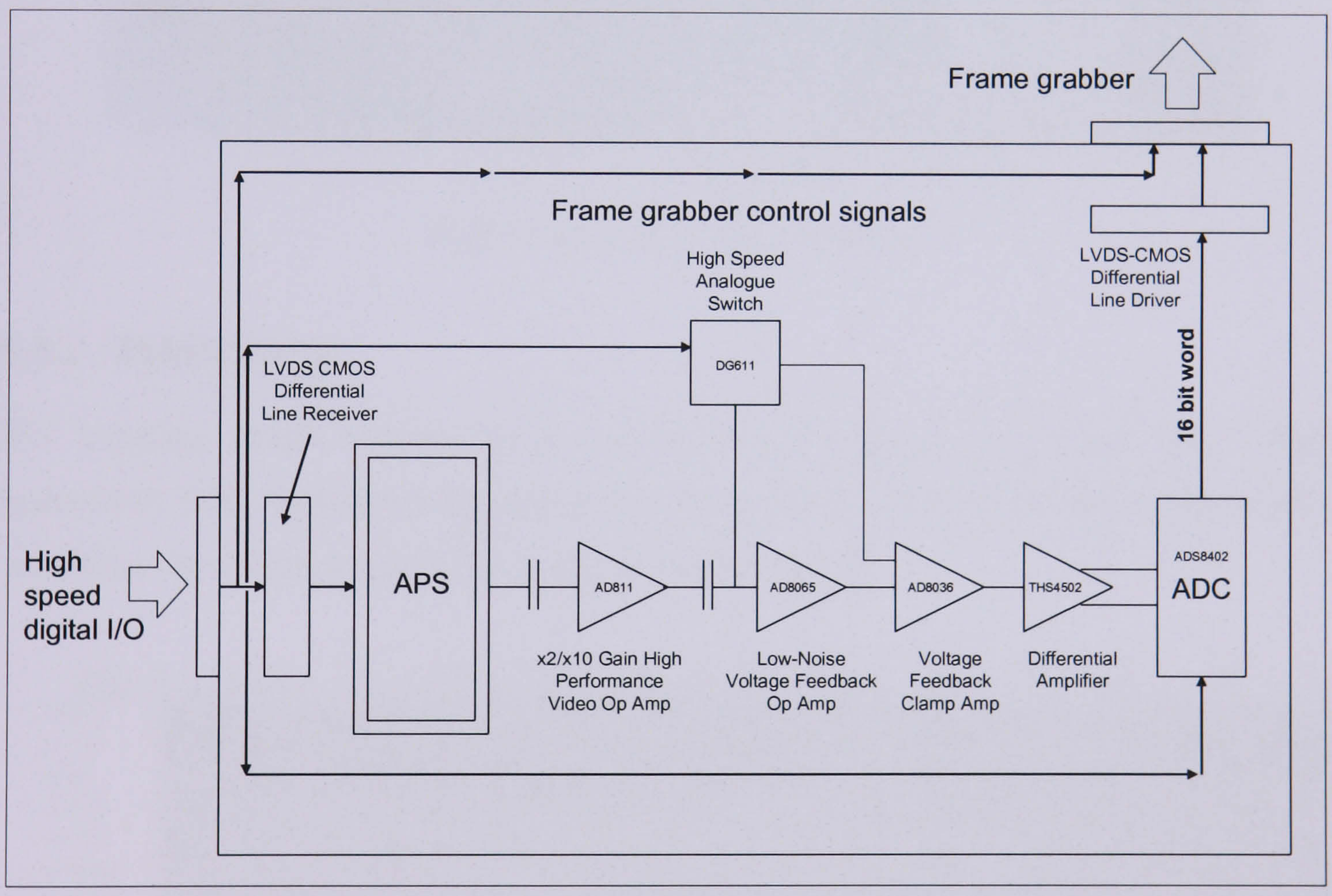


Figure 5.14 Imaging Arrays headboard block diagram

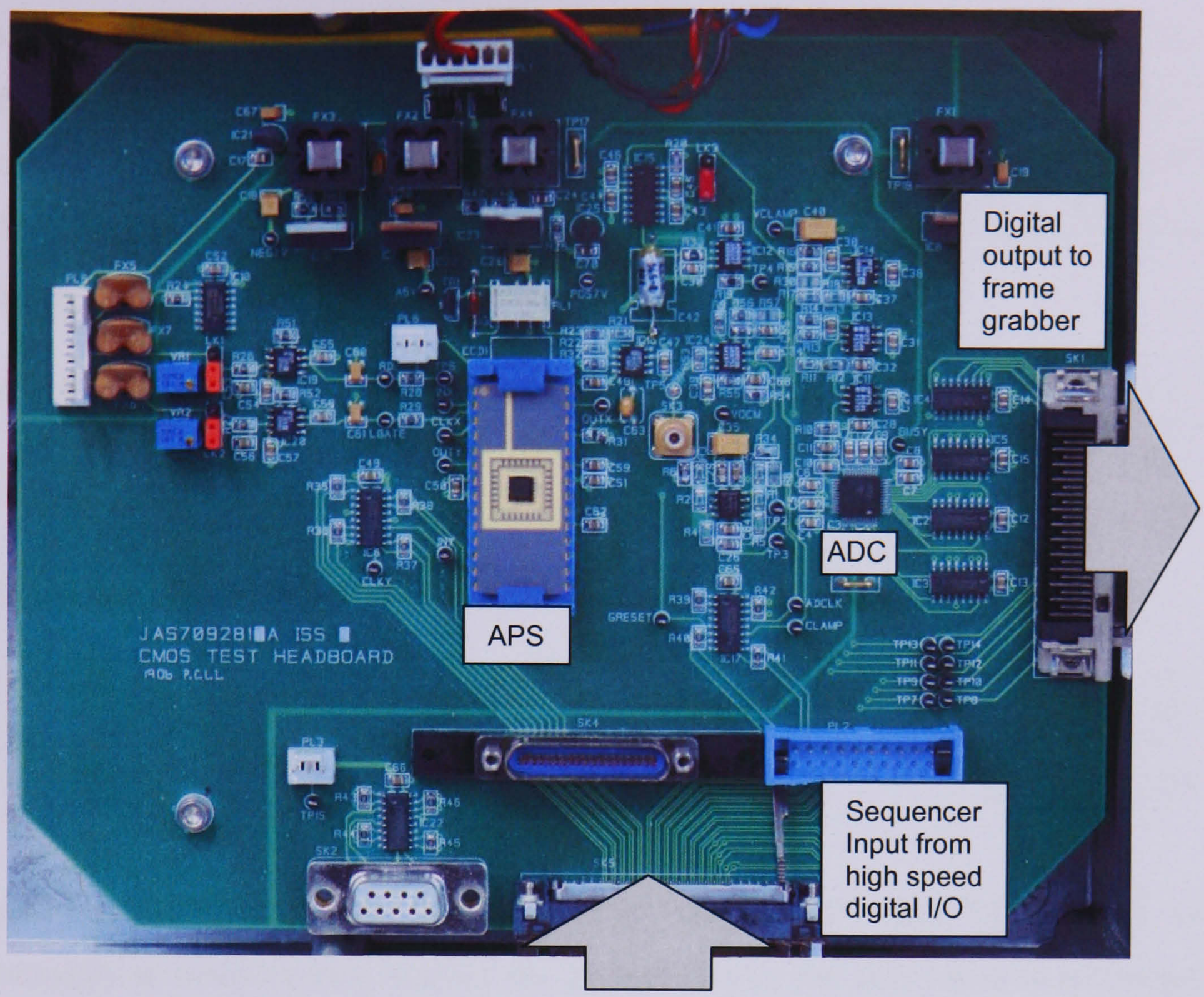


Figure 5.15 Imaging Arrays headboard

5.5.2. Sequencing

The imaging arrays sequencing is controlled with the use of a LabView Virtual Instrument (VI). Sequences are generated using the NI waveform editor and saved as .hws files. An example timer file is shown in **Figure 5.16**.

Figure 5.16 First 30 μs of clock timing for the first line of readout for CMOS001

Various timer files were generated to perform a particular function in a similar way to the sub-routines generated for the Test Pixels except the bit patterns are generated using

a visual interface. Each timer file is then selected by a script within the National Instruments VI to create a continuous loop required to read out the device. The script is then looped infinitely. Example scripts for CMOS001 and CMOS002 are shown below. For CMOS001 four timer files are required the number on the right hand side denotes the number of times a given timer file is repeated:

```
Integration                                    10
Blanking                                       100
FirstLine                                      1
LineTransfer                                   143
```

CMOS002 requires one additional timer file to perform the global reset:

```
Integration                                    10
Blanking                                       100
FirstLine                                      1
LineTransfer                                   142
LastLine                                       1
```

The sequence is loaded onto the high-speed digital I/O card, which then runs autonomously to continuously readout the device. When the user requires an image or series of images, the VI is used to acquire image data stored by the frame grabber card memory. It is then displayed and saved for analysis by the user.

5.5.3. Temperature controlled characterisation

The CMOS cold characterisation facility was used to control the temperature of the Imaging Arrays within the range -100 °C to +60 °C. A block diagram and picture of the set-up are shown in **Figure 5.17** and **Figure 5.18** respectively. The facility was required to investigate temperature dependent parameters such as dark signal and reset noise. The sequencing system here is a modified camera system for CCD characterisation based around a Texas Instruments DSP. The system is placed in a high vacuum to prevent condensation and ice forming on the devices, which could be damaging. The APS sits on a dummy version of the headboard described in the previous section. All signals are interfaced to a second headboard outside of the vacuum chamber via a vacuum feed-through. The voltages are provided via an adapted CCD bias generator, and the sequencing pulses are generated by a DSP programmed in a similar way to the Analog Devices DSP described earlier. The system is more susceptible to noise because the analogue output must be passed along an appreciable length of cable to the second headboard on the outside of the chamber.

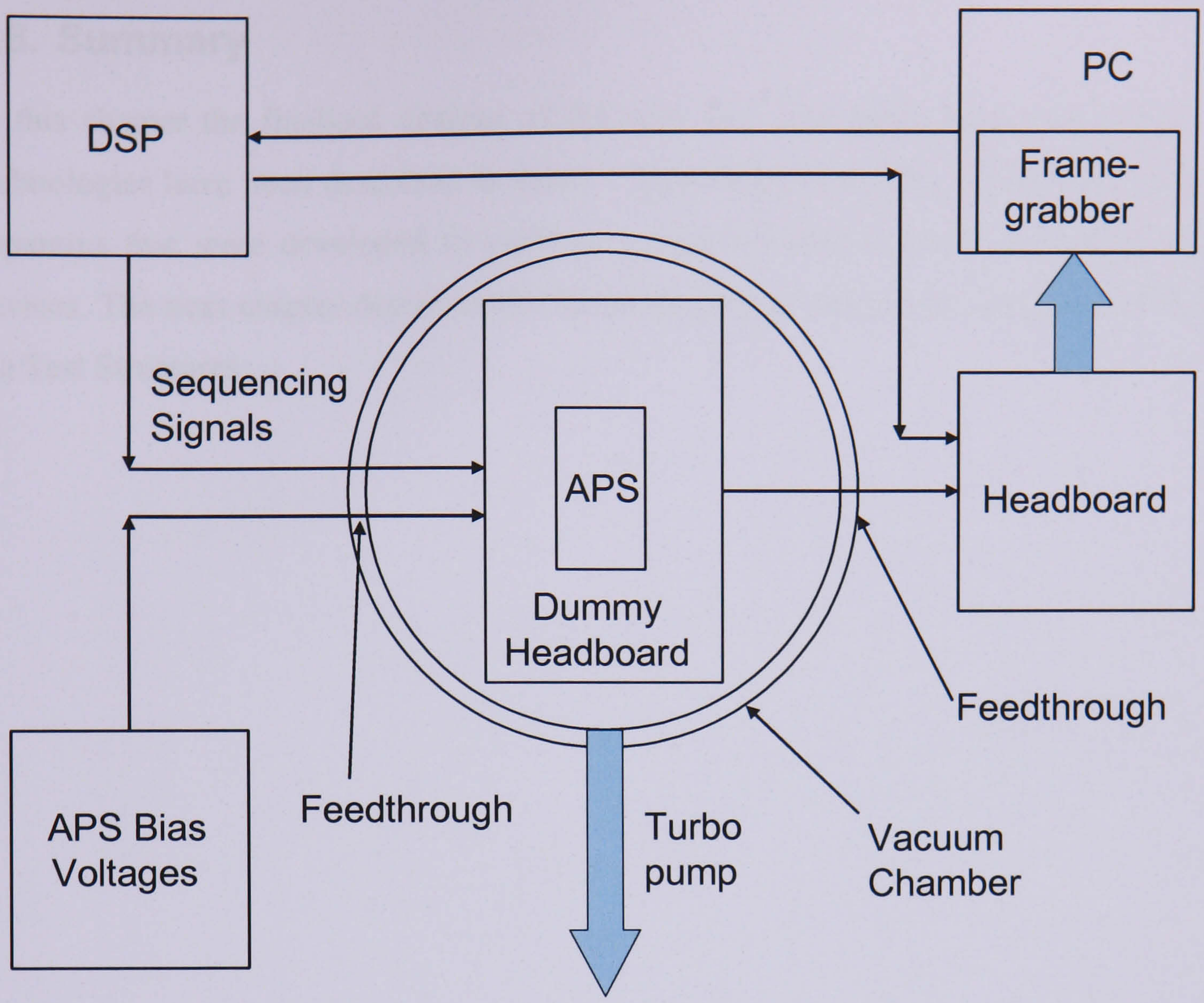


Figure 5.17 Imaging Arrays cold characterisation facility block diagram

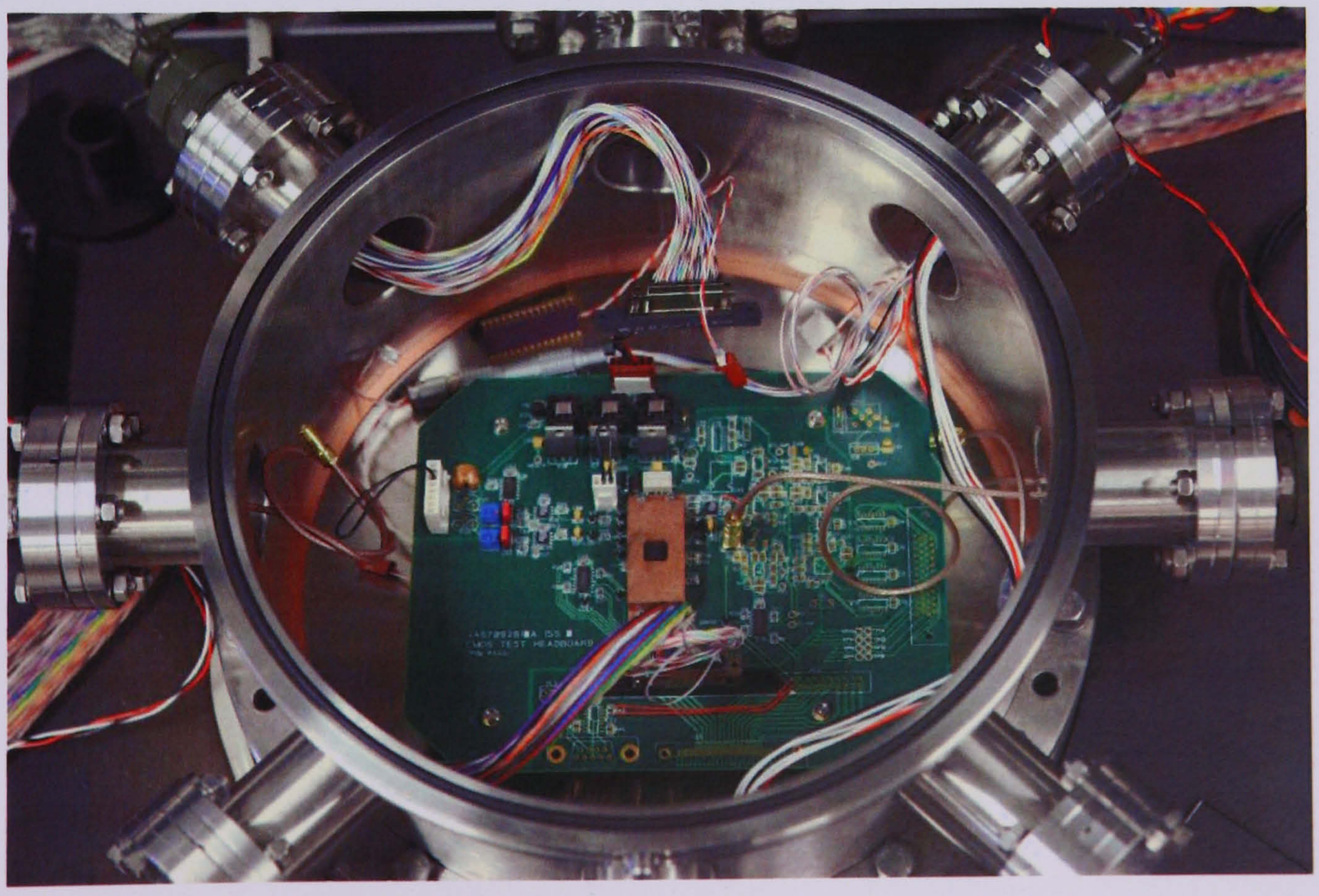


Figure 5.18 The Imaging Arrays cold characterisation facility at e2v technologies

5.6. Summary

In this chapter the finalised designs of the new Test Structures implemented by e2v technologies have been described in detail. This chapter has also outlined the various apparatus that were developed to perform a rigorous characterisation of the CMOS devices. The next chapter describes the initial functional testing and characterisation of the Test Structures.

Chapter 6: Initial electrical characterisation

Chapter 6 outlines an initial characterisation of the electrical behaviour of the Test Structures. The first section describes work performed with the Test Pixels to characterise responsivity, source follower gain and operating range. The second section describes a characterisation of the Imaging Arrays using the well-known mean-variance technique. The method was primarily used to measure the responsivity, read noise and node capacitance.

6.1. Introduction

The performance parameters used to describe an image sensor can be divided into the electrical characteristics such as dark signal and noise, and the electro-optical characteristics such as photo-response and quantum efficiency. Measurement of such parameters generally requires that the voltage change measured at the sensor output be related to the number of electrons collected within the pixel. Therefore, before any other measurements are made, one must quantify the responsivity in terms of $\mu V/e^-$. It is then possible to make further measurements such as node capacitance (fF), noise equivalent signal ($e^-_{r.m.s.}$), dark signal (e^-/pixel/s or nA/cm^2) and quantum efficiency (e^-/photon). The work described in this chapter primarily outlines two different approaches used to characterise the responsivity of the Test Structures. Before this, the first section of Chapter 6 describes some initial functional testing of the Test Pixels, which began with an investigation into the nature of the raw APS output waveform. This enabled understanding of the source follower gain, reset characteristics, operating range, and optimum biasing conditions. A novel technique was then used to perform responsivity measurements for the range of pixel designs. The second section of the chapter describes an investigation into the electrical properties of the Imaging Arrays using the mean-variance technique. This well known method was used to measure responsivity, noise, dynamic range and enabled calculation of node capacitance. The knowledge gained from this work enabled the further investigations into dark signal and quantum efficiency, which are described in Chapters 7 and 8.

6.2. Initial Test Pixels characterisation

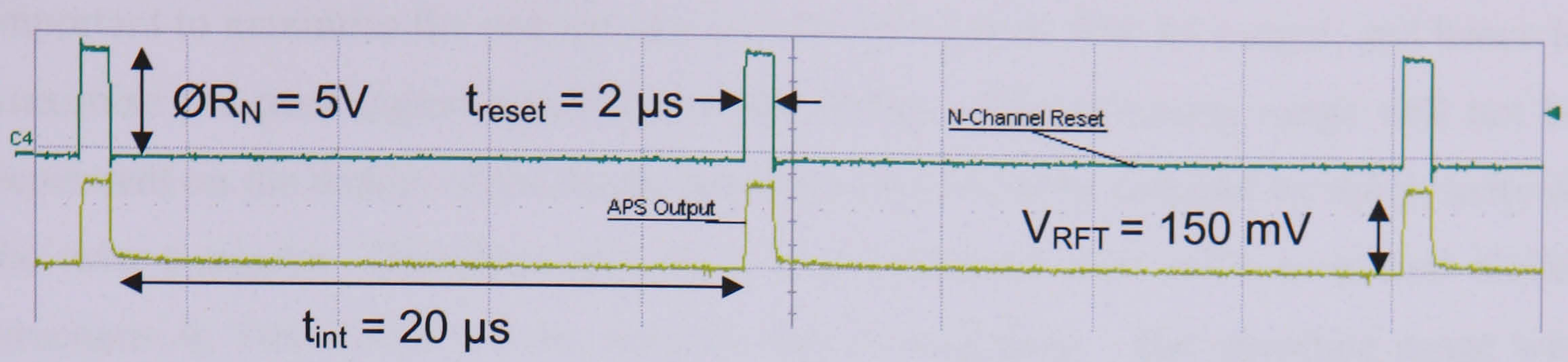
This section outlines a characterisation of the main features of the 3T pixel output waveform using the Test Pixels.

6.2.1. Functional testing

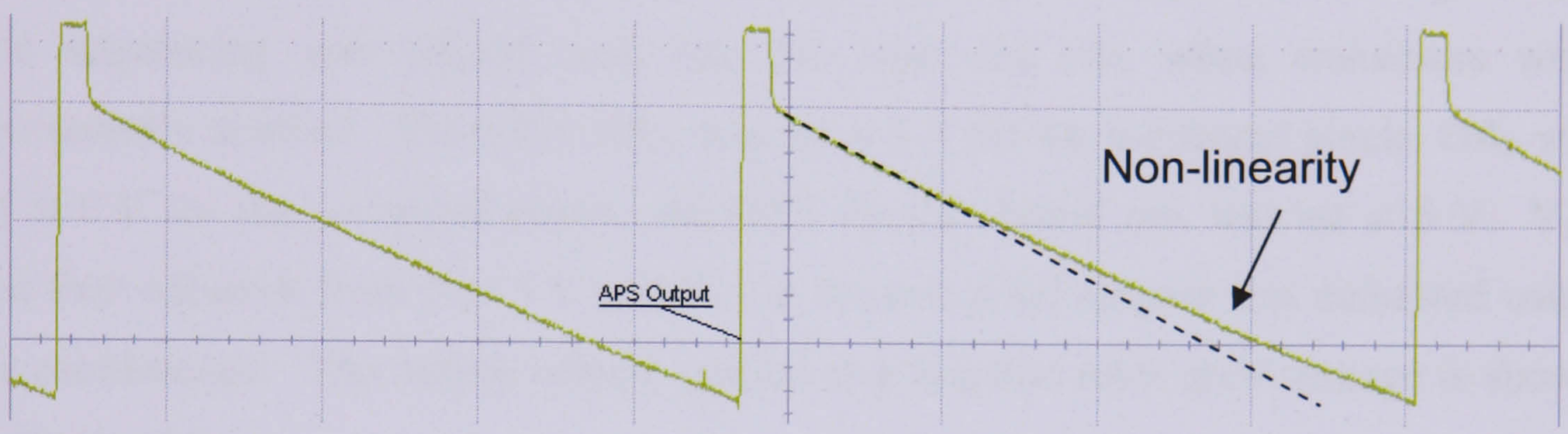
Initial characterisation of the Test Pixels was performed using the ADCDSP system described in Chapter 5. Test Pixels 1 was characterised first as this contained the same pixel structures encompassed within the two Imaging Arrays. The device was biased to $V_{DD} = 5$ V, $V_{RD} = 3$ V and $V_{LG} = 2.5$ V. The initial values were determined by the results of the simulations outlined in Chapter 4 to enable correct operation of the read-out circuitry. Test Pixels 1A, the n-channel reset with n+/p-well diode pixel was tested first as it had the same pixel design as CMOS001. The device was initially operated in darkness and was then illuminated at a range of intensities using a super-bright white LED. A reset time (t_{reset}) of 2 µs and integration time (t_{int}) of 20 µs were set using the sequencer code and the LeCroy oscilloscope was used to directly sample the pixel output.

The main features of the APS waveform under no illumination are shown in **Figure 6.1a**. When the pixel is reset the output rises to 3.3 V, which is 0.3 V greater than V_{RD} due to the offset introduced by the first and second stage source followers. After the reset transistor is turned off, the output voltage immediately decreases by 150 mV due to reset feed-through, which significantly reduces the available voltage swing at the node. Once the output has settled in darkness, it remains constant as expected because a negligible amount of dark signal is able to accumulate during the short integration time. The second output waveform, shown in **Figure 6.1b**, shows the pixel illuminated to approximately half of full well capacity by adjusting the LED brightness. After the output settles from reset feed-through the pixel output decreases as a combination of photo-generated and dark signal are accumulated by the diode. The output voltage change over time is non-linear despite the constant illumination level, which confirms the expected photo-response reduction as signal accumulates, due to the node capacitance increasing. The third output trace, shown in **Figure 6.1c**, shows the pixel under a brighter illumination such that it is saturated before reset. Under these conditions the output saturates at 2 V and the non-linearity is more severe.

a)



b)



c)

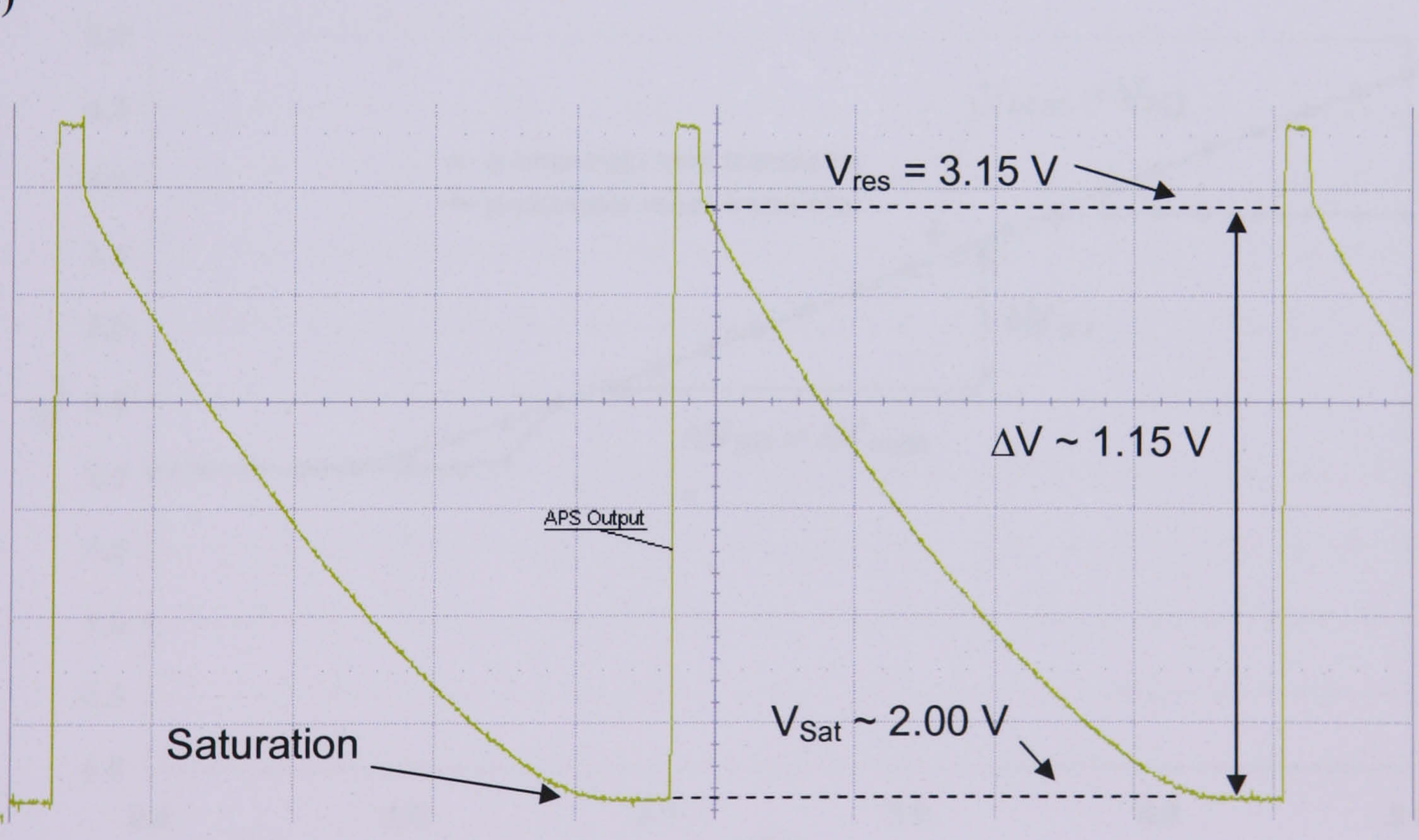


Figure 6.1 Pixel output waveform from Test Pixels 1. **a)** Under dark conditions, **b)** at half full well capacity and **c)** saturated. The key features are the reset feed-through, non-linear photo-response and saturation level

6.2.2. Pixel operating range

Knowledge of the effect of biasing and pixel design on the sensor operating range is important to maximise the voltage swing at the sense node and the output, and hence to maximise the peak signal capability of the device. The operating range will not be dependent on the design of the diode structures, but it can be affected by the polarity of the reset transistor. Therefore only the n- and p-channel reset (with n+/p-well diode) structures in Test Pixels 1 were used for this investigation. The operating range was investigated by varying the reset drain voltage (V_{RD}), which will be equal to the node voltage under correct reset operation, and observing the resulting output voltage (V_{out}). The sequencing was altered such that the reset and row select transistors were permanently enabled. Therefore $ØR_N$ was set at 5 V for the n-channel pixels, $ØR_P$ was set at 0 V for the p-channel pixels, and ØRS for the chosen row was set at 5 V. V_{RD} was then adjusted from 0 to 5 V and V_{out} at the two pixel outputs was measured using the oscilloscope. The output voltage plotted as a function reset drain voltage is shown in **Figure 6.2**.

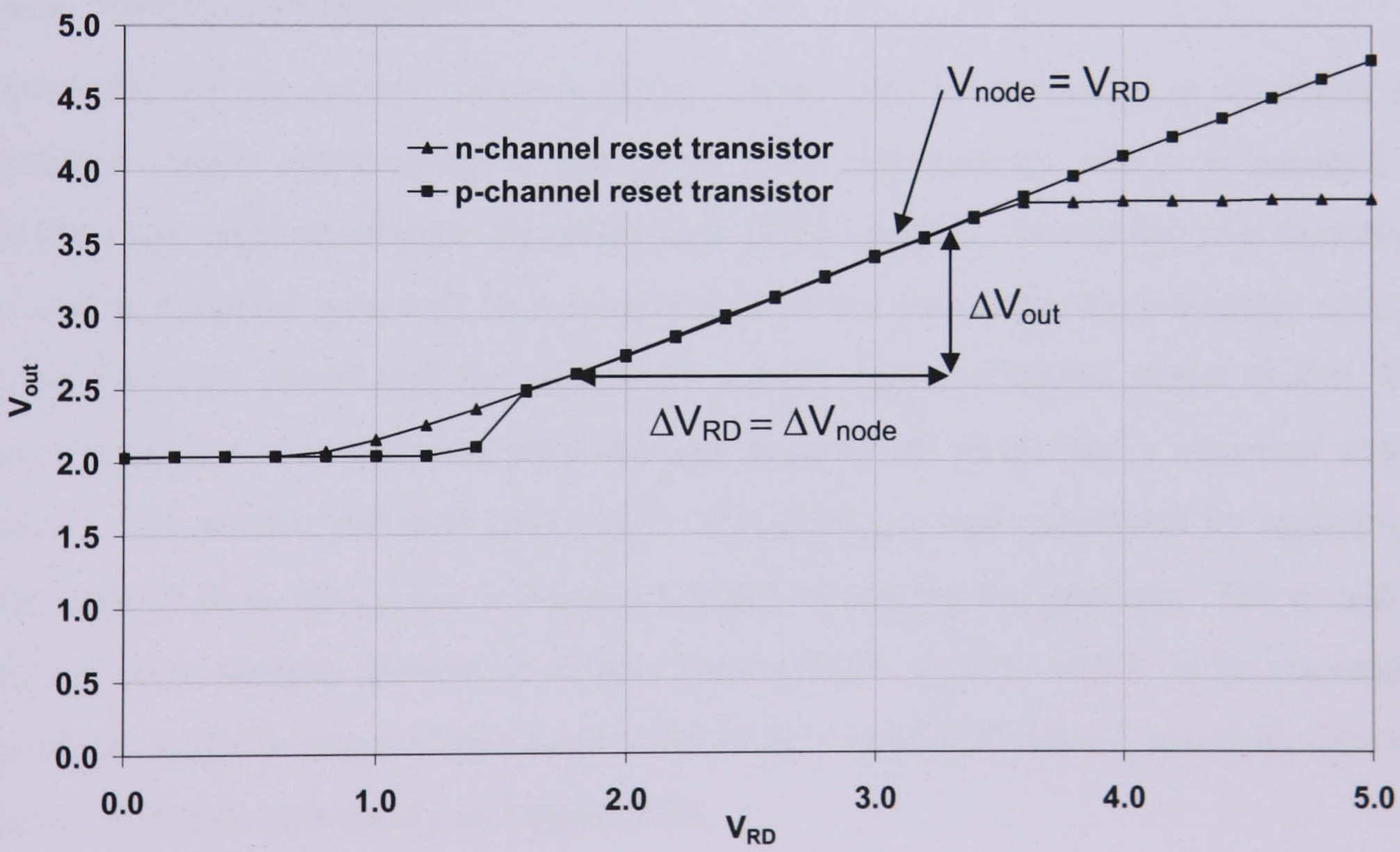


Figure 6.2 The operating range of the sensor for n- and p-channel reset with $ØR_N = 5$ V, $ØR_P = 5$ V, ØRS = 5 V and V_{RD} adjusted between 0 and 5 V. $V_{DD} = 5$ V, $V_{LG} = 2.5$ V

For the n-channel reset the output voltage saturates at 2 V as the reset drain is reduced below 0.8 V. This is due to the in pixel follower transistor turning off. The n-channel

reset behaviour is then seen to operate correctly only up to $V_{RD} = 3.5$ V, which corresponds to a maximum output voltage of $V_{out} = 3.75$ V. This corresponds well with the simulations described in Chapter 4 and occurs because the reset transistor is entering the sub-threshold regime and the pixel undergoes soft reset. V_{RD} for the n-channel reset pixels should always be set in the range 0.8 to 3.5 V to ensure correct pixel reset and output circuit operation. V_{RD} could be raised above 3.5 V, but this could introduce non-linearity problems associated with the soft reset. For the p-channel reset the output voltage also saturates at 2 V but the saturation occurs when the reset drain is reduced below 1.5 V. This was not expected but the behaviour may be due to the p-channel reset transistor entering the sub-threshold regime. The p-channel pixel resets correctly up to $V_{RD} = 5$ V, corresponding to a maximum output voltage of 4.8 V. This also agrees well with the simulations as the p-channel reset transistor does not enter the sub-threshold regime at the higher reset drain voltages. V_{RD} for the p-channel reset pixels should always be set in the range 1.5 to 4.8 V to ensure correct pixel reset and output circuit operation.

6.2.3. Output circuit gain

Knowledge of the source follower output circuit gain is important as it relates the measured output responsivity to the sense node responsivity, which is required to calculate the node capacitance described later in this chapter. For all the Test Structures the source follower gain will be a combination of the values for the n-channel column source follower circuit and the additional second stage p-channel output buffer. The gain should not vary between pixel designs because all pixels use a common output circuit. The source follower gain ($G_{SF} = \Delta V_{out}/\Delta V_{node}$) was calculated by applying a least squares fit to the curves in **Figure 6.2** and measuring the gradient. The n- and p-channel reset designs showed a similar gain of 0.68 ± 0.05, which is in reasonable agreement with the range of simulated values ($G_{SF} = 0.65$-0.85 for a 6 μm wide follower transistor) shown previously in **Figure 4.13**.

6.2.4. Column load behaviour

The behaviour of the column load transistors was investigated by varying V_{LG} (with a row selected) and measuring the current flowing between V_{DD} and ground using a Keithley 485 Picoammeter. The measurement was of the current flow through the ten column loads. The square roots of the measured current values for a range of load gate

voltages (V_{LG}) between 1 and 3 V are shown in **Figure 6.3**. Also shown are the simulated values for a single column load transistor. The mean ratio between the measured current and the simulated value is 8.7 ± 0.7 rather than the expected precise value of 10. This discrepancy may be due to the second stage p-channel output follower or an unreliable simulation model. Further analysis of the data was performed by applying a linear least squares fit to the measured and simulated data within the linear range. The measurement errors were not accounted for in the fitting procedure as they were too small to affect the level analysis required here. The measured current is seen to depart from the expected quadratic behaviour above $V_{LG} = 2.5$ V and extrapolation of the fit to lower voltages implies a threshold value (V_T) for the column loads of ~ 0.75 V (as expected from the process parameters). Therefore when biasing the Test Structures the load gate voltage should be above 1 V to minimise any non-linearity in the output circuit due to sub-threshold operation, as seen in the simulations in Chapter 4. However an excessive V_{LG} will mean the array consumes more power.

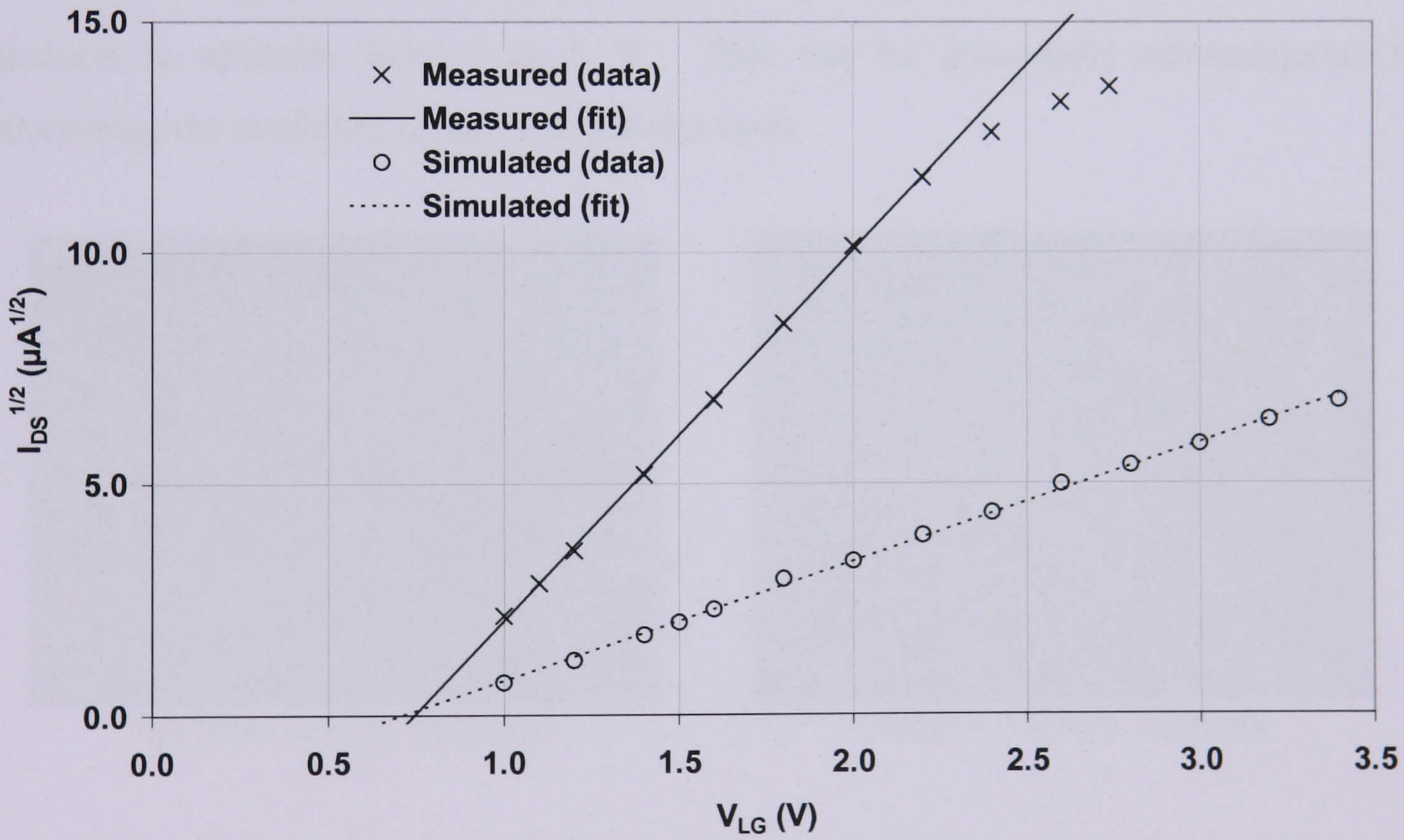


Figure 6.3 The column load transistor current vs. Load Gate Voltage, V_{LG}. An extrapolated least squared fit to the linear part of the curve implies a threshold voltage (V_T) for the column load transistors of 0.75 V

6.2.5. Reset feed-through characteristics

The reset feed-through (Crawford, 1967) seen earlier in **Figure 6.1** is an unfortunate consequence of the capacitive coupling between the reset transistor clock pulse and the

voltage sampled on the sense node capacitance. It is possible to investigate the nature of the reset feed-through using the Test Pixels because the output can be observed continuously during pixel operation. The magnitude of the feed-through at the sense node, V_{RFT} is approximated by Equation 6.1, where C_{GS} is the gate-source capacitance of the reset transistor and $V_{\O R}$ is the magnitude of the reset transistor clock pulse (usually 5 V).

$$V_{RFT} = \frac{C_{GS}}{C_{node} + C_{GS}} V_{\phi R} \qquad (6.1)$$

The effect of reset feed-through on available signal was investigated for the n- and p-channel reset pixels in Test Pixels 1. The contrasting effect is shown in **Figure 6.4**. The feed-through in the n-channel pixel is negative which reduces available signal swing at the node by 90 ± 2 mV. The feed-through is negative because the transition of the reset transistor clock pulse is downwards from 5 to 0 V to turn off the transistor. On the other hand for the p-channel reset the feed-through is positive 60 ± 2 mV because the transition is upwards from 0 to 5 V. This can be potentially advantageous for maximising the available signal swing at the node.

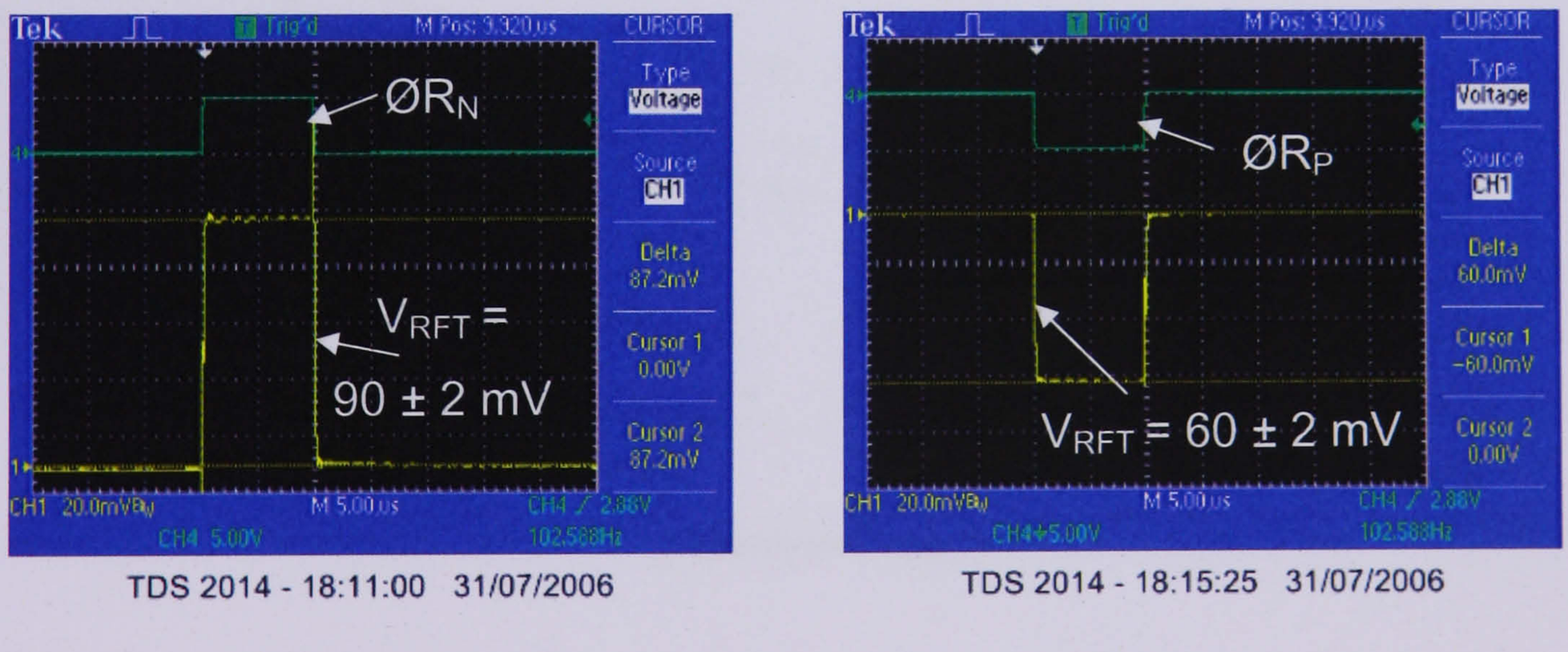


Figure 6.4 n-channel (left) and p-channel (right) reset feed-through

Equation 6.1 implies the reset feed-through variation will vary with the diode size as this strongly influences diode capacitance. The effect of different sized n+/p-well diode pixels in Test Pixels 1 and 2 was therefore investigated and is shown in **Figure 6.5**. Also plotted is the referred feed-through at the sense node calculated using the source follower gain measured previously and the simulated feed-through at the node. The

shape of the curves is very similar showing that for smaller diodes reset feed-through increases and significantly reduces available voltage swing. This agrees with expectations and occurs because the node capacitance decreases, which increases the reset feed-through, as predicted by Equation 6.1. The measured feed-through with the smallest diode is greater than 300 mV, which is a significant reduction in signal swing at the node.

Although the shapes of all the curves in **Figure 6.5** are as expected from Equation 6.1, there is a large offset between the referred (measured) and simulated values. The errors on the referred (measured) values are relatively small and not large enough to account for the discrepancy. It is therefore more likely that the difference is due to a problem with the accuracy of the simulation of parasitic capacitances within the pixel.

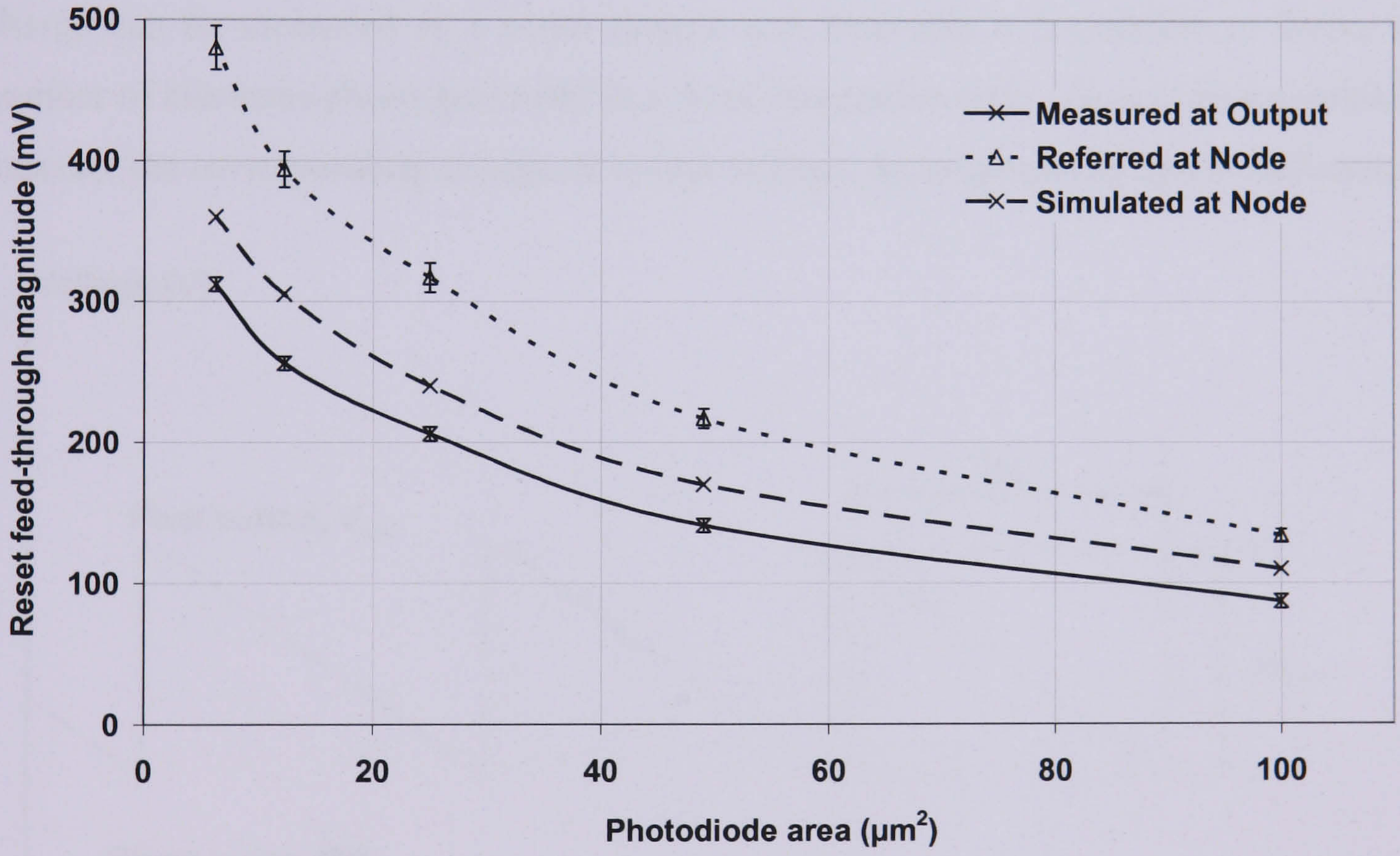


Figure 6.5 Reset feed-through variation with n+/p-well diode area ($ØR_N$ = 5 V, V_{RD} = 3 V).

It should be noted that if the reset feed-through is an important effect to minimise, then these results indicate that the best solution would be a p-channel reset pixel incorporating a larger diode.

6.3. Test Pixels responsivity measurements

The variation of responsivity of the different designs within the Test Pixels was investigated using a new method, which involves measuring the current flow between V_{RD} and ground as the pixel is operated. The method has not been reported in the literature but has been used previously to characterise CCD responsivity. The more common technique is the mean-variance method used to characterise the Imaging Arrays outlined later in this chapter.

6.3.1. Theoretical background

The basic principle of the reset drain current responsivity measurement is that when the pixel is reset all the charge that has been collected flows out of the diode through the reset transistor to the reset drain connection (V_{RD}). Under repetitive operation the charge can be measured as a mean current and from this it is possible to derive the number of electrons photo-generated in a fixed integration time. As it is also possible to measure the corresponding change of output voltage, the responsivity can be calculated.

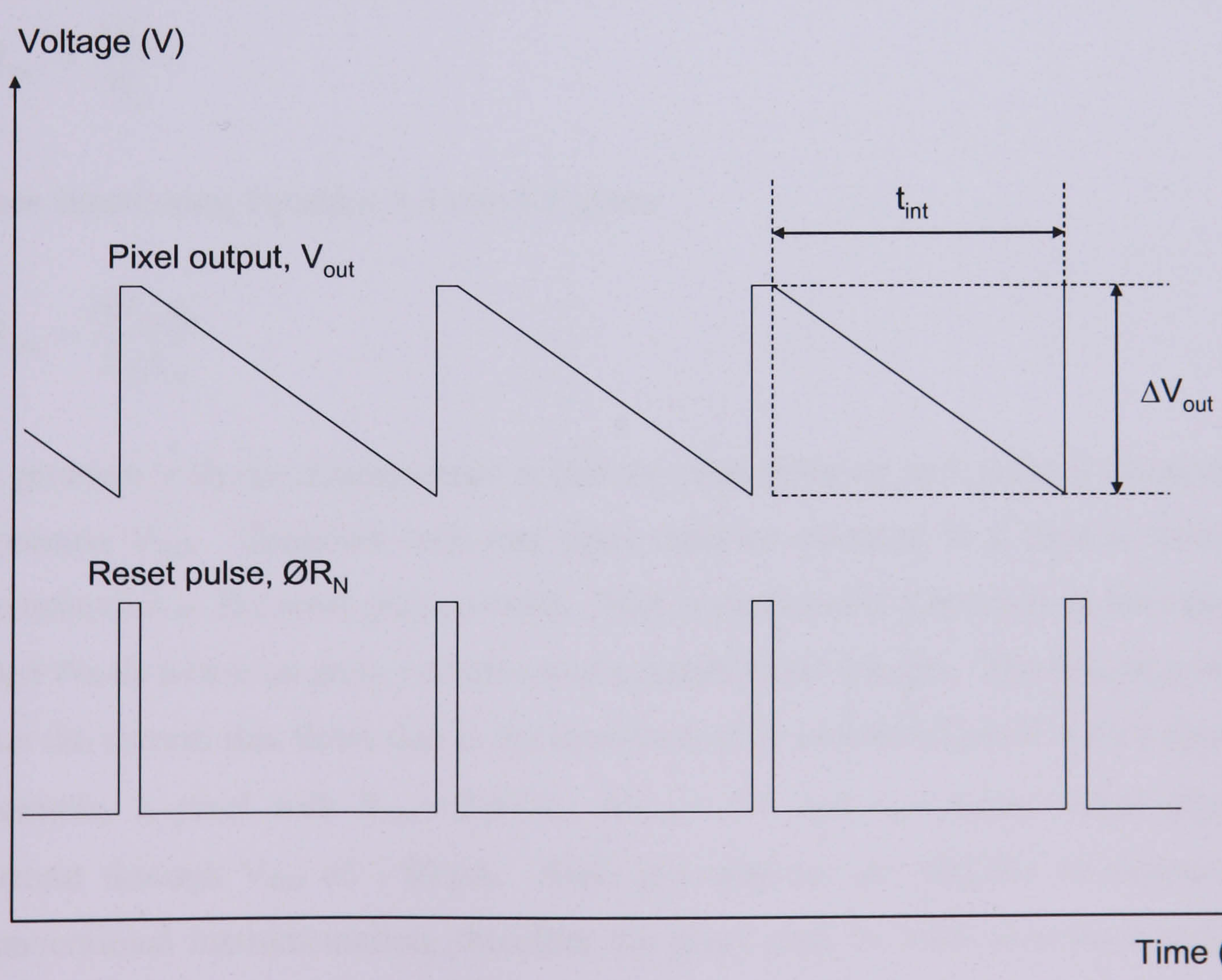


Figure 6.6 Mode of operation for the V_{RD} current responsivity measurements of the Test Pixels

The principle of the measurement is illustrated in **Figure 6.6** and is essentially identical to the normal mode of operation for the pixel. If the mean current flowing through V_{RD} is I_{RD}, the number of electrons flowing per second n_e (e^-/s) is:

$$n_e = \frac{I_{RD}}{q_e} \tag{6.2}$$

Where q_e is the electron charge. If the period over which the signal electrons are integrated is t_{int}, then the total number of electrons N_e collected will be:

$$N_e = n_e \, t_{int} \tag{6.3}$$

Substituting Equation 6.2 into 6.3 gives:

$$N_e = \frac{I_{RD}}{q_e} t_{int} \tag{6.4}$$

Therefore if the output responsivity is given by:

$$R_{out} = \frac{\Delta V_{out}}{N_e} \tag{6.5}$$

then substituting Equation 6.4 into 6.5 gives:

$$R_{out} = \frac{\Delta V_{out} q_e}{I_{RD} t_{int}} \tag{6.6}$$

A problem with the measurement is that the reset drain of each pixel is connected to a common V_{RD}. Therefore only one pixel must be operated at a time to measure its contribution to the reset drain current. This is particularly important in the case of the Test Pixels where an array contains four separate pixel designs. The second problem is that the current that flows due to the operation of an individual pixel is very small. For example, a pixel with $R_{out} = 2\ \mu V/e^-$, $\Delta V_{out} = 1$ V and $t_{int} = 1$ ms, would generate a current through V_{RD} of ~ 80 pA. Such low currents are difficult to measure using conventional instrumentation, therefore the pixel must be reset at a much higher rate ($t_{int} \sim 10\ \mu s$) and a bright source must be used to discharge the pixel appreciably (~ 1 V) during the short integration time. This should increase the current to > 10 nA. The

solution to the above problems was to illuminate the pixel of interest using a laser spot focussed to sub-pixel dimensions.

6.3.2. Experimental set-up

The experimental set-up for the measurement consisted of the Test Pixels device and basic headboard, a ×10 microscope objective and an infrared laser diode ($\lambda = 790$ nm) mounted onto an optical bench. The APS and headboard were mounted on an X-Y-Z translation stage for focussing of the laser spot, and for lateral movement of the spot between pixels. Sequencing of the APS was controlled by the ADCDSP system outlined in Chapter 5. To obtain an appreciable current at the reset drain the pixel was reset with a t_{int} of 5 μs. V_{SS}, V_{LG}, V_{RD}, V_{DD}, were fixed at 0, 1, 3 and 5 V respectively. The output waveform from a column was sampled directly by an oscilloscope, therefore the chosen row of pixels was permanently selected by maintaining the ØRS connection at 5 V. Three pixel column outputs were observed simultaneously using the four channel oscilloscope. The laser spot was focussed and positioned within an individual pixel by observing when the pixel discharge was maximum in the central pixel of a set of rows or columns, and minimal within the two adjacent rows. It was found that it was not possible to eliminate signal from any of the surrounding eight pixels, therefore the ΔV_{out} from all nine pixels was recorded and summed to give the total voltage change due to the measured current. The current generated at V_{RD} was of the order of 10 nA, therefore accurate measurement required the use of a Keithley 617 Electrometer. Measurements were made for all twelve pixel designs contained within Test Pixels 1, 2 and 3 and the results are outlined in the next section.

6.3.3. Results and discussion

The structures in Test Pixels 1 enabled comparison of the responsivity of the two types of diode available using the TS50 fabrication process. Results are summarised in **Table 6.1**. Also shown is the simulated output responsivity for the 100 μm^2, n+/p-well photodiode, using the capacitance model supplied by Tower Semiconductor. Unfortunately no information was available from the foundry regarding the n-well/p-sub photodiode capacitance for comparison with the measured values.

Photodiode type	Photodiode area (μm^2)	Reset transistor	Measured R_{out} ($\mu V/e^-$)	Simulated R_{out} ($\mu V/e^-$)
n+/p-well	100	n	2.3 ± 0.3	2.3
n+/p-well	100	p	2.1 ± 0.3	2.3
n-well/p-sub	100	n	3.8 ± 0.3	-
n-well/p-sub	80	p	3.8 ± 0.3	-

Table 6.1 Responsivity measurements summary for Test Pixels 1. Simulated R_{out} is for V_{node} = 2 V

The two values measured for the n+/p-well diode agree well with the simulated values and the there is no significant change between the n- and p-channel reset versions, as expected due to the expected negligible difference in node capacitance. The n-well/p-sub diode shows a much higher responsivity but unfortunately no comparison can be made with a simulated value. The p-channel reset version should have shown an increase in the responsivity, due to reduced capacitance associated with the smaller diode, but this was not observed. The structures in Test Pixels 2 and 3 further enabled understanding of the effect of diode size on the responsivity of the n+/p-well diodes. The values measured for the range of n+/p-well diode sizes along with simulated values, using the n+/p-well capacitance model, are plotted in **Figure 6.7**.

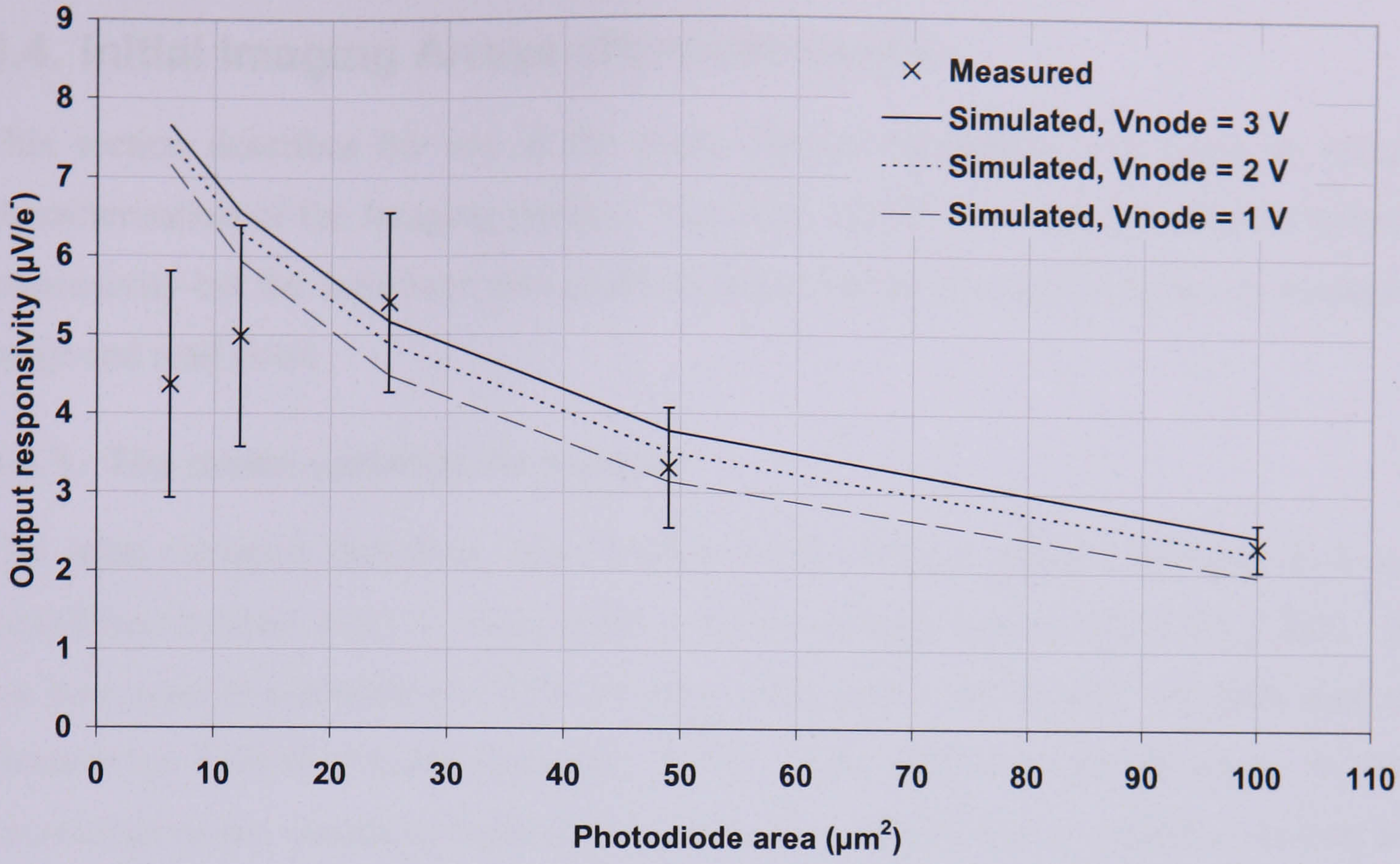


Figure 6.7 Measured responsivity for the range of diode sizes compared with the simulated values for a range of node voltages

The measured values agree quite well with the simulated values for the range of diode sizes except for the two smallest diodes. The discrepancy for the two smallest diodes may be due to some of the signal diffusing outside of the 3 × 3 pixel square due to the smaller collecting area in each pixel. Another source of error for the measurements is the non-linearity of the responsivity. The voltage change ΔV_{out} was measured over a wide range of ~ 1.5 V. The simulations show the responsivity over this range changes by 0.5 μV/e⁻. Therefore the value measured is only a mean value for the middle of the output range of the pixel. It should increase for higher sense node voltages and decrease for lower voltages.

6.4. Initial Imaging Arrays characterisation

This section describes the use of the mean-variance technique to perform an initial characterisation of the Imaging Arrays. The main objective was to quantify the output responsivity but the technique also enabled measurement of node capacitance, dynamic range and read noise.

6.4.1. The mean-variance technique

The mean-variance technique (also known as the photon transfer technique) is an established method used to characterise solid-state image sensors (Janesick, 1985). It has been used to characterise CCDs for many years and more recently has been used to characterise CMOS sensors (Janesick, 2002). The method takes advantage of the knowledge of the statistical behaviour of the arrival of photons at a surface, known as shot noise. Shot noise is the noise associated with the random arrival of photons at the pixel. The noise obeys a Poisson statistical distribution whereby the mean number of photons incident on a pixel during a given time period is equal to the variance. If the mean number of photons is $\mu_{photons}$ then the associated variance, $\sigma^2_{photons}$ and the standard deviation, $\sigma_{photons}$ are:

$$\sigma^2_{photons} = \mu_{photons} \tag{6.7}$$

$$\sigma_{photons} = \sqrt{\mu_{photons}} \tag{6.8}$$

If the quantum efficiency of the device is η, then the mean number of electrons generated and the associated variance and the standard deviation are given by:

$$\mu_{electrons} = \eta\mu_{photons} \tag{6.9}$$

$$\sigma^2_{electrons} = \eta\mu_{photons} \tag{6.10}$$

$$\sigma_{photons} = \sqrt{\eta\mu_{photons}} = \sqrt{\mu_{electrons}} \tag{6.11}$$

Therefore the uncertainty in the quantity of charge collected in a pixel is given by the square root of the mean number of incident photons. If the responsivity of the device is

R_{out}, then the mean output voltage and associated variance and standard deviation are given by:

$$\mu_{volts} = R_{out}\mu_{electrons} \tag{6.12}$$

$$\sigma^2_{volts} = R^2_{out}\mu_{electrons} \tag{6.13}$$

$$\sigma_{volts} = R_{out}\sqrt{\mu_{electrons}} \tag{6.14}$$

After analogue to digital conversion and any other associated signal processing the mean signal, in terms of ADC counts, and the associated variance and standard deviation are given by:

$$\mu_{counts} = G_E R_{out}\mu_{electrons} \tag{6.15}$$

$$\sigma^2_{counts} = G^2_E R^2_{out}\mu_{electrons} \tag{6.16}$$

$$\sigma_{counts} = G_E R_{out}\sqrt{\mu_{electrons}} \tag{6.17}$$

where G_E is the electronic gain in terms of ADC counts/μV. Dividing the variance by the mean gives the system gain, G_S in terms of ADC counts/e^-:

$$G_S = \frac{\sigma^2_{counts}}{\mu_{counts}} = \frac{R^2_{out}G^2_E\mu_{electrons}}{R_{out}G_E\mu_{electrons}} \tag{6.18}$$

Therefore by measuring the mean signal and corresponding variance for a range of signal levels of the sensor, one can calculate the gradient of the resulting curve and measure G_S. Knowledge of G_S then enables any measurement made in ADC counts to be converted into more fundamental units of electrons. Rearranging Equation 6.18 also gives R_{out} in terms of G_S and G_E only:

$$R_{out} = \frac{G_S}{G_E} \tag{6.19}$$

Therefore if the electronic gain is measured by performing a calibration of the electronics and G_S is measured using mean-variance data, then R_{out} can be calculated.

6.4.2. Experimental set-up

There are a number of different approaches to generating the data for the mean-variance measurement. The first task is to generate images with a signal level over the full output range of the device. This can be done either by fixing the integration time and varying the illumination, or by fixing the illumination and varying the integration time. The second task is to generate the mean and variance data for each signal level. There are two main approaches to do this. The first is to illuminate the device with a highly uniform beam at a given illumination level and calculate the mean signal level of the array and the spatial variation from pixel to pixel. This approach is more suited to CCD characterisation as all pixels use the same readout circuit. It can be used for APS characterisation but care must be taken to and isolate the spatial variance due to the shot noise by removing the fixed pattern noise introduced by the individual readout circuits.

A more suitable approach for an APS with a readout circuit within each pixel is to illuminate the sensor and take many (100-1000) successive images. By calculating the temporal variation in the output for each pixel from image to image, the mean and variance data can be generated for individual pixels. Therefore the variation in performance from pixel to pixel can be investigated. This approach requires that the illumination within each pixel is constant over the period of multiple image acquisition, but the beam does not need to be uniform across the array. In fact this can be advantageous as multiple mean-variance data points can be generated in one set of images. The disadvantage is that many images must be taken at many signal levels, which requires a large amount of data processing.

The mean-variance data was generated using the room temperature Imaging Arrays drive electronics system described previously in Chapter 5. The APS and headboard were mounted on an optical bench within a dark box. A Bentham quartz tungsten halogen (QTH) light source was coupled to an in-line integrating sphere with fibre optics to illuminate the APS. The light source power supply was current stabilised to ensure a constant light level during successive exposures. The output from the integrating sphere was passed through a collimating lens onto the APS. The signal level was varied over the full output range of the device by changing the intensity of the light source with neutral density filters, and also by varying the integration time. The low

gain setting of ×2 was set on the headboard to enable the full output range of the device to be sampled by the ADC. Use of the higher gain setting would have meant the ADC would have saturated before the pixel output. With this setting the electronic gain (G_E) was measured using a calibrated voltage reference to be 0.03104 ± 0.00010 ADC counts/μV.

For all images acquired, V_{DD} and V_{LG} were set at 5 V and 3 V, respectively, and V_{RD} was set at 3 V to ensure hard reset. The mean-variance data for each signal level was then generated by acquiring 1000 successive images. The temporal mean signal and associated variance for each pixel was then calculated. 1000 images were also read out of the device for a zero integration time to obtain the mean DC offset for each pixel. This value was then subtracted from each pixel output for each signal level to obtain the true absolute mean signal level. The mean variance data generated over the full output range of both Imaging Arrays are shown in **Figure 6.8** and **Figure 6.9** respectively. The data are plotted in the classic photon transfer curve (PTC) style (Janesick, 2001) with the noise (standard deviation) plotted as a function of the mean signal level on a logarithmic scale. At low signal levels the noise is dominated by the read noise of the device, then as the signal level increases the shot noise increases and begins to dominate until the pixel approaches saturation and the noise reduces rapidly. Also shown is the noise data with the read noise floor removed. The mean read noise for each device was subtracted in quadrature to give the shot noise component only. A simple visual inspection of the shot noise data shows a gradient of ~ 0.5 on the logarithmic plot. This agrees with the Poissonian statistics of shot noise whereby the noise is the square root of the mean signal. At very low signal levels the noise is dominated by the noise from the electronics. The analysis and results from this data are outlined in the following sub sections.

It is generally acknowledged in the imaging business that the shape of a mean-variance curve is a good indicator as to the "quality" of an imaging system. The fact that the curves in **Figure 6.8** and **Figure 6.9** are exactly as expected from theory (i.e. no artefacts are present) gives confidence that both the device and the drive electronics are functioning correctly.

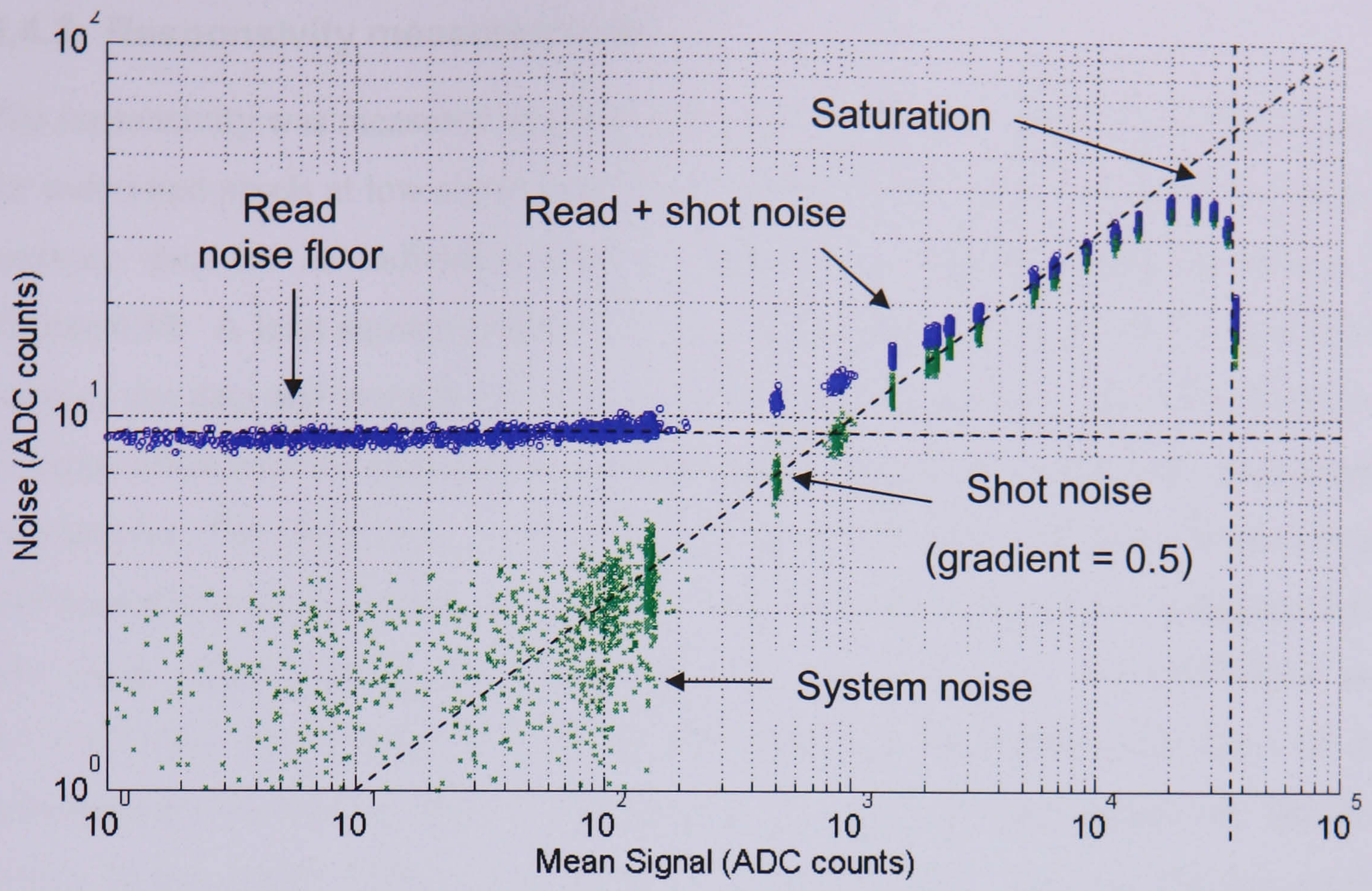


Figure 6.8 Mean-variance data over the full well capacity of CMOS001 plotted as a photon transfer curve (PTC) for the central 10 × 10 pixels

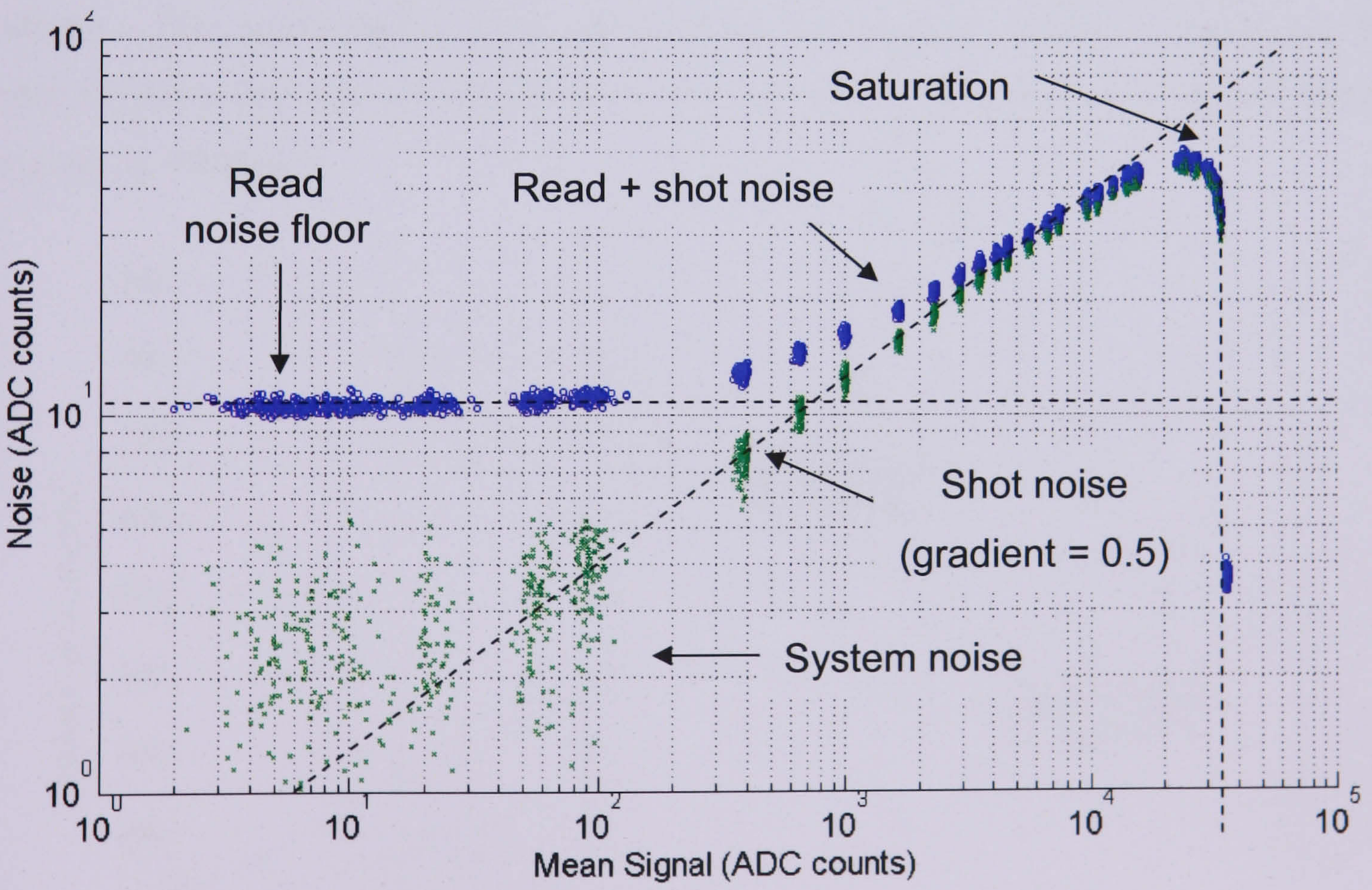


Figure 6.9 Mean-variance data over the full well capacity of CMOS002 plotted as a photon transfer curve (PTC) for the central 10 × 10 pixels

6.4.3. Responsivity measurements

The responsivity was measured by plotting the mean signal as a function of the variance for individual pixels at low signal levels to avoid the non-linearity problem. The mean-variance data for an individual pixel in each of the Imaging Arrays is shown in **Figure 6.10**. A least squares method (not accounting for errors) was used to fit a linear curve to the data and measure the gradient i.e. the system gain, G_S. This was then used in conjunction with the electronic gain measured previously to calculate the pixel output responsivity. The calculation was repeated for the central 100 × 100 pixels in each array and histograms of the distributions of the calculated values are shown in **Figure 6.11**. The mean output responsivity was found to be 3.0 ± 0.1 μV/e$^-$ for CMOS001 and 4.7 ± 0.3 μV/e$^-$ for CMOS002. The quoted errors are the standard deviation of the distribution of values for the 100 × 100 pixels. The process was repeated for the data with a fit to a higher signal range, as shown in **Figure 6.12**. The analysis showed the responsivity to reduce to 2.3 ± 0.1 μV/e$^-$ for CMOS001 and 3.8 ± 0.3 μV/e$^-$ for CMOS002. In both cases the output responsivity reduced by ~ 20 %. This was as expected as the capacitance increases as signal is collected and the sense node voltage reduces. The non-linearity of the responsivity was not investigated in detail, as the mean-variance data was not considered to be accurate enough. A summary of the results is given in **Table 6.2**.

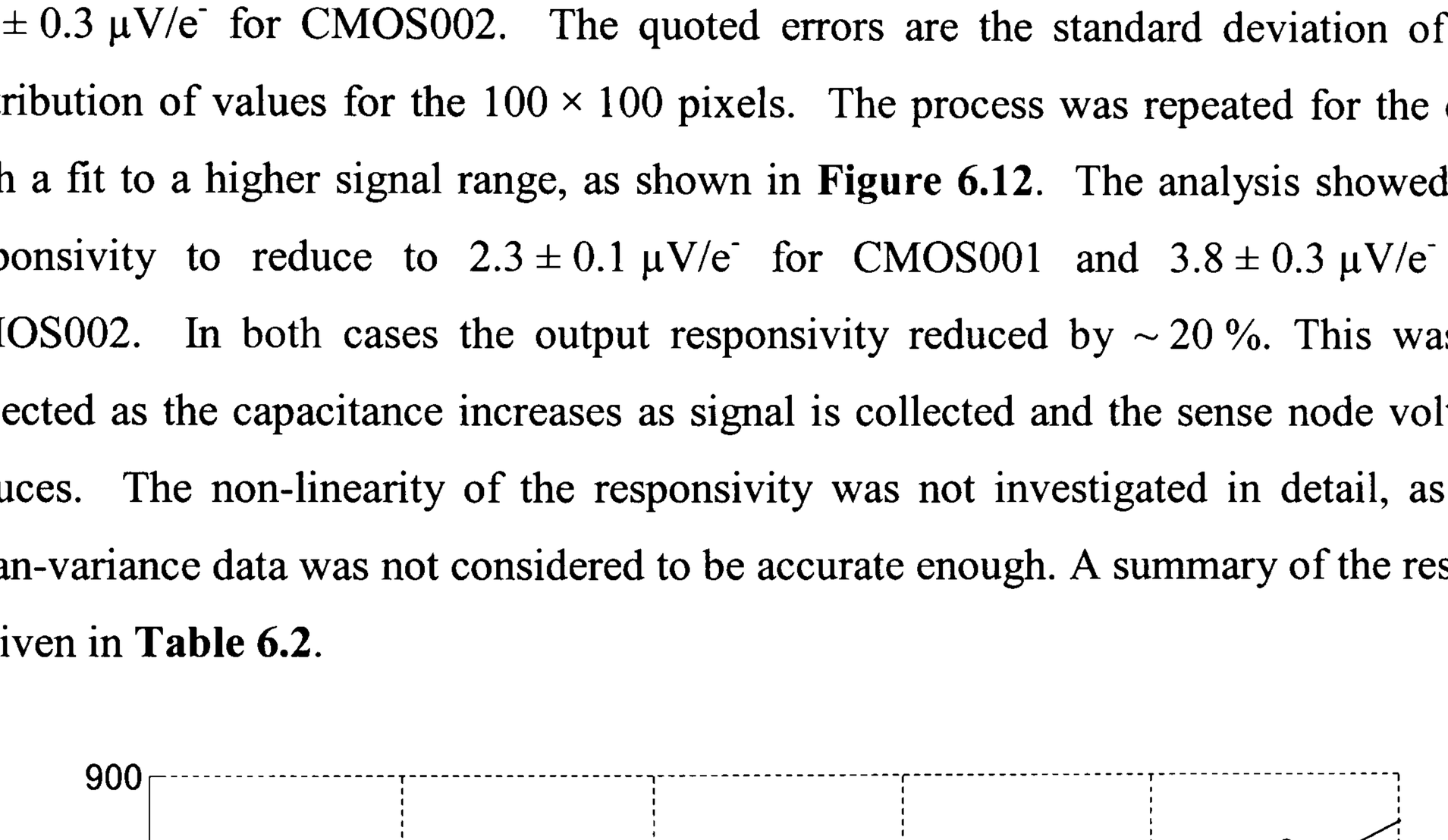


Figure 6.10 Mean-variance data for a single pixel over a low signal range for both Imaging Arrays

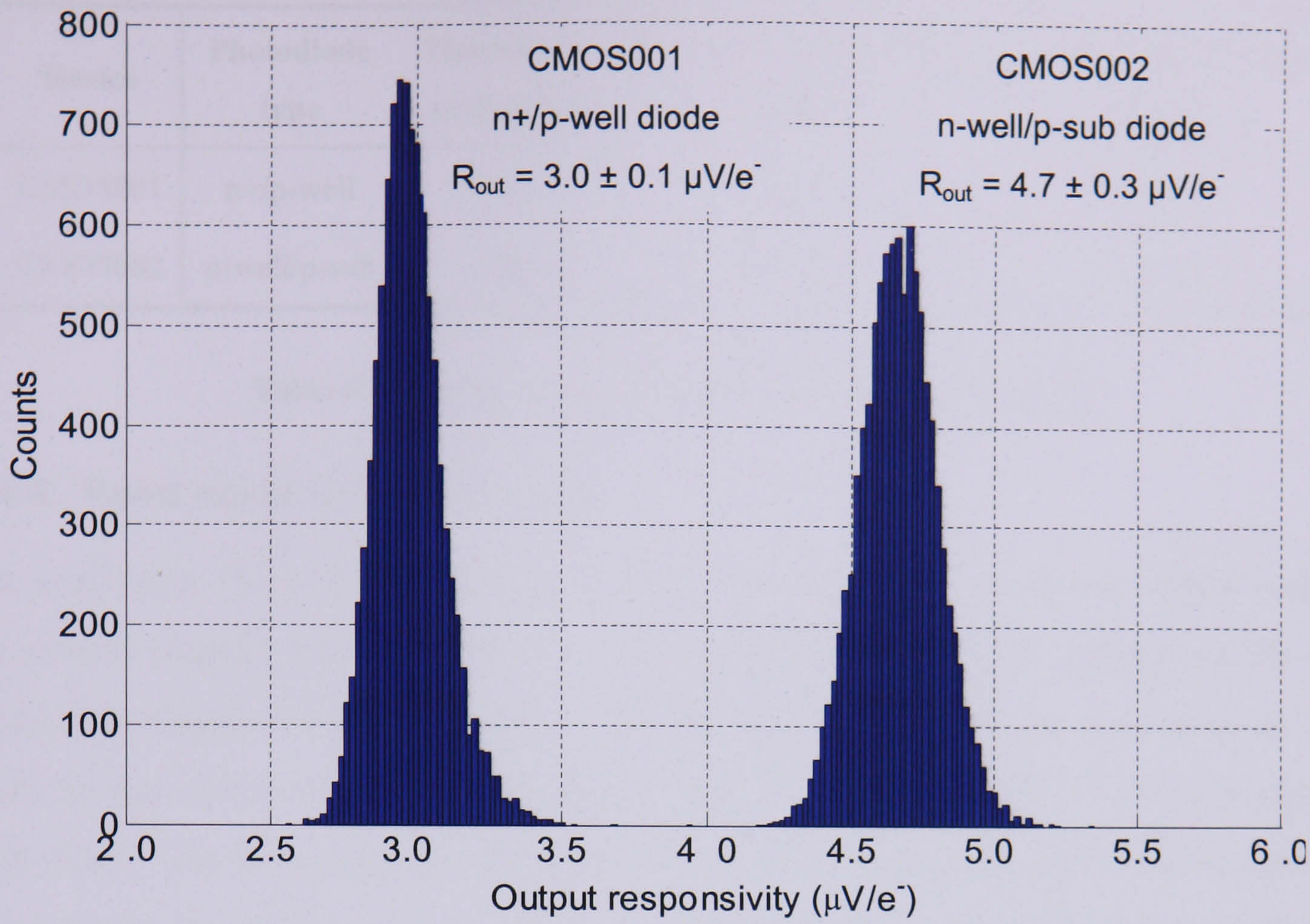


Figure 6.11 Histogram of responsivity values calculated for the central 100 × 100 pixels in each of the Imaging Arrays

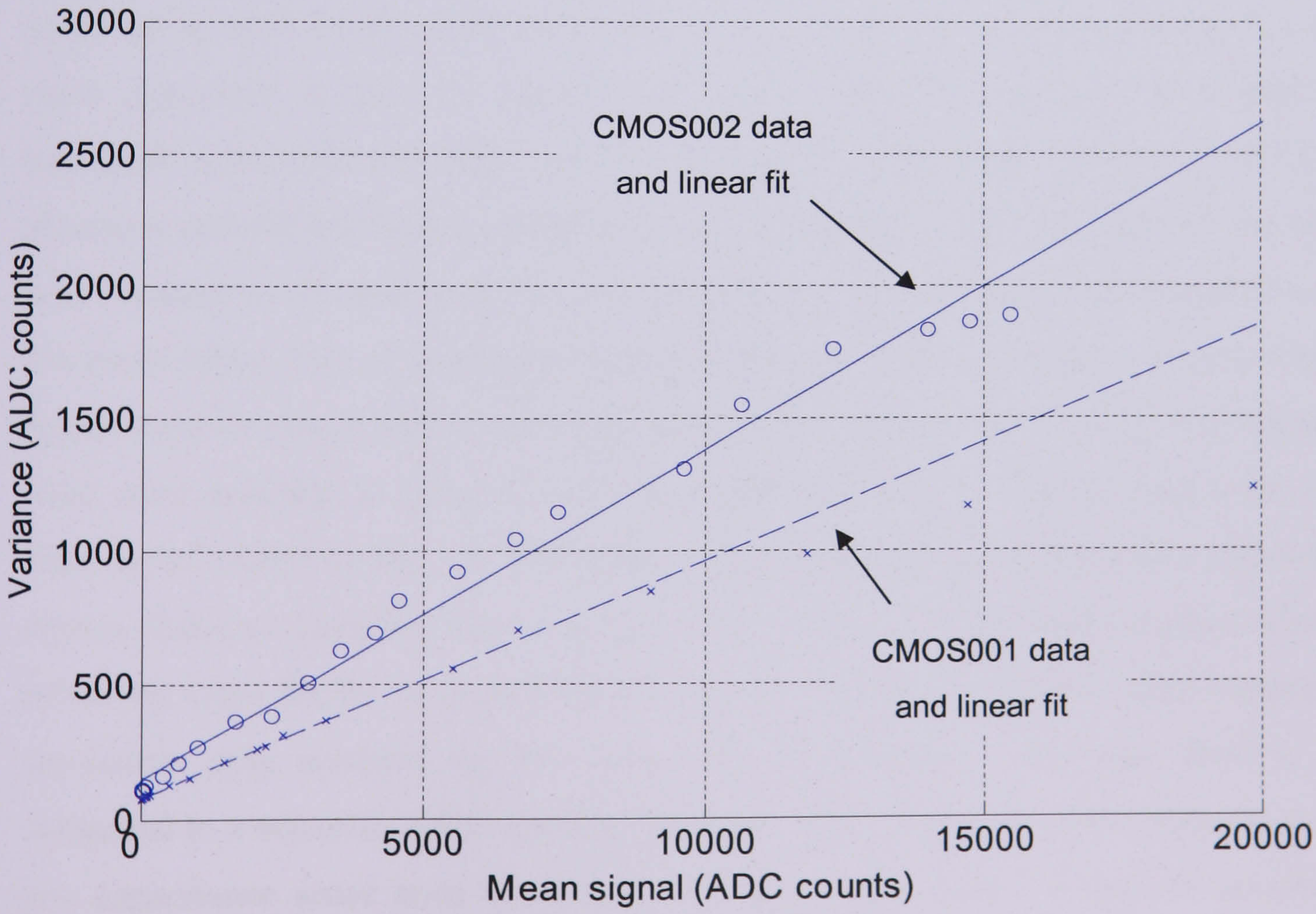


Figure 6.12 Mean-variance data for a single pixel plotted over a larger signal range for both Imaging Arrays

Device	Photodiode type	Photodiode area (μm^2)	R_{out} (low signal range) ($\mu V/e^-$)	R_{out} (high signal range) ($\mu V/e^-$)
CMOS001	n+/p-well	100	3.0 ± 0.1	2.3 ± 0.1
CMOS002	n-well/p-sub	100	4.7 ± 0.3	3.8 ± 0.2

Table 6.2 Imaging Arrays responsivity measurement summary

6.4.4. Read noise measurements

The read noise floor of the Imaging Arrays can clearly be seen at low signal levels in the photon transfer curves. The noise was separately measured by analysing the 1000 dark offset images from each device. The standard deviation of the reset level for each pixel for the 1000 images was calculated to give the reset fluctuation in ADC counts for each pixel. The average noise was then measured by calculating the mean of the reset noise across the central 100 × 100 pixels. The read noise measured also includes any component introduced by the electronics. Removing the APS and connecting a resistor between the input to the electronics signal chain and ground and acquiring 1000 dummy images measured the electronics noise. Using this method the total system noise was measured to be 3.0 ± 0.1 ADC counts (r.m.s). This value was subtracted from the total noise measured to give the sensor read noise. The low signal level responsivity measured previously was then used to calculate the read noise in terms of volts and electrons and the results are summarised in **Table 6.3**. The noise floor of the sensor was expected to be reset noise limited because no CDS processing was performed on the pixel output. This is confirmed by the fact that the lower capacitance (implied by the higher responsivity) n-well/p-sub diode exhibits lower noise than the n+/p-well diode. If CDS were available to remove the reset component, then one would expect the noise floor to be limited by the 1/f, RTS and thermal components introduced by the in-pixel source follower transistor (the total probably < 10 e^-). This would explain why the measured value for the n+/p-well diode is greater than the simulated value, because the simulation only accounts for the reset noise component. The noise level is high compared to a scientific CCD and highlights the need for a CDS enabled pixel and/or a low capacitance sense node to suppress the large reset noise. It may be possible to reduce the noise using soft reset but this was not investigated.

Device	Photodiode structure	Photo-diode area (μm^2)	Mean total noise (ADC counts)	Mean read noise (ADC counts)	Mean Sensor read noise (μV)	Mean Sensor read noise (e^-)	Simulated reset noise (e^-)
CMOS001	n+/p-well	100	8.6 ± 0.3	8.10 ± 0.3	261 ± 9	87 ± 9	82
CMOS002	n-well/p-sub	100	10.5 ± 0.7	10.05 ± 0.3	324 ± 24	69 ± 5	-

Table 6.3 Imaging Arrays read noise summary. The simulated noise is for $V_{node} = 3$ V at T = 300 K. The errors on the noise values are derived from the standard deviation of the mean total noise in Column 4

6.4.5. Full well capacity and dynamic range

The maximum output signal from the Imaging Arrays is effectively the point in the mean-variance data at which the noise starts to decrease. For both devices this is seen to occur at 35,000 ADC counts. Using the system gain measured previously for each design enables calculation of the maximum number of electrons each pixel design can collect, known as the full well capacity (FWC), N_{FWC}. The calculated values are given in **Table 6.4**. Also shown is the dynamic range in terms of decibels calculated using the noise values measured in the previous section:

$$DR = 20\log\left(\frac{N_{FWC}}{N_n}\right) \tag{6.20}$$

The two devices have similar output voltage ranges but the n+/p-well pixel has a much higher full well capacity because the responsivity is 50 % lower. The dynamic range of the n-well/p-sub design is also lower than the n+/p-well pixel, although the reduction is partly recovered because of the lower read noise. It should be noted that the values for the FWC and dynamic range are likely to have been underestimated slightly due to the non-linear behaviour of the responsivity.

Device	Photodiode structure	Photodiode area (μm^2)	Full well capacity (ke^-)	Dynamic range (dB)
CMOS001	n+/p-well	100	400 ± 13	73.3 ± 0.9
CMOS002	n-well/p-sub	100	250 ± 16	71.2 ± 0.8

Table 6.4 Imaging Arrays full well capacity and dynamic range ($V_{DD} = 5$ V, $V_{RD} = 3$ V, $V_{LG} = 3$ V)

6.4.6. Node capacitance measurements

Measurement of the responsivity and the read noise provides two methods of calculating the sense node capacitance. If both the responsivity and voltage gain are known then the node capacitance can be calculated using:

$$C_{node} = \frac{q_e G_{SF}}{R_{out}} \tag{6.21}$$

Also if the read noise is known in terms of electrons and assumed to be dominated by the reset noise component under hard reset conditions, then the node capacitance is given by:

$$C_{node} = \frac{(q_e N_n)^2}{kT} \tag{6.22}$$

The responsivity and noise values measured for the Imaging Arrays were therefore used to calculate the sense node capacitance of the two pixel designs. The noise capacitance calculation assumed a temperature of 300 K and that the majority of the read noise is due to reset noise. The results are summarised in **Table 6.5**. The responsivity-inferred capacitance of the n-well/p-sub pixel is lower than the n+/p-well design, which follows from the higher measured responsivity. The same is seen with the noise-inferred capacitance calculation as a lower capacitance implies a lower reset noise component. The noise-inferred capacitance appears to overestimate the node capacitance predicted by the model because, as mentioned before, not all the read noise will be due to the reset component. Other noise contributions such as source follower noise would need to be characterised to make a more accurate noise-inferred node capacitance measurement. It is also likely that this is the reason why the noise-inferred capacitance is higher than the responsivity-inferred value.

Device	**Photodiode type**	**Photodiode area (μm^2)**	**Responsivity inferred C_{node} (fF)**	**Reset noise inferred C_{node} (fF)**	**Simulated C_{node} (fF)**
CMOS001	n+/p-well	100	36 ± 1	47 ± 10	42
CMOS002	n-well/p-sub	100	23 ± 1	29 ± 4	-

Table 6.5 Imaging Arrays node capacitance measurements. The simulated C_{node} is for $V_{node} = 3$ V

6.5. Summary and discussion

The main aim of the work described in this chapter was to characterise the responsivity of the different pixel designs contained within the Test Structures. This was primarily required to enable further measurement of parameters such as dark signal and quantum efficiency. The key features of the devices gained from the initial Test Pixels characterisation are as follows:

- The output signal saturation is ~ 2 V for all pixel designs due to the source follower circuit transistor ceasing to function at lower node voltages
- The upper limit on the operating range of the sensor is determined by the polarity of the reset transistor used in the pixel design
- Use of the p-channel reset transistor increases available signal swing by ~ 1 V
- Reset feed-through has a significant effect on available signal swing and is strongly dependent on the pixel design
- The V/V gain (G_{SF}) of the readout circuit common to all designs is 0.68 ± 0.05 and allows the output responsivity to be related to the node responsivity enabling a node capacitance calculation
- All devices exhibit a significant output response non-linearity due to the photodiode capacitance variation with signal

Subsequently the key features extracted from the initial Imaging Arrays mean-variance characterisation are:

- The responsivity of the n-well/p-sub photodiode structure is 50% higher than the n+/p-well type and the pixel to pixel variation is low
- The derived node capacitance is therefore lower for the n-well/p-sub diode
- The read noise of the Imaging Arrays is limited by the reset (kTC) contribution
- The noise is therefore lower in the n-well/p-sub diode because of the lower sense node capacitance
- The full well capacity and dynamic range of the n+/p-well pixel is much higher than the n-well/p-sub pixel (despite the higher read noise) because of the lower responsivity

Perhaps the most important results from this chapter are the values obtained for the responsivity. Two independent methods have been used to obtain these values. The disadvantage of the V_{RD} current technique was that it returned an average value for the responsivity across the signal range. The technique also failed to yield good results for the smaller diode sizes. An alternative method (which was not explored) is the use of a Fe55 X-ray source to generate a known amount of charge in the pixel. Further work should use the mean variance technique for the Test Pixels to confirm the responsivity variation and also the noise performance of each design. Another area needing investigation is the response non-linearity. This will require improved mean variance data for all the Test Structures. Finally further work is required to investigate the benefits of the p-channel reset pixel and the extent of the noise contribution under soft reset. The results outlined here have laid the foundations for the detailed dark signal characterisation outlined in Chapter 7 and the electro-optical performance described in Chapter 8.

Chapter 7: Dark signal characterisation

This chapter describes an investigation into the dark signal performance of the Test Structures. The chapter begins by outlining the different sources of dark signal in an active pixel. The first experimental section describes an investigation of the Imaging Arrays dark signal behaviour at room temperature and then over a wider temperature range. The chapter then reports the discovery of an additional source of dark signal observed in the Test Pixels due to "hot-carrier" effects and includes a subsequent investigation into the characteristics of the extra contribution. The chapter closes with a discussion of the relative importance of the two effects to the overall dark current.

7.1. Introduction

The dark signal is a major performance limitation in all solid-state imaging devices. In the absence of light input all semiconductor devices suffer from parasitic currents arising from electrons that have sufficient thermal energy to break free from the lattice and enter the conduction band. In an APS the electrons can be collected by the sense node and discharge the pixel. The suppression of dark signal is essential to:

- Minimise fixed pattern noise sources due to dark signal shot noise and non-uniformity
- Maximise dynamic range for long exposures

The overall dark signal is highly dependent on the design of the sensor, the manufacturing process used and the operating conditions. Therefore the various sources of dark signal in a CMOS active pixel sensor must be carefully considered when designing and operating a high performance scientific imaging device. Competing CCD fabrication processes have been optimised to reduce the dark signal under normal operation from > 1 nA/cm^2, to < 10 pA/cm^2 using special pinning implants (Burkey et al., 1984) and inverted mode operation (e2v technologies, 2006). On the other hand CMOS manufacturing processes tend to exhibit high levels of dark signal as the processes are primarily optimised for high-speed digital applications. Extra design considerations must be taken and customised processing steps similar to the CCD must be used to reduce the dark signal to acceptable levels.

7.2. Theoretical background

The dark signal in a CMOS active pixel is primarily the result of classic "generation-recombination" centres associated with the p-n junction photodiode (Sze, 1981). The density and distribution of these centres is highly dependent on the fabrication process, a consequence of which is that the dark signal can vary greatly from pixel to pixel.

7.2.1. Dark signal generation

The dark signal is essentially comprised of the dark current generated in and diffusing from the quasi-neutral areas around the p-n junction and the dark current directly generated in the depletion region (Sze, 1981). The total dark current density (A/cm^2) can be approximated by:

$$I_d \approx \left(q_e \sqrt{\frac{D_n}{\tau_n}} \frac{n_i^2}{N_A} \right) + \left(q_e \frac{n_i}{\tau_{gen}} W \right) \qquad (7.1)$$

where D_n is the electron diffusivity, τ_n is the electron lifetime in the undepleted p-type material, N_A is the doping concentration of the p-type region, n_i is the intrinsic carrier concentration of silicon, τ_{gen} is the effective generation lifetime in the depleted material and W is the depletion width.

The first term in Equation 7.1 is the diffusion component arising from any generation within a minority carrier diffusion length $L_d = \sqrt{(D_n/\tau_n)}$ of the depletion edge. CMOS devices are generally fabricated on epitaxial silicon having a thin active layer on a thick heavily doped substrate and in this case the quantity L_d can be replaced with the active thickness t. Since t is generally much smaller than L_d, the diffusion component becomes insignificant.

The second term in Equation 7.1 is the more significant generation component. This is dependent on the depletion width W and therefore dependent on the square root of the reverse bias voltage. The generation lifetime is strongly dependent on the density of defects in the silicon and is discussed in the next sub-section.

7.2.2. Defect generated sources

The dark signal given by Equation 7.1 may be considered the "ideal" component that is classically associated with a p-n junction. There are however additional "defect-generated" sources of dark signal, which are associated with localised imperfections in the silicon crystal lattice. In a CMOS active pixel the defects tend to be introduced by the damage caused by the high dose implants used to form the p-n junctions and also by the LOCOS or STI processes used for the isolation. These defect-generated sources are therefore highly dependent on the diode properties including:

- Cross sectional structure
- Doping profile
- Dimensions and shape
- Fill factor

Studies have shown that changing the shape of the diode affects the electrical stress and a smoother shaped diode such as an octagon can reduce the dark signal by 15% compared with a square diode (Schherback et al., 2002). Other techniques to reduce dark signal include the pinned photodiode mentioned earlier in Chapter 3 (Guidash et al., 1997), the non-silicide source drain pixel (Yaung et al., 2001), and the use of deuterium annealing to passivate the interface traps introduced by the STI process (Kwon et al., 2004).

7.2.3. Temperature dependence

The temperature dependence of the dark current is primarily determined by the temperature variation of the intrinsic carrier concentration, n_i (Grove, 1967). The temperature dependence of n_i is given by:

$$n_i^2 = KT^{1.5}e^{-E_g/kT} \tag{7.2}$$

where K is a constant, T is the device operating temperature (K), E_g is the silicon band gap energy and k is Boltzmann's constant. If the diffusion component is assumed to be negligible (as will be the case with epitaxial silicon), then Equation 7.1 implies that the dark current variation with temperature is given by:

$$I_d(T) = CT^{1.5}e^{-E_g/2kT} \tag{7.3}$$

where C is a constant. Given that $E_g \sim 1.1$ eV and $kT \sim 0.025$ eV at room temperature, then normalising the dark current to that at a temperature of 20°C (T = 293K) gives the following equations:

$$I_d(293) = C(293)^{1.5} e^{-0.55/0.025} \tag{7.4}$$

$$I_d(T) = CT^{1.5} e^{-0.55\times293/0.025T} \tag{7.5}$$

From which the final dark current formula is obtained:

$$I_d(T) = I_d(293)\times 7.1\times10^5 T^{1.5} e^{-6446/T} \tag{7.6}$$

The dark signal in terms of electrons per pixel per second is given by:

$$N_d(T) = I_d(T)\times A_p / q_e \tag{7.7}$$

where A_p is the pixel area (cm^2). Equation 7.6 shows that the dark signal is strongly dependent on temperature (largely through the exponential term) and scientific devices are often operated at low temperatures to reduce the mean level dark signal level and the associated shot noise.

7.3. Imaging Arrays dark signal

The first stage in the dark signal characterisation used the two Imaging Arrays. Initially the dark signal was investigated at room temperature and then the temperature dependence of the dark signal was investigated using the e2v cold characterisation facility.

7.3.1. Room temperature measurements

The initial dark signal measurements of the Imaging Arrays used the e2v based drive system described in Chapter 5. The temperature control was minimal; therefore the device temperature was highly dependent on the ambient conditions within the laboratory. The experimental set-up was identical to that used for the previous responsivity measurements except the light source was removed and the sensor was shielded from any external light sources. The bias voltages were maintained at the following values V_{DD} = 5V, V_{RD} = 3V, V_{LG} = 3V and V_{SS} = 0V. A dark image was acquired from each device for a range of integration periods. The integration period was

initially increased in 0.5s increments up to 6s and then increased in larger increments of 1s from 6s to 15s. Above 15s the integration period was increased in 15s increments up to 500s. For each of the integration periods a corresponding image with no integration was also read out to measure the DC offset level of each pixel. The mean output for a given integration time was then calculated by subtracting the mean signal level of the offset image from the mean signal level of the dark image. The mean signal was only calculated for the central 100×100 pixel region to eliminate any edge effects. The error on each mean signal data point was derived from the error in the measured output signal in ADC counts, G_E and G_S. The pixel-to-pixel variation was also measured for each integration time period by calculating the spatial variance across each dark image. The dark signal non-uniformity (DSNU), defined as (standard deviation/mean) × 100 %, was also calculated for each exposure.

7.3.2. Room temperature results and discussion

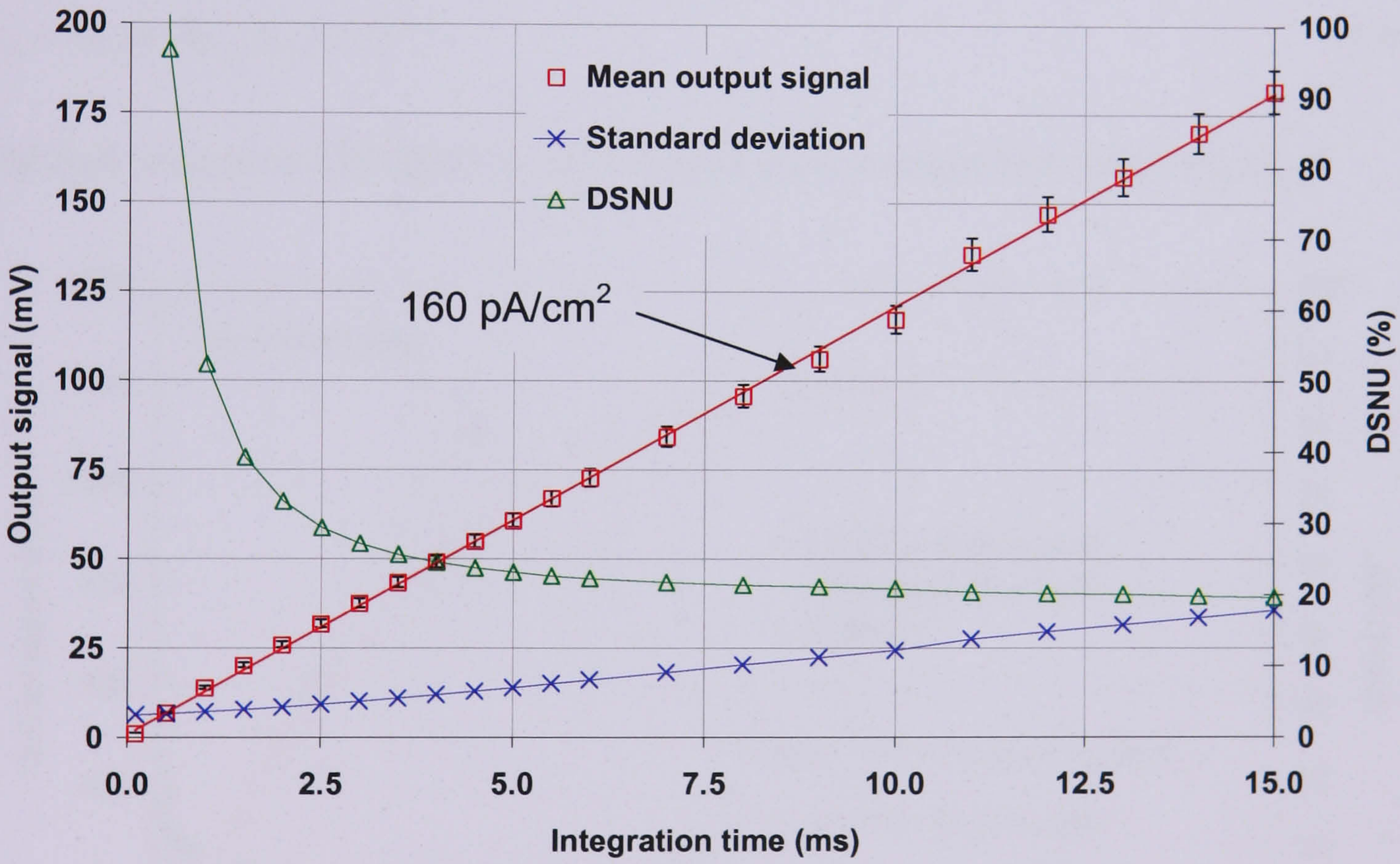


Figure 7.1 CMOS001 mean dark signal accumulation for the first 15 s of integration. The error on the mean output signal data is derived from the error in measured output signal in ADC counts, G_E and G_S

Figure 7.1 shows the mean output voltage as a function of integration period for CMOS001 under dark conditions for the first 15s of exposure. The mean output signal in ADC counts was converted to an output signal in volts using the previously measured electronic gain $G_E = 0.03104 \pm 0.00010$ ADC counts/μV. The plot also shows the

corresponding standard deviation and DSNU for each integration period. It can be seen that the dark signal exhibits linear characteristics over this time period. The rate of change of the output voltage was measured by applying a linear least squares fit to the data. The least squares method does not account for the errors on the output signal so this was roughly estimated to be ± 0.5 mV/s. For CMOS001 the gradient was measured as m = 12.0 ± 0.5 mV/s. The dark signal N_D, in terms of electrons per pixel per second, was calculated using the responsivity R_{out} (volts/electron) determined previously in Chapter 6:

$$N_d = m / R_{out} \tag{7.8}$$

Therefore, at these lower signal levels, the CMOS001 gave a dark signal of 4000 ± 213 e^-/pixel/s. For comparison purposes this figure was further converted to an equivalent current per unit area (pA/cm^2) using:

$$I_D = (q_e m / R_{out} A_p) \times 10^{12} \tag{7.9}$$

The dark current of CMOS001 at room temperature was therefore 160 ± 9 pA/cm^2.

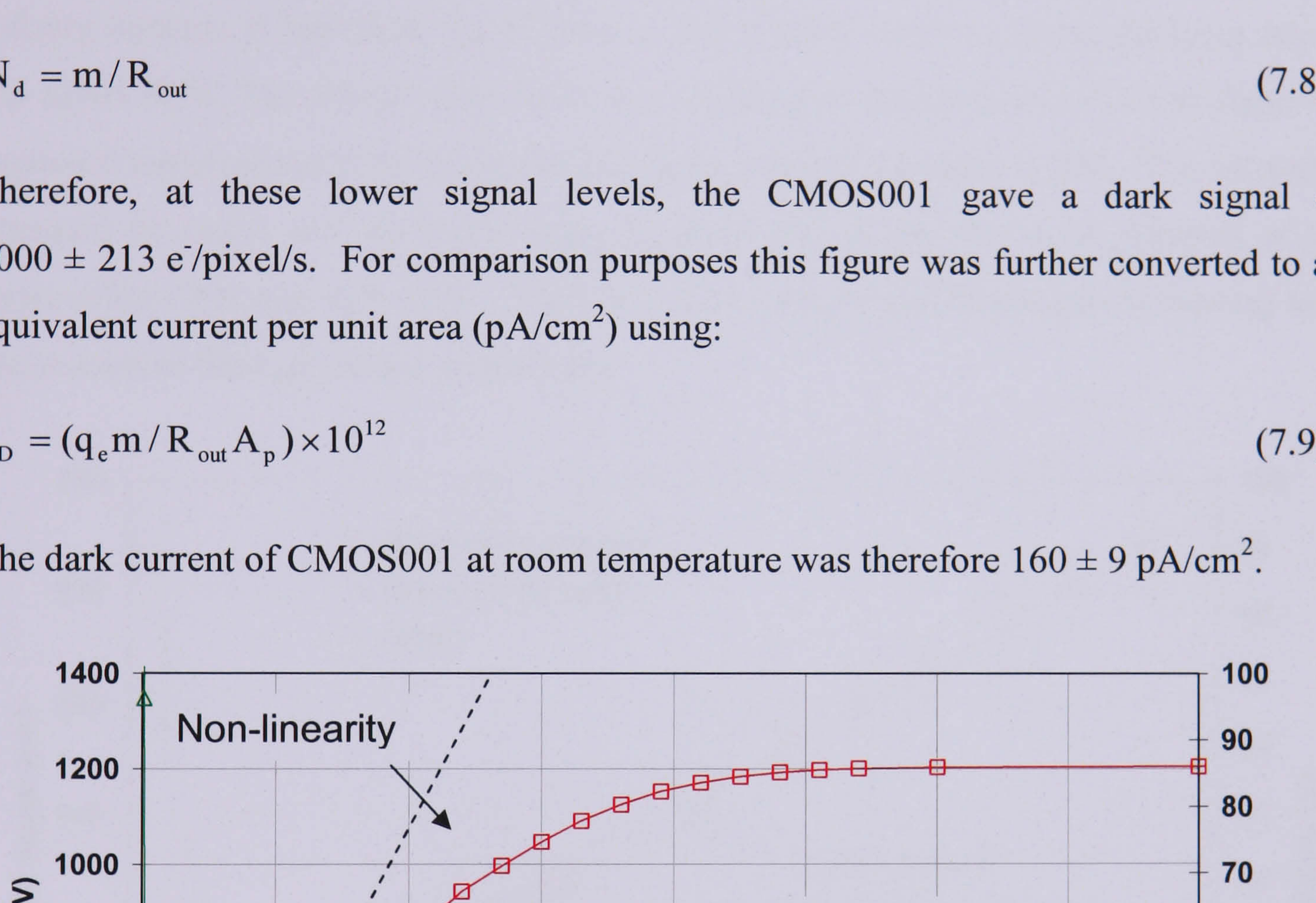


Figure 7.2 CMOS001 saturation due to dark current

Figure 7.2 shows the output voltage under dark conditions for CMOS001 plotted over a longer time period. The dark signal is seen to become non-linear with time. The non-linearity is caused by the increase in capacitance of the sense node as signal accumulates, as described previously in Chapter 6. The device reaches the saturation level after approximately 250s. It can be seen that some of the pixels in the device must saturate as early as 100s, as shown by the fact that the standard deviation peaks at 100s then begins to reduce. There are three components to the standard deviation and DSNU: the offset FPN, the dark FPN and the dark shot noise. The DSNU starts from infinity because at zero dark signal there is still a large variance across the array due to the offset FPN. The DSNU then decreases rapidly but than flattens off as it obeys the expected variation with the inverse of the square root of the mean signal. The measured standard deviation will be higher than expected due to the shot noise because of the extra offset FPN and dark FPN. Further work is required to investigate removing both these sources through image subtraction.

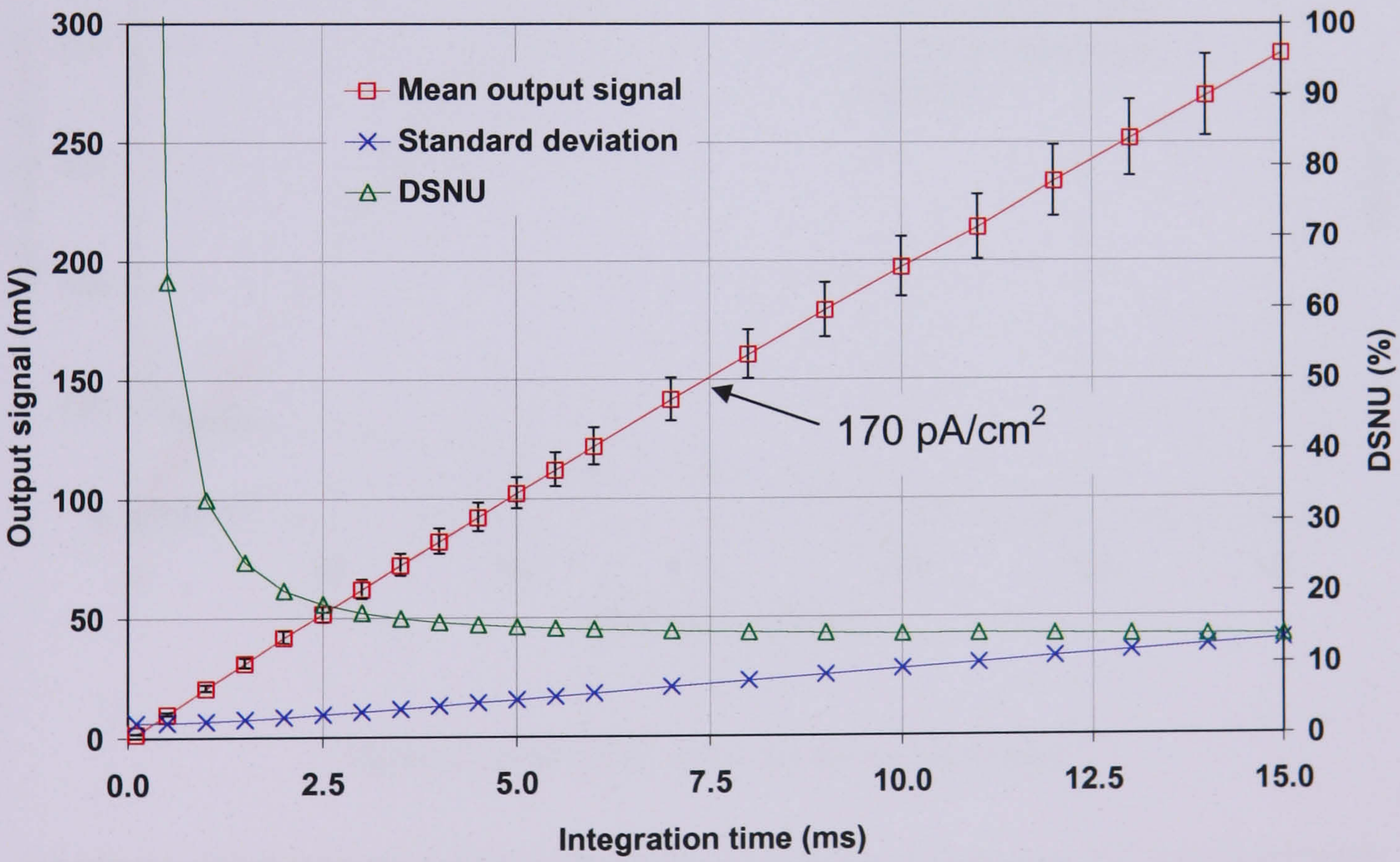


Figure 7.3 CMOS002 mean dark signal accumulation for the first 15 s of integration. The error on the mean output signal data is derived from the error in measured output signal in ADC counts, G_E and G_S

Figure 7.3 and **Figure 7.4** show the same dark signal measurements repeated for CMOS002. The same linear least squared fit technique used **Figure 7.1** of the data in **Figure 7.3** yielded a gradient m = 19.2 ± 0.5 mV/s. Using the responsivity of 4.7 μV/e^-,

measured previously for lower signal levels for CMOS002, yielded a value for the dark current of 4260 ± 294 e^-/pixel/s equal to 170 ± 12 pA/cm^2. **Figure 7.4** shows the dark signal for CMOS002 plotted over a longer time period. The dark signal is again seen to become non-linear with integration period. The device reaches the saturation level after 150s and some pixels saturate as early as 50s. A summary of the results from the room temperature characterisation of the Imaging Arrays is given in **Table 7.1**. The two different diode structures exhibit similar fundamental performance with the magnitude lying between that of an inverted mode (10 pA/cm^2) and normal mode (1 nA/cm^2) operation CCD. Although both diodes have a similar dark current the CMOS002 device saturates in a shorter time period because the responsivity is 50% higher. This will significantly reduce the dynamic range compared with CMOS001.

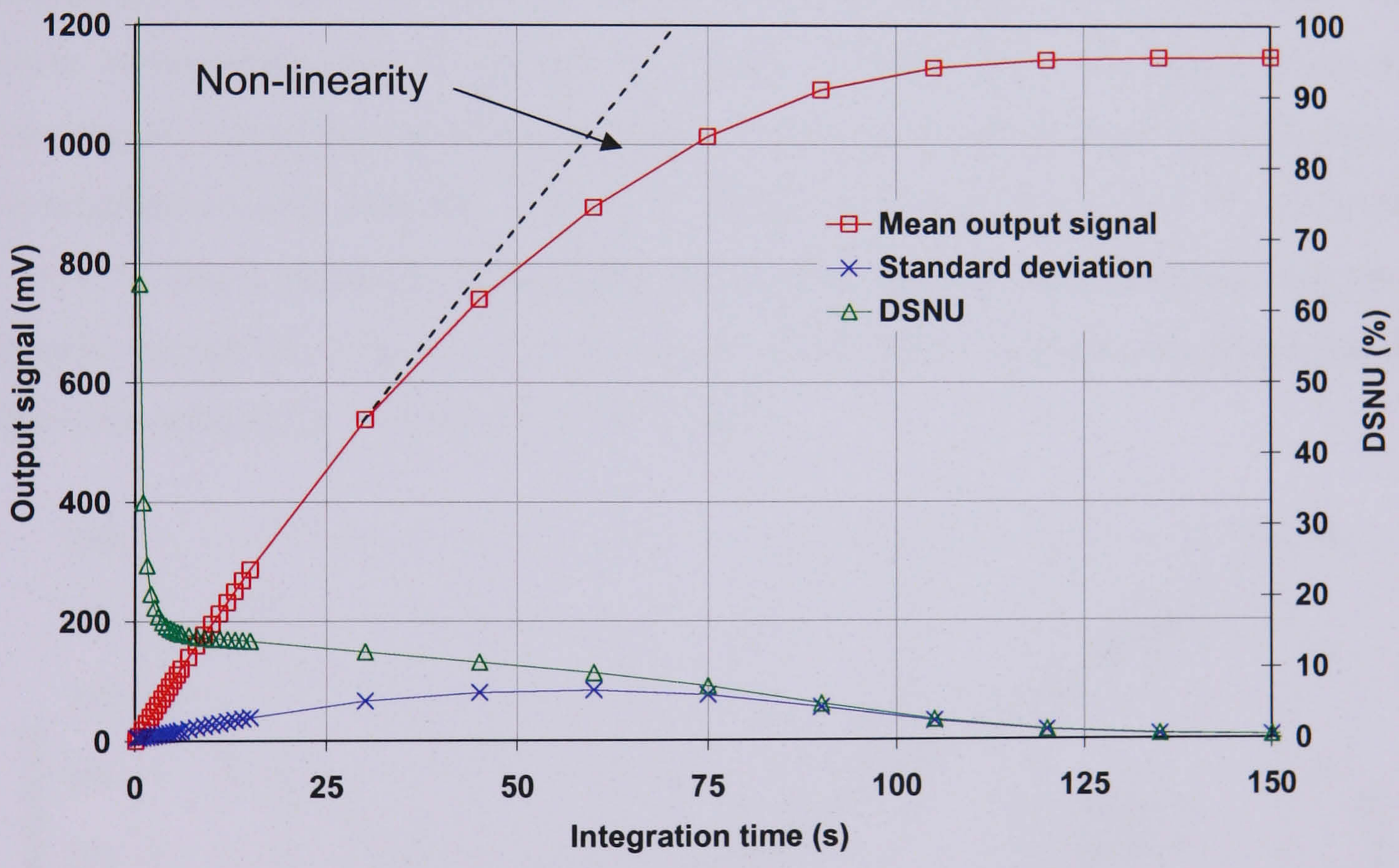


Figure 7.4 CMOS002 saturation due to dark current

Device	Photodiode type	Responsivity ($\mu V/e^-$)	dV_{out}/dt (mV/s)	N_D (e^-/pixel/s)	I_D (pA/cm^2)
CMOS001	n+/p-well	3.0	12.0 ± 0.5	4000 ± 213	160 ± 9
CMOS002	n-well/p-sub	4.5	19.2 ± 0.5	4260 ± 294	170 ± 12

Table 7.1 Imaging Arrays room temperature dark signal characterisation summary

7.3.3. Low temperature measurements

The previous room temperature measurements were simply an initial investigation with a lack of temperature control and stabilisation. As it is not possible to directly compare the performance of different devices if there are significant temperature differences, subsequent measurements of the Imaging Arrays utilised the e2v cold characterisation facility described in Chapter 5.

A vacuum based system is required to prevent the formation of condensation or ice on the sensor causing damage at low temperatures. Before the system was used a temperature calibration was performed using a dummy chip with a PT100 platinum resistance thermometer (PRT) bonded. This enabled comparison of the actual device temperature with that measured by the primary PRT bonded to the cold plate. The results of the temperature calibration are shown in **Figure 7.5**. The figure shows that there was an increasing temperature difference between the device and the cold plate as the temperature was reduced. Dataset 1 shows there was 17.5 ± 2.1 °C difference at −100 °C due to parasitic thermal loads in the test device. A second dataset was taken after the connection between the chip and the cold finger had been improved and the difference reduced to ~ 10.4 ± 2.1 °C at − 100°C.

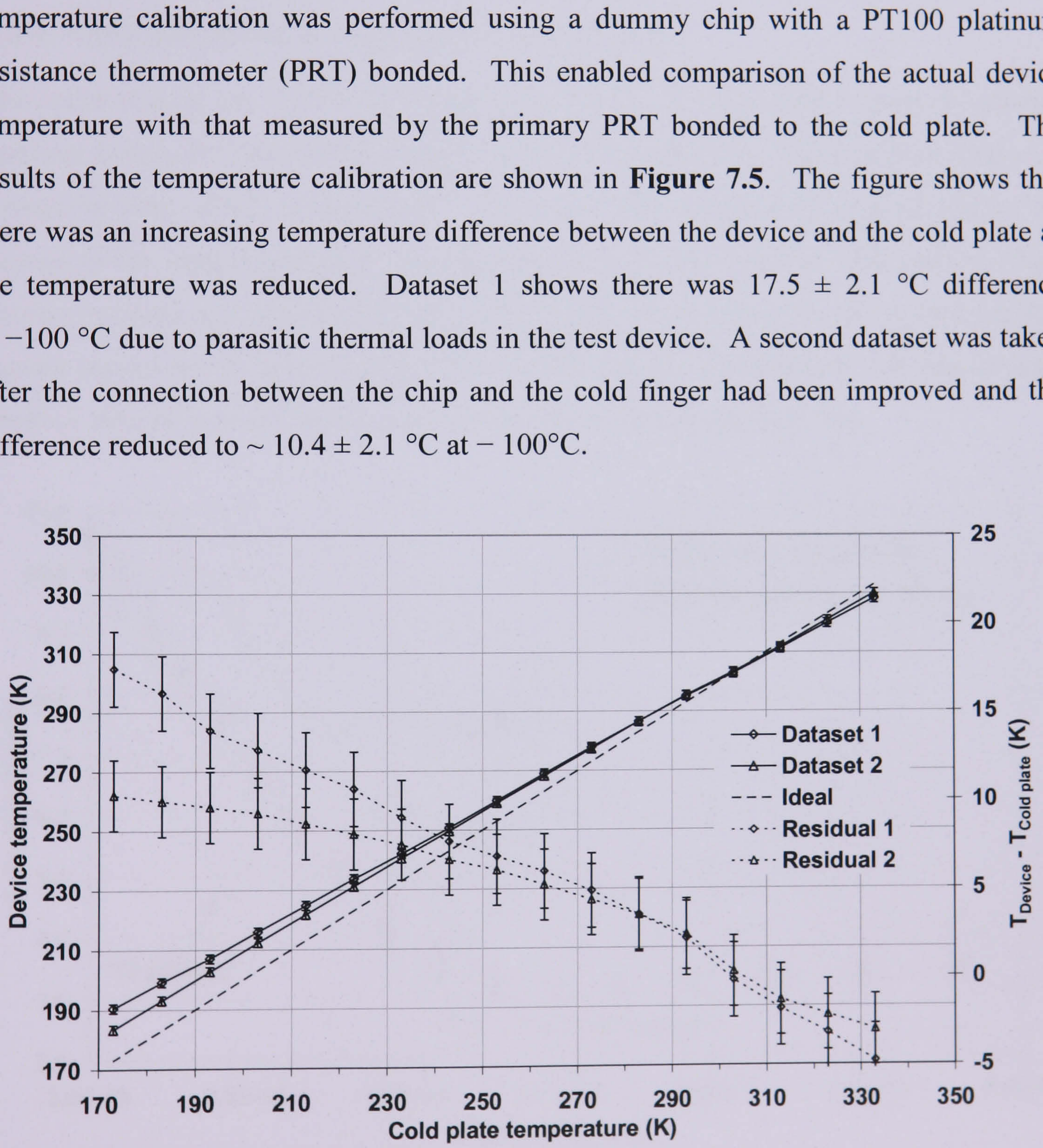


Figure 7.5 Cold characterisation facility temperature calibration using the dummy device with PT100 PRT bonded

After the temperature calibration the dark signal was characterised for both Imaging Arrays from –100°C to +60°C in 10°C steps. The bias conditions were maintained at the same values as the previous measurements. At each temperature an offset image was read out with zero integration and then a long exposure was acquired to allow the dark signal to accumulate. The exposure time was increased from 1s to 300s as the temperature decreased to allow a measurable amount of dark signal to accumulate. In addition to the dark images a series of illuminated diagnostic images were acquired at –100°C to confirm correct photo-response. The photo-response data showed similar behaviour to that seen in the initial functional testing described in Chapter 6.

7.3.4. Low temperature results and discussion

The mean dark signal across the central 100×100 pixels, calculated using the method used previously for each temperature, is shown in **Figure 7.6**. The data is plotted as an Arrhenius plot, which is the natural log of the dark signal (N_d) plotted against the inverse of the temperature (K). Thus a linear curve shows that the dark current obeys the theory (with the exponential term dominating). Also shown are the theoretical dark current curves for an inverted mode (10 pA/cm^2 at room temperature) and non-inverted mode (1 nA/cm^2 at room temperature) CCD plotted using Equation 7.6.

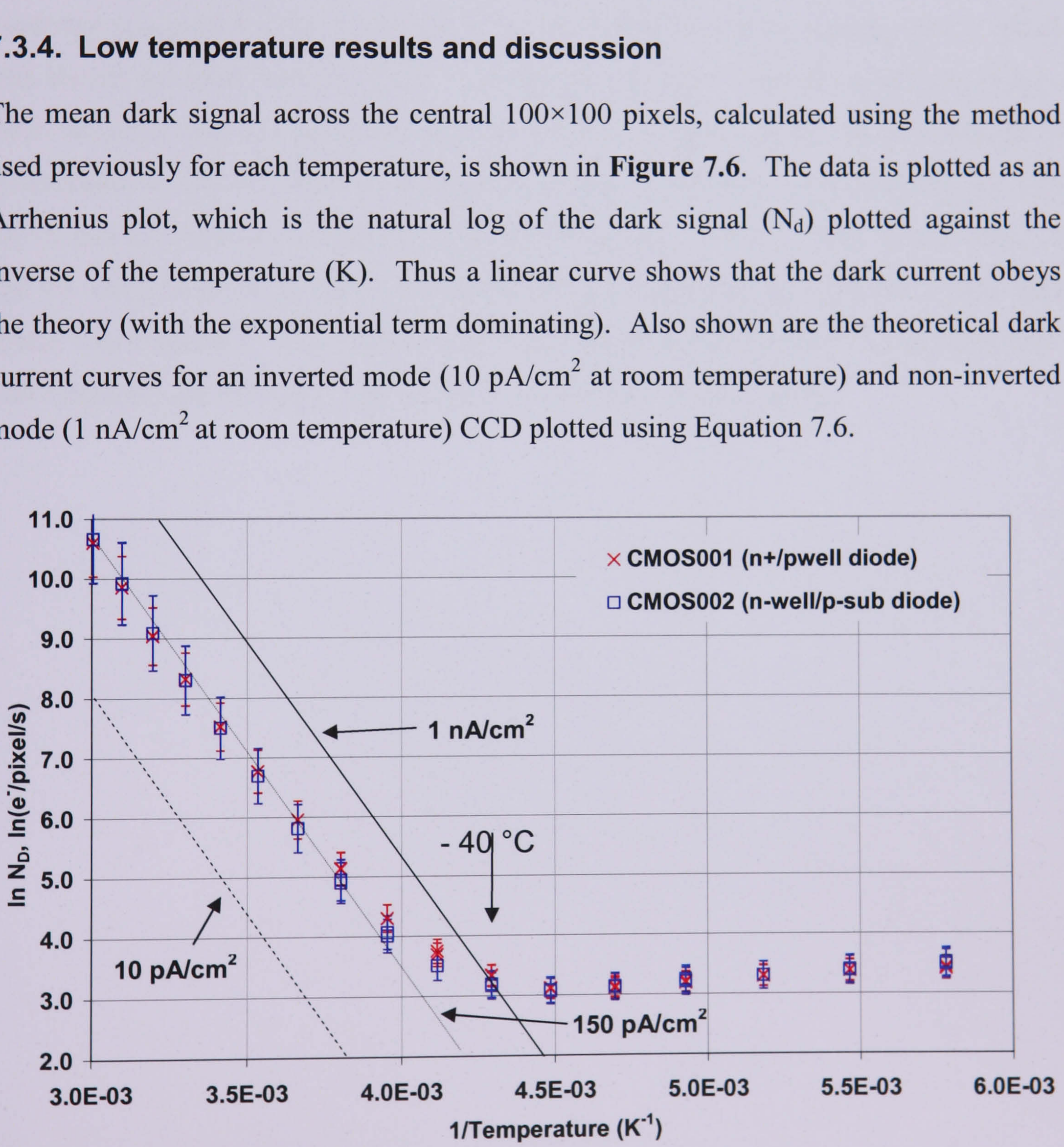


Figure 7.6 Dark signal variation with temperature for the Imaging Arrays

A fit to the data was applied using a theoretical curve with a room temperature dark current of 150 pA/cm^2. The plot shows a good fit to both sets of data from T = −10°C to 60°C and the dark signal is seen to double for approximately every 10°C change. However below −10°C the dark current begins to level off and reduce no further. This deviation from the normal curve could be accounted for partially by the large errors at these low signal levels, but there is a clear trend towards a levelling off the dark current. It may be that there was light leaking into the system, but this was checked rigorously at all interfaces e.g. at interconnections. It could also be that the device was not cooling down to the temperature indicated by the sensor on the cold head due to a poor thermal contact, but the two datasets from the dummy device shows this should not have been the case. To improve the errors multiple images could have been acquired and averaged to improve the poor statistics of the lower temperature measurements, but this was not attempted. Similar behaviour was observed in an APS developed for charged particle imaging (Takayanagi et al., 2003). A possible source of the low temperature dark signal saturation was not discovered until the Test Pixels dark signal was evaluated. This extra source was found to be due to "Hot-Carrier Injection" and a detailed description is outlined in the remainder of this chapter.

7.4. Test Pixels dark signal: Initial investigation

The characterisation of dark signal using the Imaging Arrays provided an initial understanding of the dark signal behaviour of the new devices and the basic properties of the TS50 process. The same pixel designs in the Test Pixels were then investigated to examine performance in more detail in the expectation that the results from the variety of smaller scale test structures would be scaleable to larger array sizes.

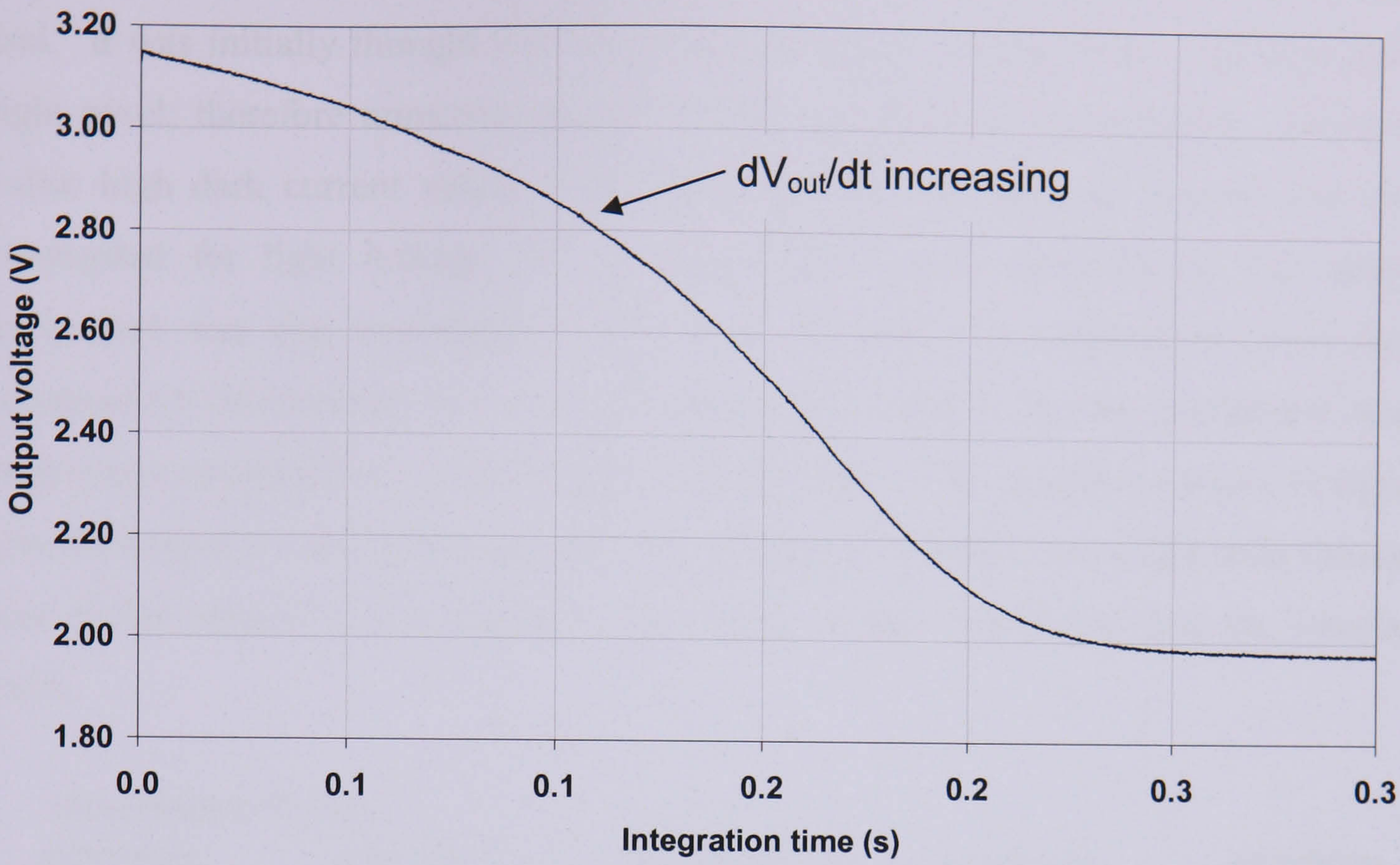
The initial approach to dark signal characterisation of the Test Pixels was to select and periodically reset a given pixel within the array and to continuously sample the output under dark conditions. The leakage rate was then calculated by measuring the rate of change of voltage with time and converting to a current value using the responsivity measured from previous work. An example waveform sampled from a pixel within the Test Pixels 1 quadrant, containing the same pixel design as CMOS001, is shown in **Figure 7.7a**. At room temperature the time to saturate the pixel is less than 1 s, which implies a much higher leakage rate relative to that measured with the Imaging Arrays. The initial and maximum rates of change of the dark signal were calculated by using a linear least squares fit to different narrow regions of the waveform. A summary of the range of leakage rates and corresponding leakage currents is given in **Table 7.2**.

Dark signal	dV_{out}/dt (V/s)	N_D (ke^-/pixel/s)	I_D (nA/cm^2)
Test Pixels 1 (initial)	1.8	600	24
Test Pixels 1 (maximum)	9.6	3200	128
CMOS001	0.012	4	0.16

Table 7.2 Test Structures initial dark signal characterisation summary

The dark signal is clearly much higher than in the Imaging Arrays. A further difference was evident from the characteristic shape of the waveform. The rate of change of voltage increases as the diode discharges. Previous behaviour for the CMOS001 pixel (shown in **Figure 7.7b**) was for the discharge rate to decrease as the diode voltage decreases. This occurs because the photodiode depletion capacitance increases as signal accumulates, thereby reducing the conversion gain of the pixel.

a)



b)

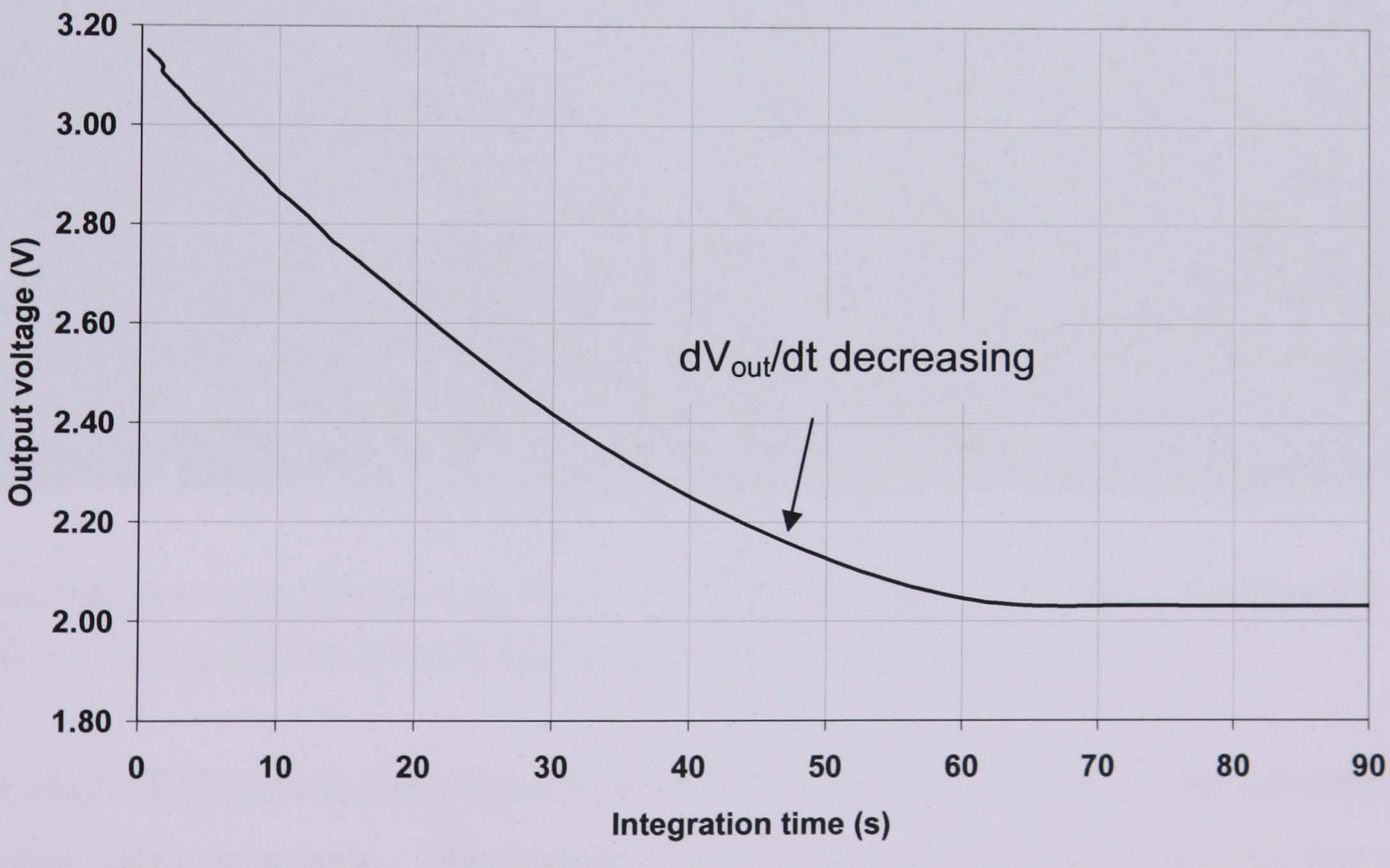


Figure 7.7 a) Initial dark signal from Test Pixels 1A and **b)** from CMOS001 containing the equivalent pixel design

There is clearly a large discrepancy between the dark signal characteristics of the scanned Imaging Arrays and the Test Pixels, when continuously sampling a single pixel. It was initially thought that the high dark signal could be due to an anomalous bright pixel; therefore numerous pixels of the same design were sampled. However similar high dark current values were measured. The measurement system was then investigated for light leakage but no stray light sources were found. The device temperature was also investigated, as a major difference in temperature could have accounted for the increase, however the devices were found to operate in a similar room temperature environment to the Imaging Arrays. Once these possible sources of signal were eliminated, it was postulated that the difference in behaviour might arise through some factor related to the different sequencing of the Test Pixels and the Imaging arrays.

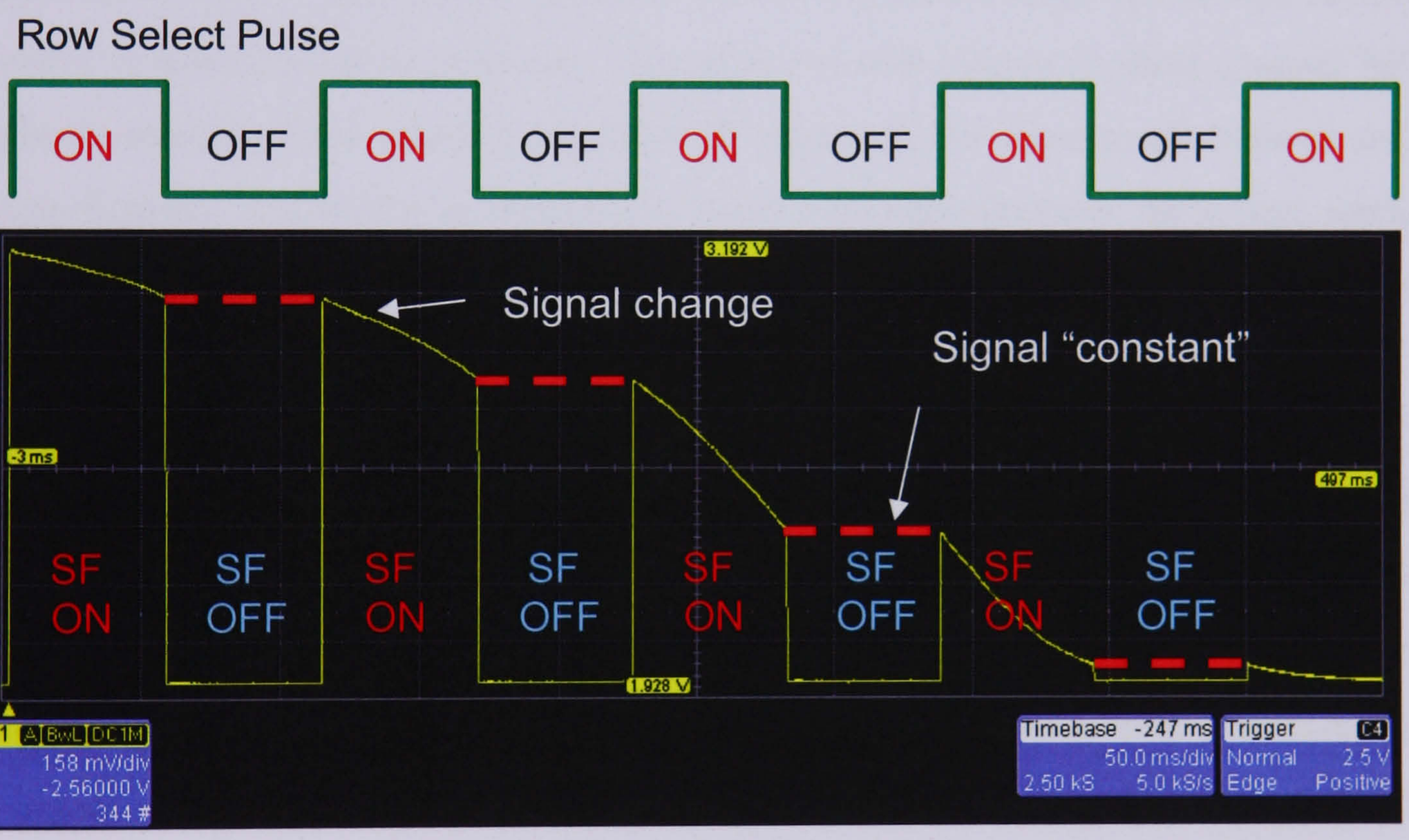


Figure 7.8 Oscilloscope trace showing characteristic APS dark signal output voltage waveform with row select transistor enabled and disabled (source follower (SF) on and off)

The major difference in operation of the devices was time duration of the activation of the row select transistor. The Imaging Arrays were operated such that the row was selected only during the readout phase at the end of integration. The Test Pixels were operated with the row constantly selected to enable constant viewing of the output waveform on the oscilloscope. The increase in dark signal therefore appeared to be highly dependent on activation of the row select transistor. The sequencing for the Test

Pixels was adjusted to clock the row select at regular intervals after the initial reset. The effect of enabling the row select transistor is demonstrated by the dark signal trace shown in **Figure 7.8**. When the select transistor is enabled the pixel is observed to discharge rapidly until the row is deselected and the pixel is disconnected from the oscilloscope input. However, when the row is re-selected the pixel output appears to resume at the same level as when it was previously accessed, implying a much lower dark signal when the select transistor is disabled.

Further investigation of the literature found that, during read-out, the CMOS Pixel is potentially vulnerable to an extra source of dark signal due to minority hot-carrier injection from the in-pixel follower transistor (Wang and Sodini, 2001, Maestre et al., 2003, Hsu et al., 2004). The most viable source of the extra dark signal was therefore thought to be due to hot-carrier injection within the pixel, when the source follower transistor is selected during read-out. The effect is well known in short channel MOS transistors used in digital integrated circuit (IC) devices, but these small currents are of no significance. The effect is potentially much more problematic for image sensors because the small parasitic current generated is collected by the photodiode region and contributes to the measured output signal.

As the literature showed that little work had been carried out on the nature of the effect in CMOS pixels, a detailed investigation into the hot-carrier effect on the Test Structures dark signal was carried out using the Test Pixels. The following sub-sections outline the findings of the investigation and discuss the implications for producing low dark signal sensors.

7.5. Test Pixels: Hot-Carrier effects

The "hot carrier" effect is an extra source of parasitic current within a CMOS pixel in addition to the conventional diode leakage current described earlier. The effect is well known in short-channel MOSFETs and has been observed by many groups for a number of years. Image sensors are particularly sensitive to the effect as accurate image reproduction depends critically upon the collection of photo generated free carriers and the minimisation of the collection of any other parasitic currents. The problem was originally observed in the output amplifiers of CCD image sensors (Janesick and Elliot, 1987). However, the small number of groups mentioned previously has only recently investigated the effect on the operation of CMOS pixels. Active pixels are more susceptible to the effect due to the presence of transistor circuitry within the pixel.

7.5.1. Theoretical background

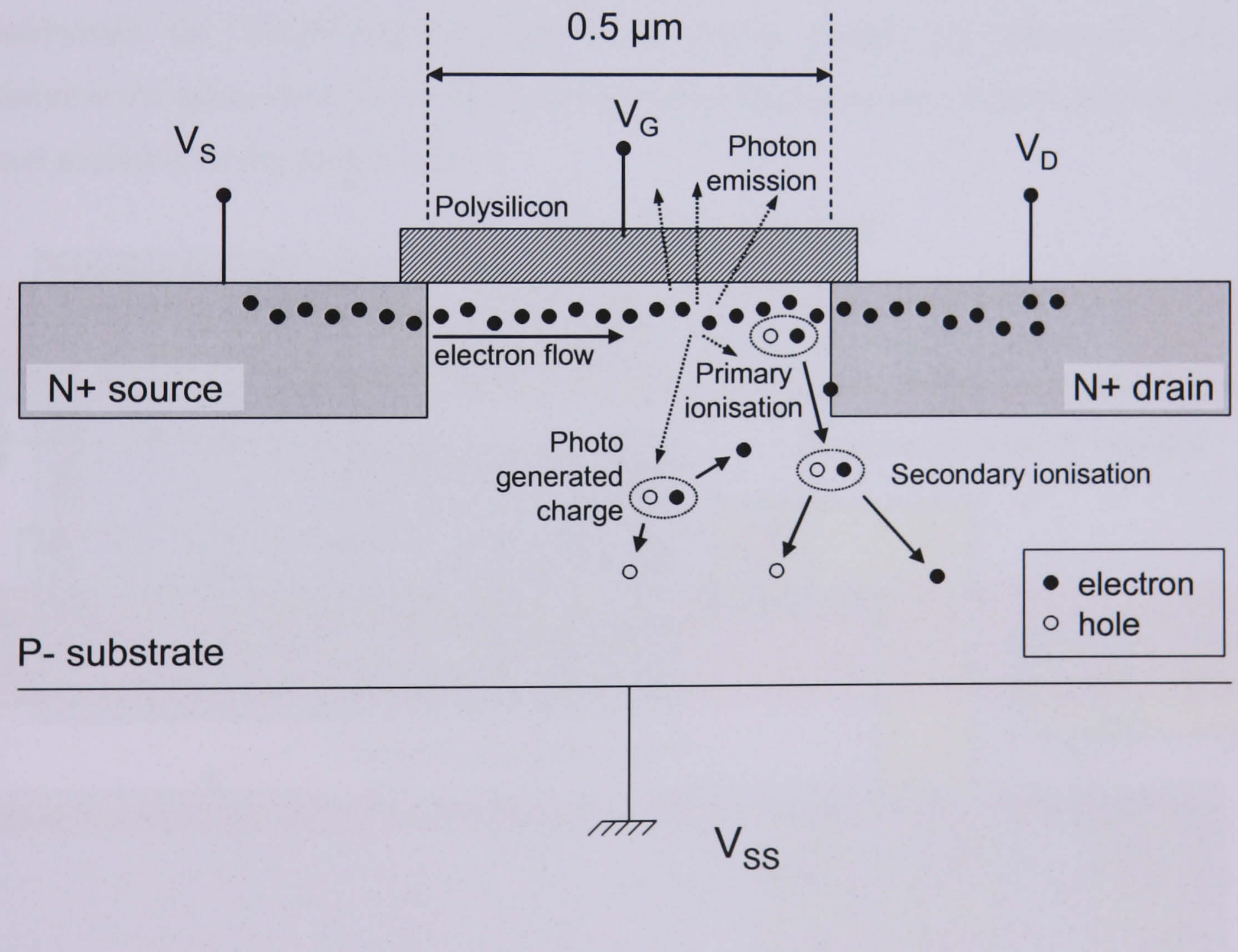


Figure 7.9 Cross section of an MOS transistor showing the source of the hot-carrier effect

A cross section of a standard n-channel enhancement-mode MOSFET is shown in **Figure 7.9**. Electrons are accelerated between the source and drain terminals by the strong electric field within the channel region of the transistor. The electric field

increases towards the drain terminal and close to this region the electrons have significant amounts of kinetic energy. Such electrons, which have much greater energy than the equilibrium level for the temperature of the surrounding bulk semiconductor, are known as "hot electrons". The presence of hot carriers leads to two phenomena within the substrate material. Firstly, the hot electrons are able to ionise surrounding silicon atoms and create additional electron-hole pairs (Matsunaga and Kohyama, 1978), and it is also possible that the newly freed electron can have enough remaining energy to cause a further secondary impact ionisation. Secondly, by virtue of black-body radiation, the hot electrons can emit near infra red (NIR) photons ($\lambda \sim 1000$ nm) which can travel through the silicon and generate electron-hole pairs through the photo-electric effect (Toriumi et al., 1987, Lacaita et al., 1993). The combination of these two processes is referred to as hot-carrier electro-luminescence. The effects tend to worsen as the channel length of the transistor reduces because the supply voltage, and hence the electric field strength, does not scale proportionately with minimum feature size. This is problematic for CMOS pixels because short channel lengths are commonly used to minimise the space occupied by the transistors and maximise the surface area within the pixel available to the photodiode.

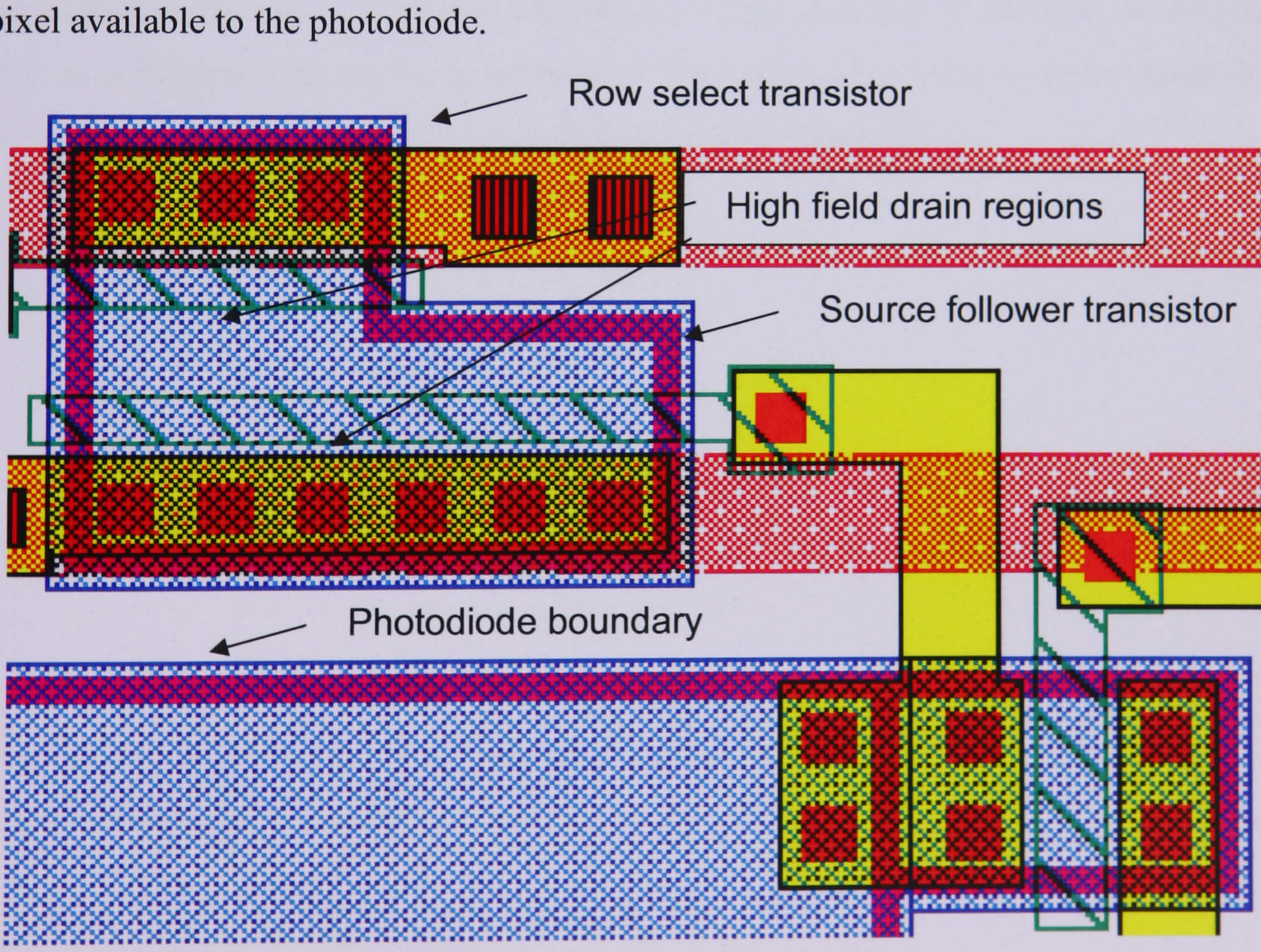


Figure 7.10 CAD schematic showing the layout of the readout region used in the Test Structures

Figure 7.10 shows the common layout of the readout region used in the majority of the Test Structures. The channel length of the follower and the enable transistors is 0.5 μm, the minimum feature size of the manufacturing process, and therefore high electric fields are present. The transistors are also located close to the photodiode collection region and therefore minority carriers generated in the substrate due to the two previously mentioned phenomena can easily migrate to the sense node and contribute to the measured signal. The 3T pixel is clearly susceptible to the hot-carrier effect and the following sections describe an investigation into the effect of the bias conditions and pixel layout on overall dark signal performance.

7.5.2. Effect of electric field in follower transistor

The initial investigation into dark signal concluded that the dark signal anomaly was due to activation of the row select transistor, which in turn activates the in-pixel follower transistor. The main difference between the waveforms shown in **Figure 7.7** is the evolution of the dark signal rate as the pixel discharges. The normal leakage behaviour is essentially linear with time but shows a decreasing rate due to the capacitance non-linearity of the photodiode. The increase in the rate of discharge shown in **Figure 7.7a** can be understood by considering the drain-source voltage (V_{DS}) of the follower transistor as the pixel discharges (see **Figure 7.11**).

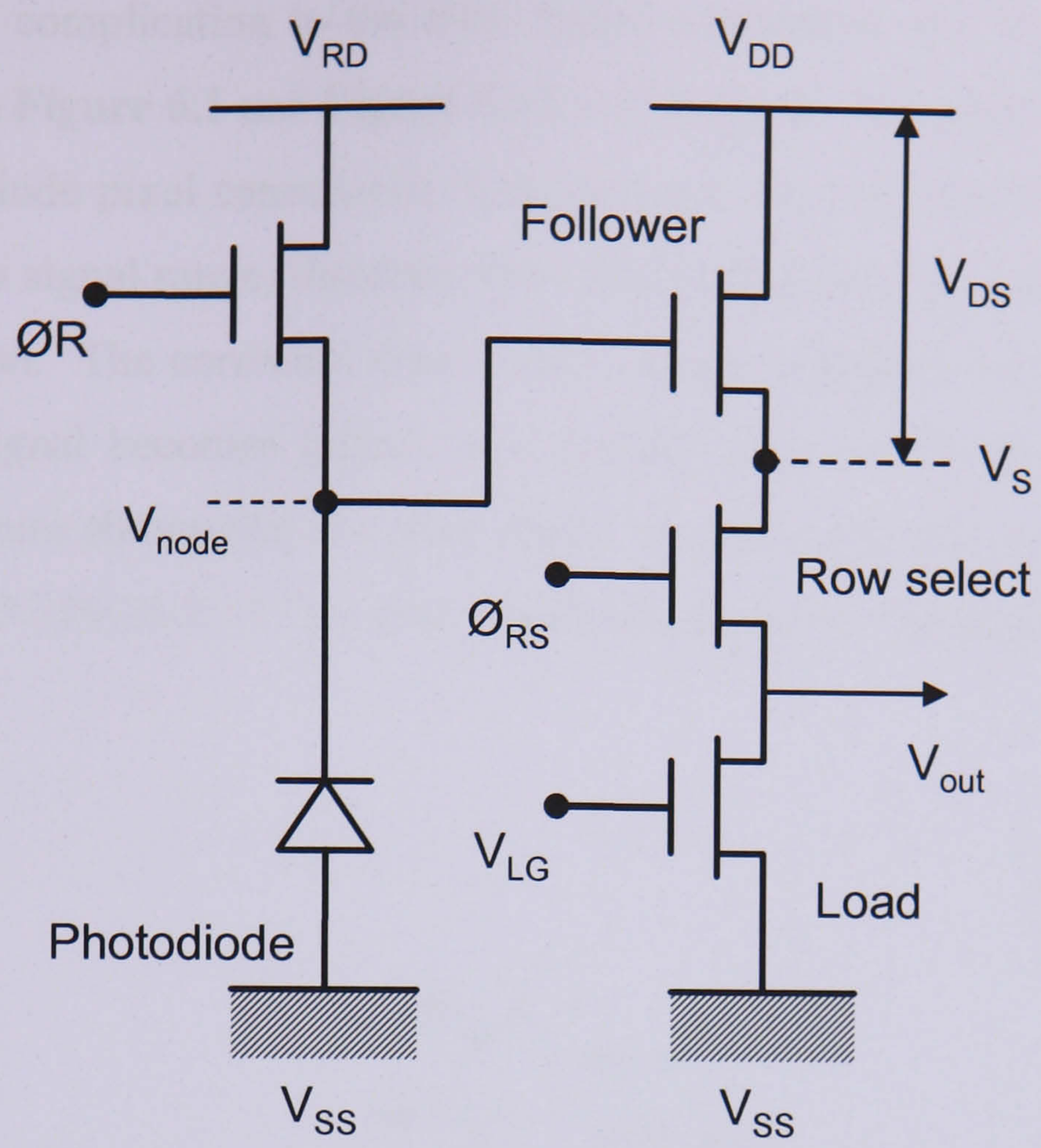


Figure 7.11 The electric field in the source follower transistor is determined by the bias conditions of the active pixel sensor

As the photodiode accumulates signal the gate voltage of the follower transistor reduces and the source voltage follows. Therefore, as the supply voltage V_{DD} is fixed, the drain-source voltage V_{DS} increases as any signal accumulates on the diode. The electric field consequently increases and the electrons in the channel are accelerated to a higher velocity and they acquire more kinetic energy. This explains why the rate of discharge increases as the diode discharges. The hot-carrier injection is thus clearly highly dependent on the instantaneous bias conditions of the follower transistor and therefore a more detailed investigation was performed to characterise the effect.

The dependence of the electric field on the hot-carrier effect was investigated further using Test Pixels 1A. The output voltage was sampled under dark conditions with the row select transistor permanently enabled. The instantaneous discharge rate as a function of output voltage was calculated by measuring the gradient of the curve for a range of output voltages between reset and saturation. The dark signal was then calculated for each output voltage using the same method used in section 7.3. The instantaneous dark signal plotted as a function of output voltage is shown in

Figure 7.12. A complication to the dark signal calculation was the responsivity non-linearity seen in **Figure 6.1** and **Figure 6.12** in Chapter 6. Between reset and saturation the n+/p-well diode pixel capacitance increases and the responsivity reduces by ~ 0.5 $\mu V/e^-$ across the signal range, therefore the varying responsivity must be accounted for in the calculation. The corrected data is also shown in **Figure 7.12**. One can observe that the dark signal becomes higher than initially seen for the lower output voltage values. The figure shows that the dark signal increases linearly as the output voltage decreases from 3.25V to 2.5V but then rapidly decreases as the pixel saturates between 2.5V and 2.0V.

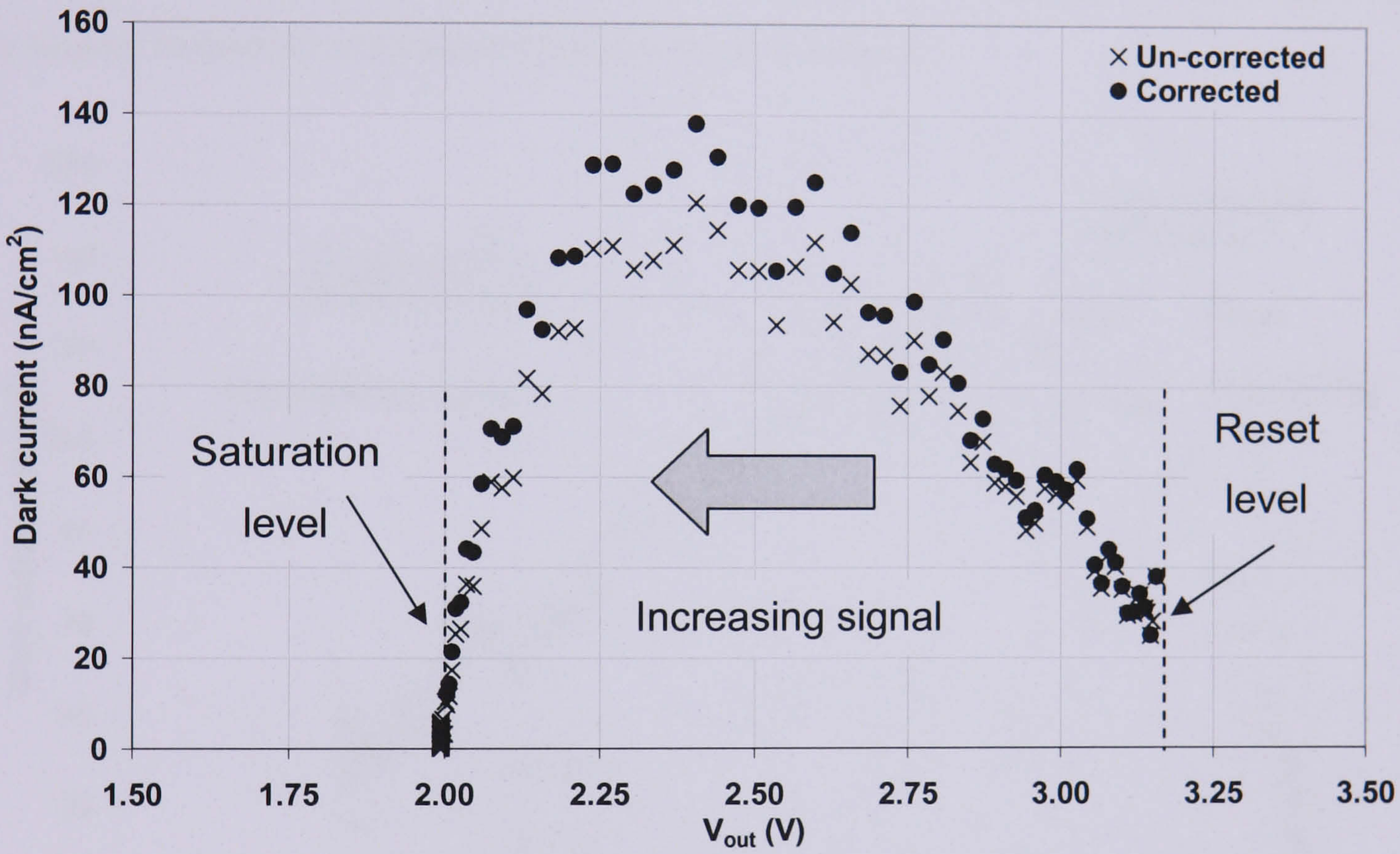


Figure 7.12 Plot of leakage current vs. output voltage with all other biases constant

If the dark signal as a function of output voltage is known, it is possible to calculate the dark signal as a function of V_{DS} and subsequently the electric field. The drain source voltage is related approximately to the output voltage by the expression:

$$V_{DS} = V_{DD} - \frac{(V_{out} - V_{GS})}{G_{SF}} \tag{7.10}$$

where G_{SF} is the gain of the source follower. The expression holds true because the extra p-channel output follower means that output voltage is approximately the same as the diode voltage, therefore V_{DS} is the difference between the diode voltage minus the

gate source drop across the follower transistor. V_{DS} for each output voltage was calculated using a simulated value for V_{GS} of 1.55V, V_{DD} = 5V and G_{SF} = 0.68. **Figure 7.13** shows the dark signal plotted as a function of the drain source voltage of the follower. As the V_{DS} is known, the electric field in the follower can also be approximated by dividing the voltage by the channel length, L = 0.5 μm. The dark signal is plotted as a function of electric field in **Figure 7.14**. As only a simple linear approximation for the electric field is used the data show the same dependence on the electric field as V_{DS} and the dark signal increases as the electric field increases. This would be expected as the energy distribution of carriers should have a higher mean level therefore more carriers will become hot and contribute to increased dark signal through the impact ionisation and electro luminescence processes.

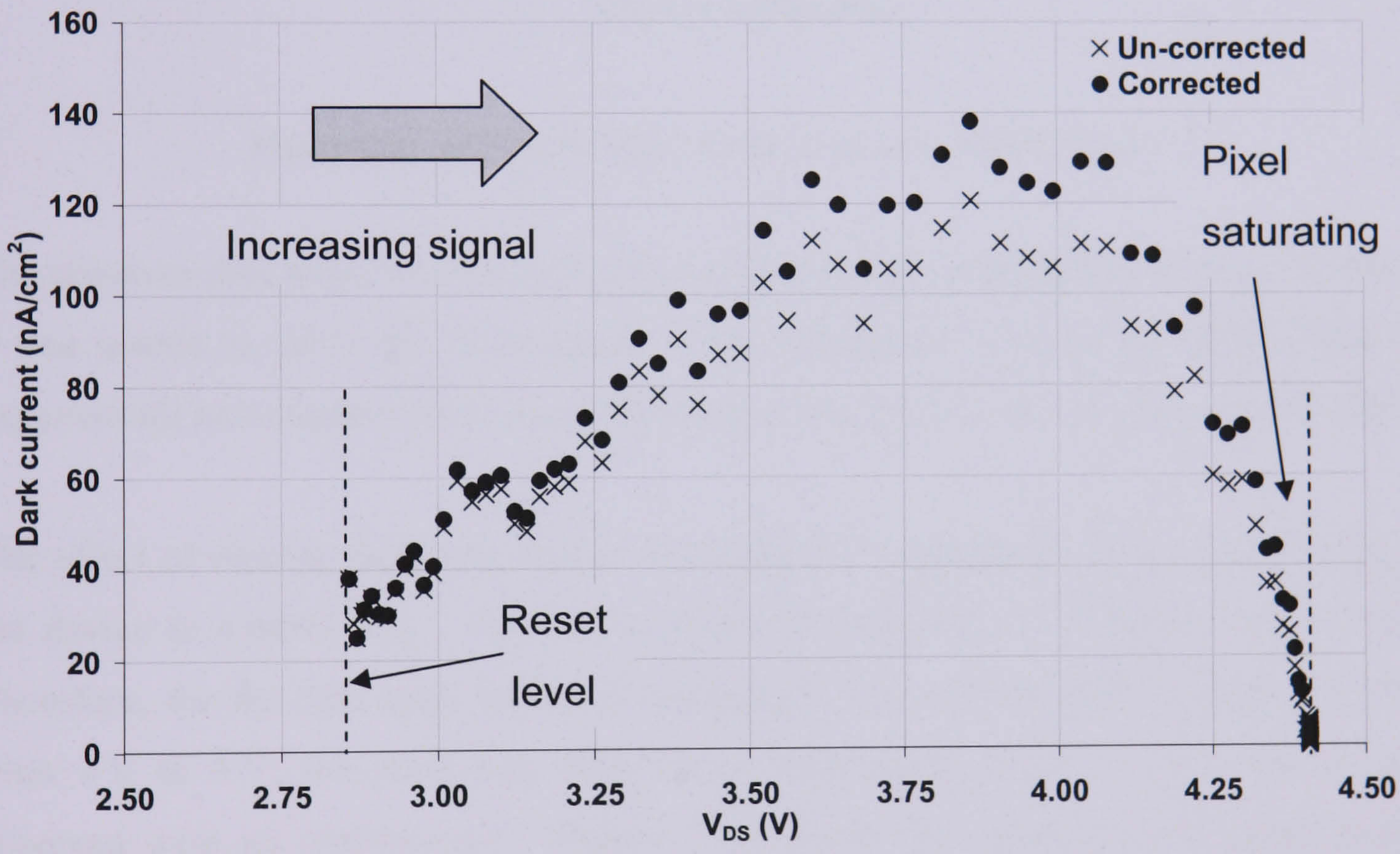


Figure 7.13 Plot of dark signal against source follower V_{DS} (non-linearity corrected and un-corrected).

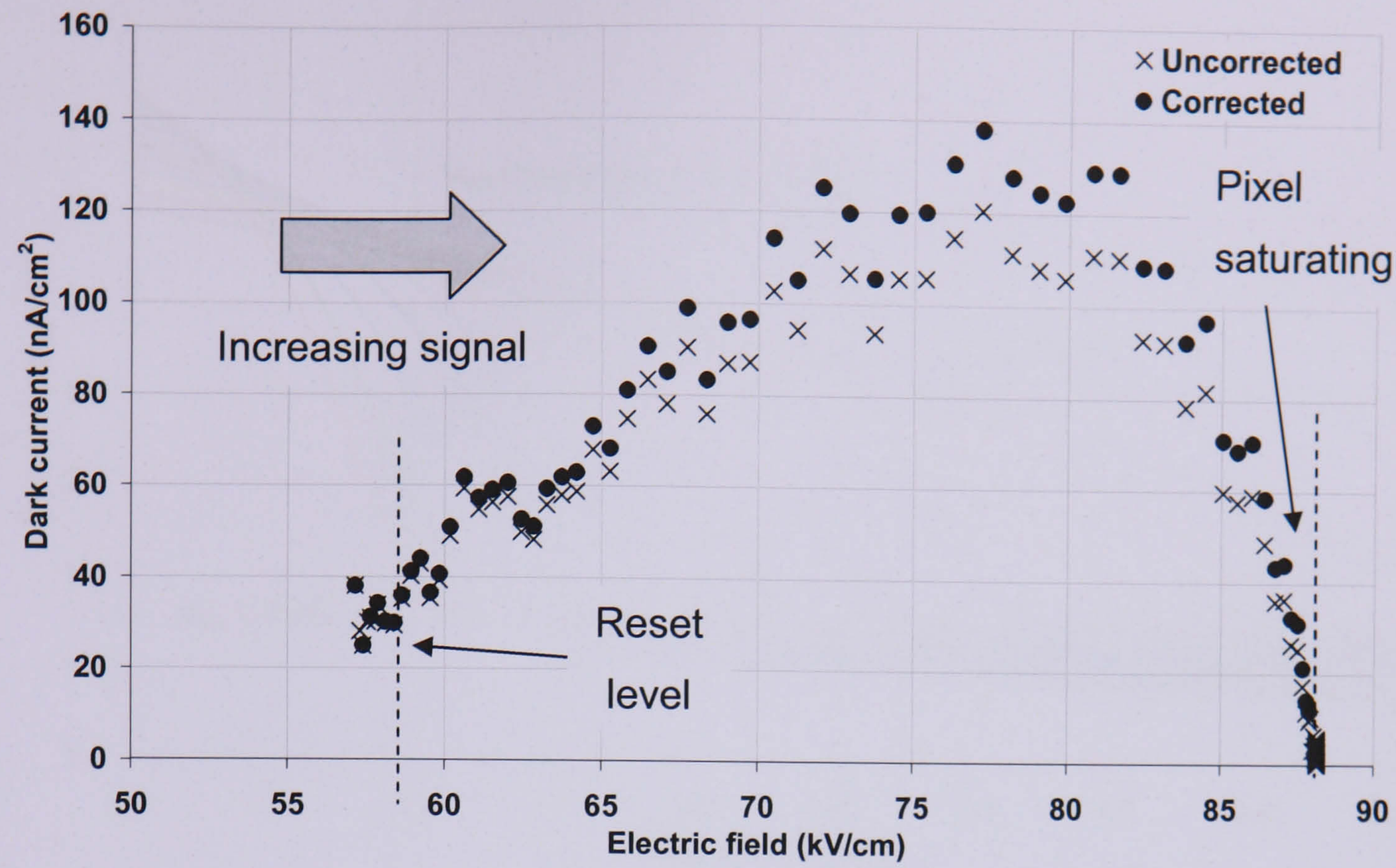


Figure 7.14 Dark signal variation with mean electric field (V_{DS}/L)

The previous data show that the hot-carrier effect is highly dependent on V_{DS}, however it was unable to show the exact nature of the dependency on electric field (linear or exponential) and whether there was a threshold level determining the onset of the effect.

The effect of electric field was further investigated by adjusting the bias conditions of the device to control V_{DS}. V_{DS} can be manually adjusted by changing V_{DD} or V_{RD}. Therefore, for the next stage of the investigation, V_{DD} was adjusted in steps of 0.1 V from 4 V to 5 V, the pixel was reset and a dark signal trace for each setting was observed with an oscilloscope. **Figure 7.15** shows the range of dark signal traces obtained. One can see that the dark signal rate is strongly dependent on the drain voltage supplied to the chip. The dark signal was then calculated (for a fixed output voltage of 2.5 V) for each value of the V_{DD}. The results are shown in **Figure 7.16**. The data show that the effect may have an exponential rather than linear dependence on V_{DD}, and hence V_{DS}, and that there may be a threshold value below which the effect is minimal. However the lowest dark signal measured is still an order of magnitude higher than that seen in CMOS001. Further investigation required a wider range of V_{DS} values using the higher V_{RD} possible with the p-channel reset devices and is described later in this section.

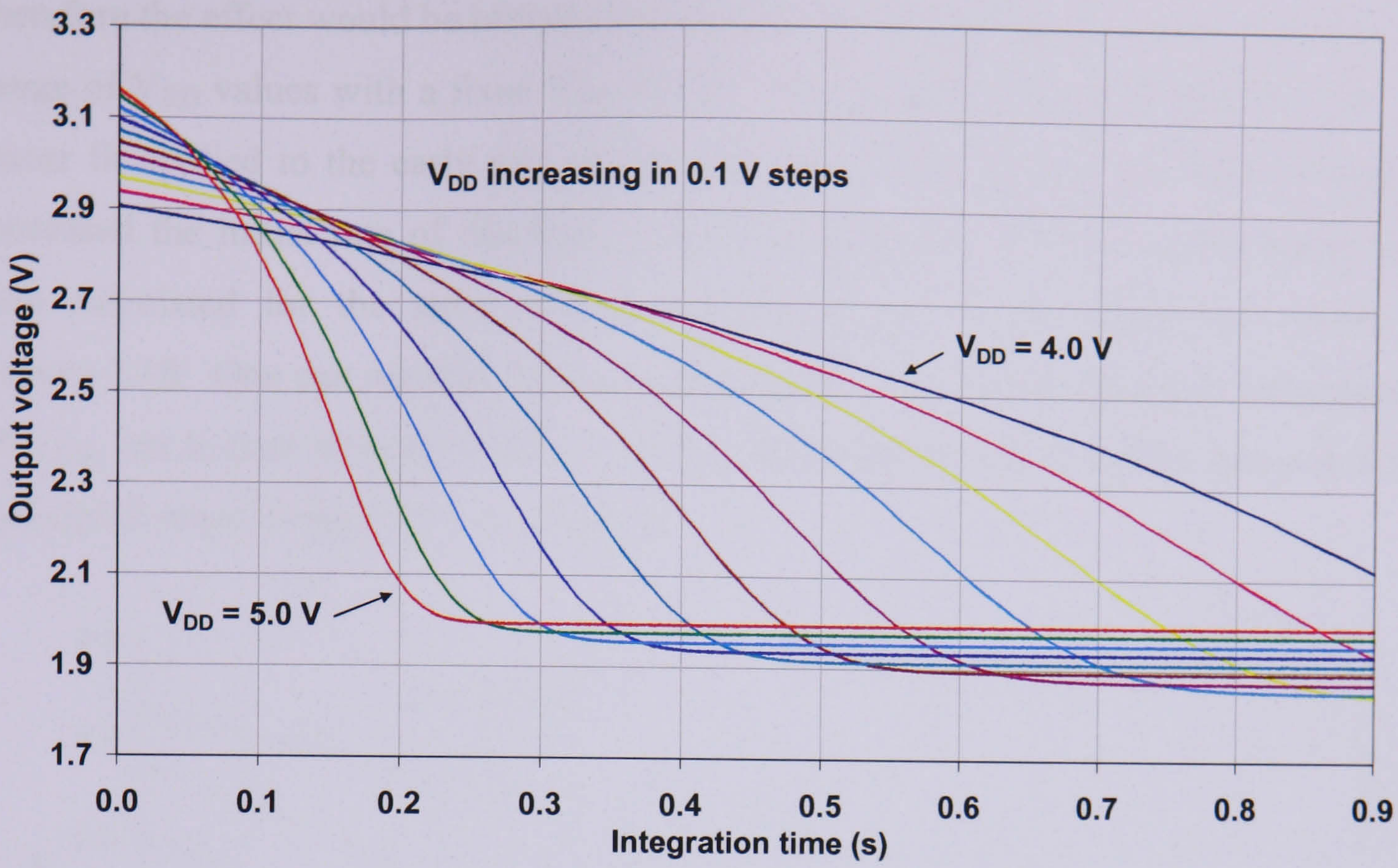


Figure 7.15 The variation of dark signal vs. time, with pixel supply voltage V_{DD} = 4 to 5 V in 0.1 V steps

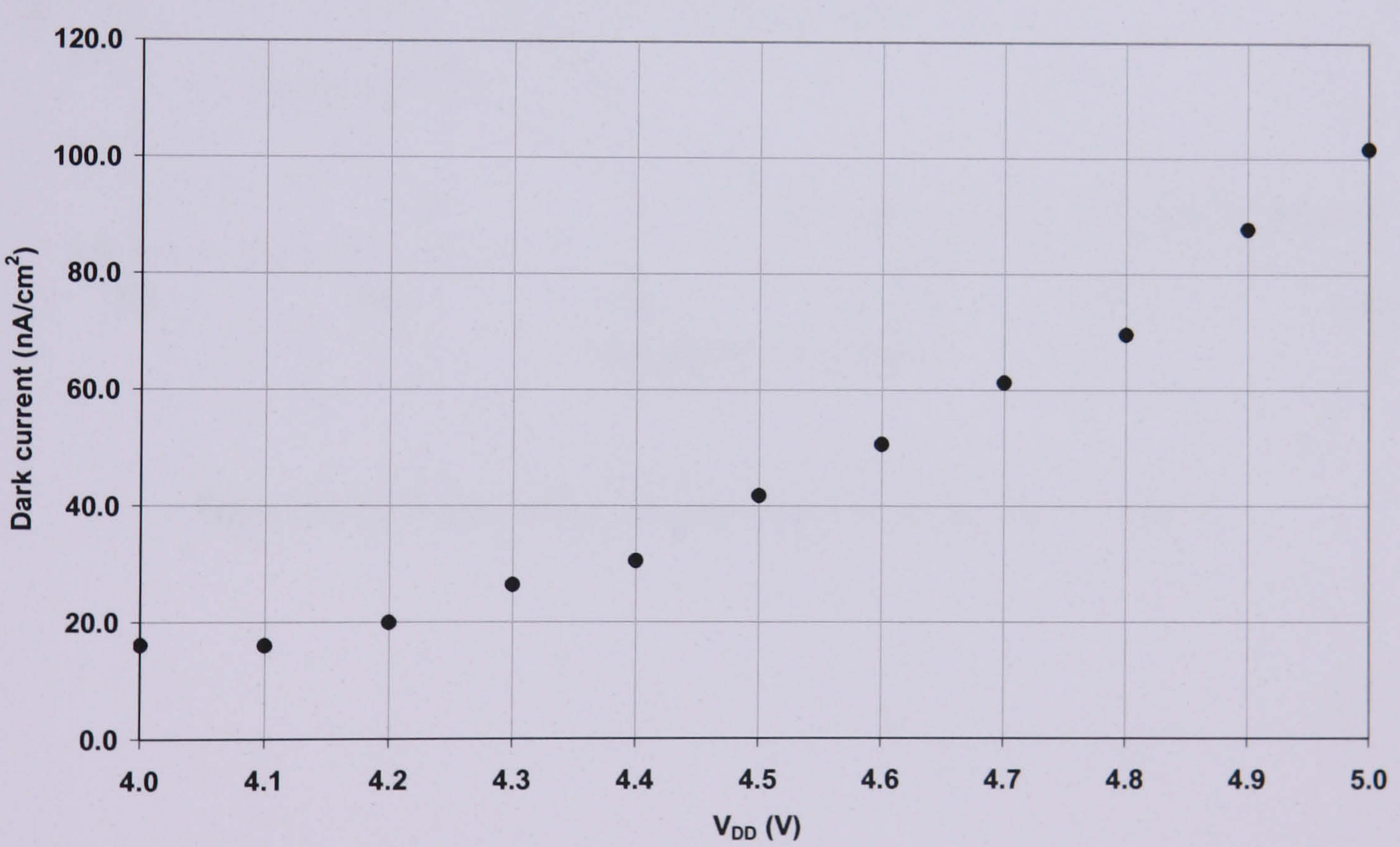


Figure 7.16 Dark signal variation with supply voltage V_{DD}, for a fixed V_{out} = 2.5 V

The reset voltage, V_{RD}, affects the initial bias conditions of the pixel and so will also affect the rate of discharge of the diode due to leakage current. If the reset level is higher, the initial drain-source voltage of the follower transistor will be lower, and

therefore the effect would be initially less severe. Dark signal traces were acquired for a range of V_{RD} values with a fixed V_{DD} of 5V. The traces are shown in **Figure 7.17**. A linear fit applied to the early part of the trace shows that as the reset drain voltage is increased the initial rate of discharge reduces as expected. The rate of discharge was also calculated for the same output voltage for each reset voltage as shown in **Figure 7.18**. One can see that the dark signal for a given output voltage is independent of V_{RD}, but it does determine the initial V_{DS}, therefore the effect can be reduced if the full signal range of the chip is not needed.

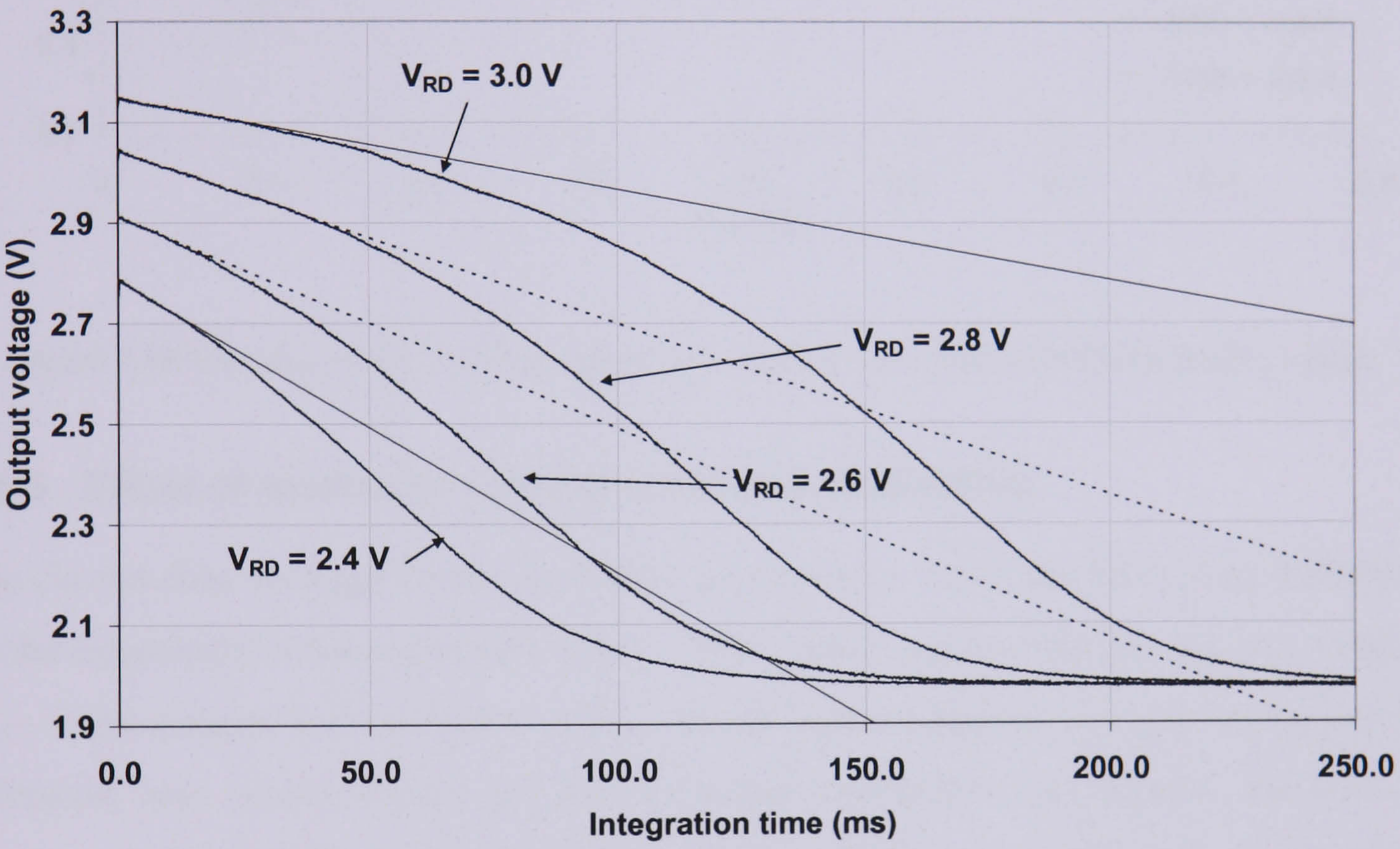


Figure 7.17 The effect of V_{RD} on dark signal for a range of reset voltages

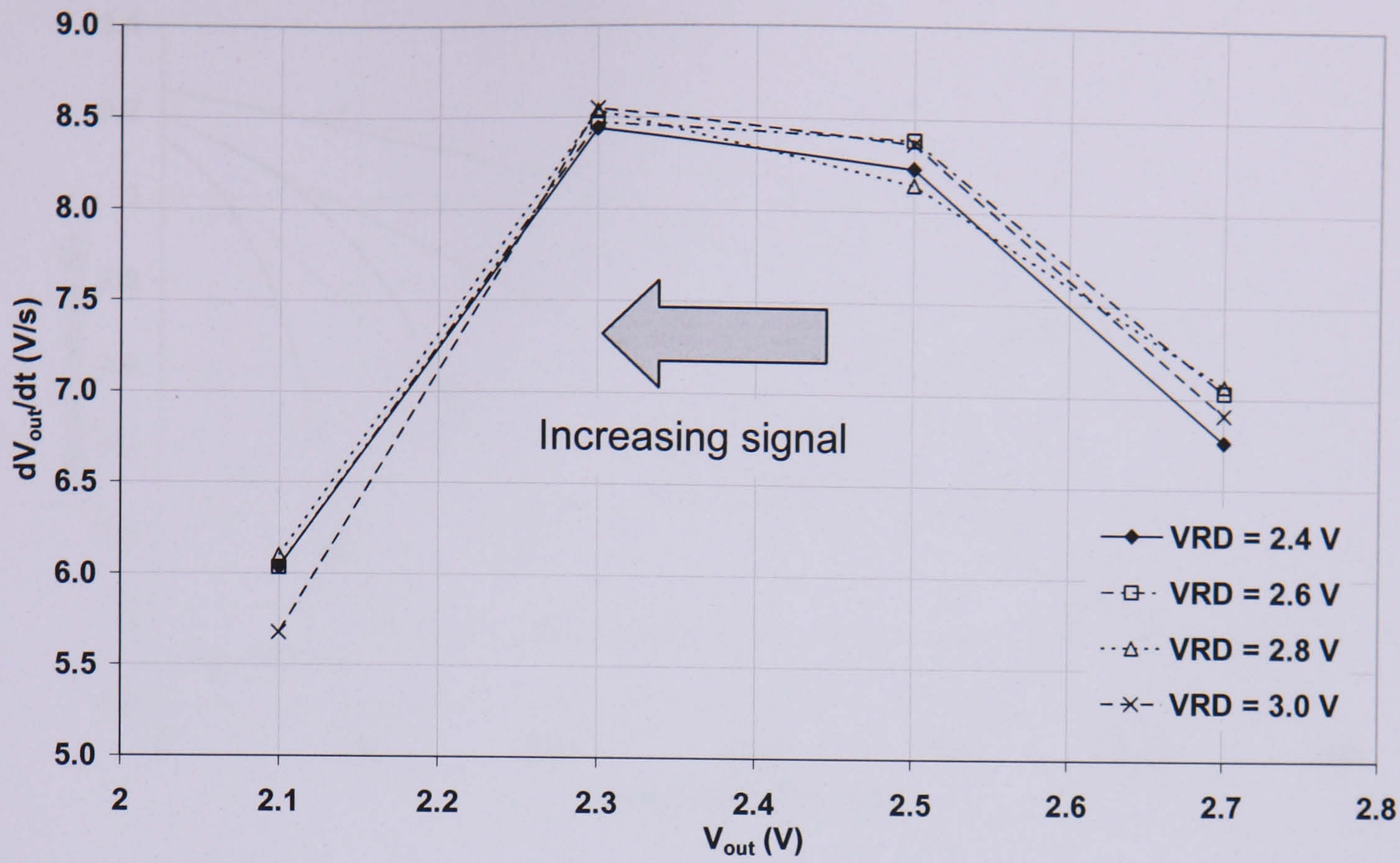


Figure 7.18 The effect of V_{RD} on dark signal for a range of V_{RD} values with a fixed output voltage

7.5.3. Effect of photosite current in follower transistor

The current flow through the in-pixel follower transistor could also have some influence on the magnitude of the hot carrier effect. This current is set by the gate-source voltage, V_{LG}, of the column load transistor. If the rate of electrons passing through the channel is increased, one would expect the rate of impact ionisation and photon emission to increase proportionally. Therefore, one would expect the overall dark signal to be linearly dependent on the load current and correct biasing of the column transistor could potentially minimise the effect.

Adjusting the current and observing the rate of discharge for the diode under dark conditions investigated the effect. The column load transistors in all the test devices have a W/L = 5/30. The current they supply can be set in the range 0 to 100 μA by adjusting the gate bias between 1 and 5V. Below 1V the transistor operates in the sub-threshold region and minimal current flows. The effect on the dark signal rate for a range of load gate voltages is shown in **Figure 7.19**.

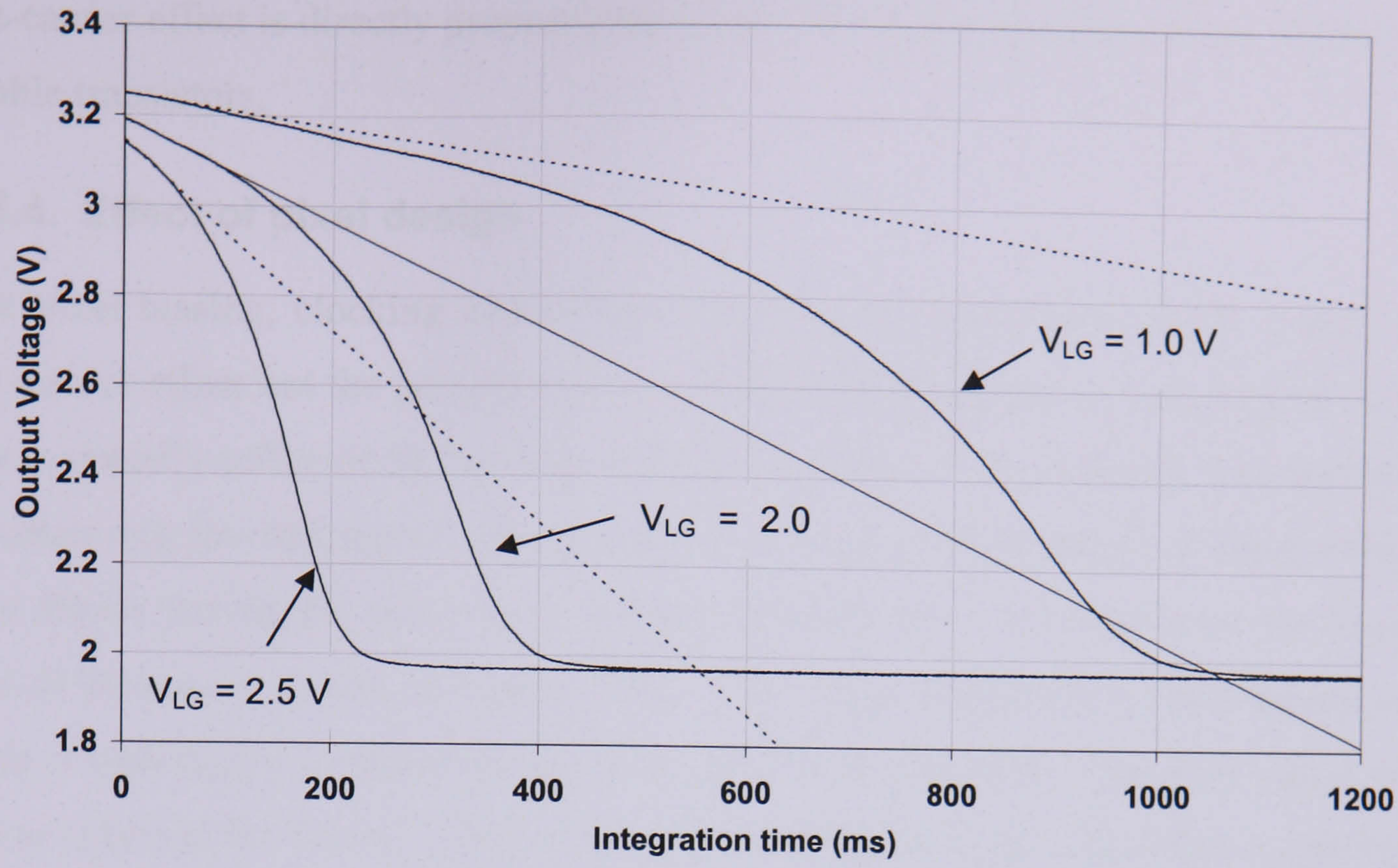


Figure 7.19 The effect of photo-site current on dark signal

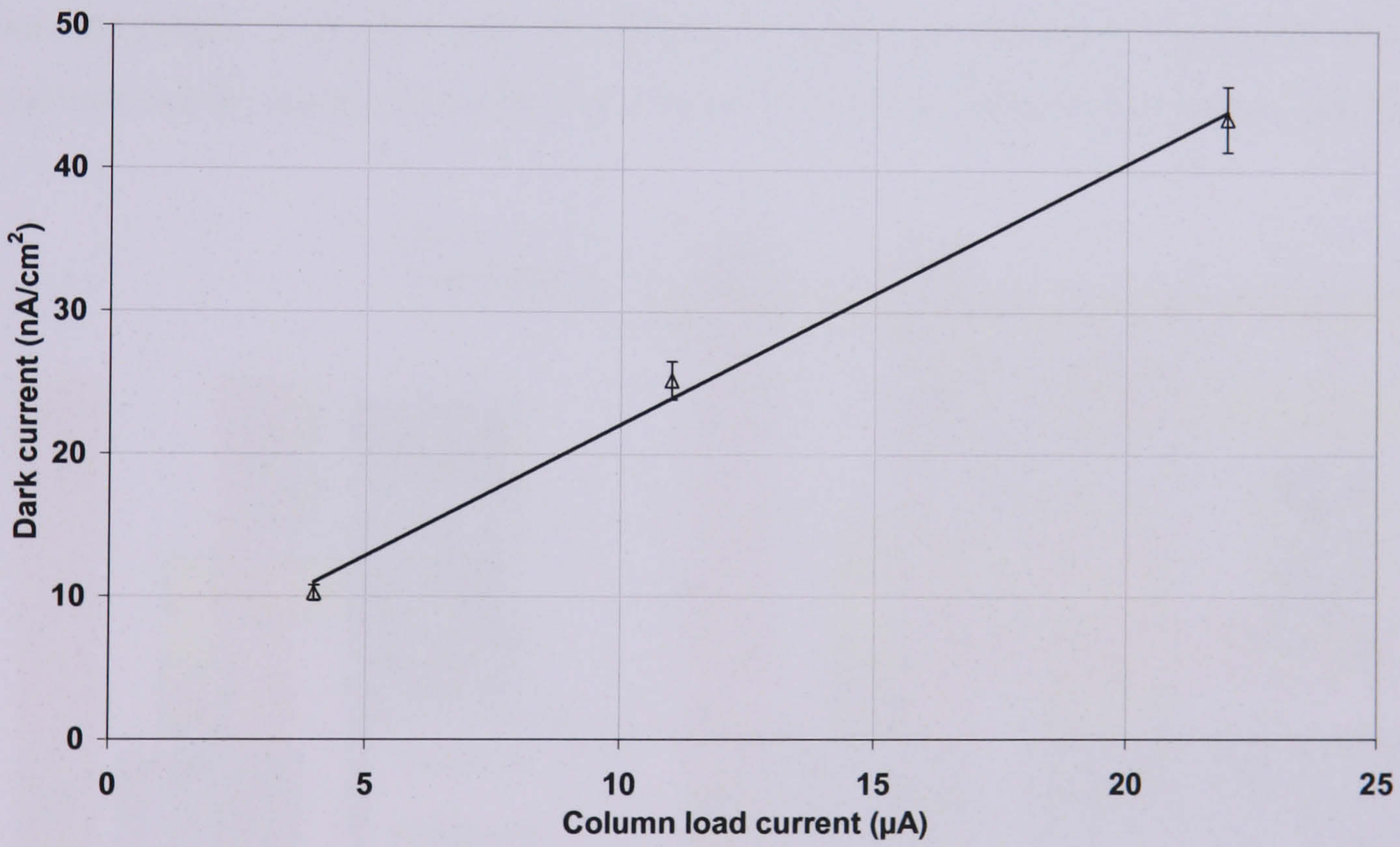


Figure 7.20 The effect of photo-site current on dark signal for a constant output voltage of 2.5 V. The error bars are derived from the uncertainty in the fit to the output voltage waveform and the responsivity

The waveforms in **Figure 7.19** were then fitted at $V_{out} = 2.5V$ for each waveform. The instantaneous leakage rate for each V_{LG} was plotted as a function of corresponding column load current and is shown in **Figure 7.20**. The gain and V_{GS} of the follower circuit is affected by biasing of V_{LG} (as seen in Chapter 4) but it can be seen that the

hot-carrier effect is directly proportional to the current flowing through the follower and enable transistors.

7.5.4. Effect of pixel design

The pixel biasing, clocking and design determine the magnitude of the source of the hot-carrier effect but the pixel design also affects the proportion of the parasitic current that is actually collected by the sense node. The effect of pixel design was investigated by observing the dark signal rates in another of the pixel structures contained within the Test Pixels having the same diode but a p-channel reset. A close-up of the layout of two of devices is shown in **Figure 7.21**. The major difference is the presence of the extra n-well region required for the p-channel reset transistor. The dark signal output traces obtained for the two designs are shown in **Figure 7.22**. The effect is observed to be considerably lower in the p-channel reset pixel. The dark signal as a function of output voltage for both devices is plotted in **Figure 7.23**. The ratio between the dark signals of the n- and p-channel reset is ~ 2.5 and is independent of the output voltage across the range. It is clear that the additional n-type well strongly suppresses the dark signal rate and is likely to be acting as a drain for some of the extra minority carriers.

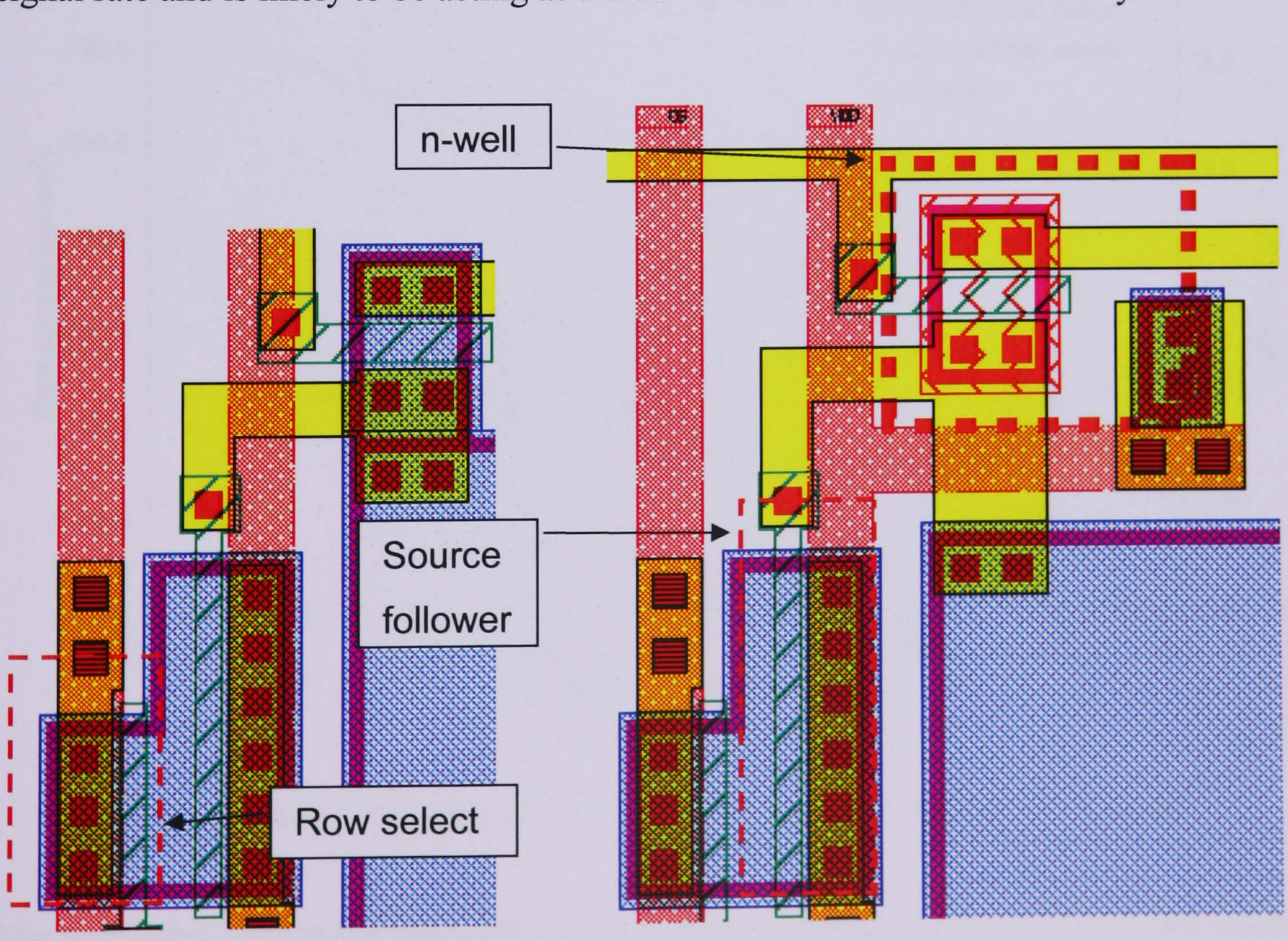


Figure 7.21 CAD layout showing close-up of the readout circuitry for the n-channel (left) and p-channel (right) reset pixels

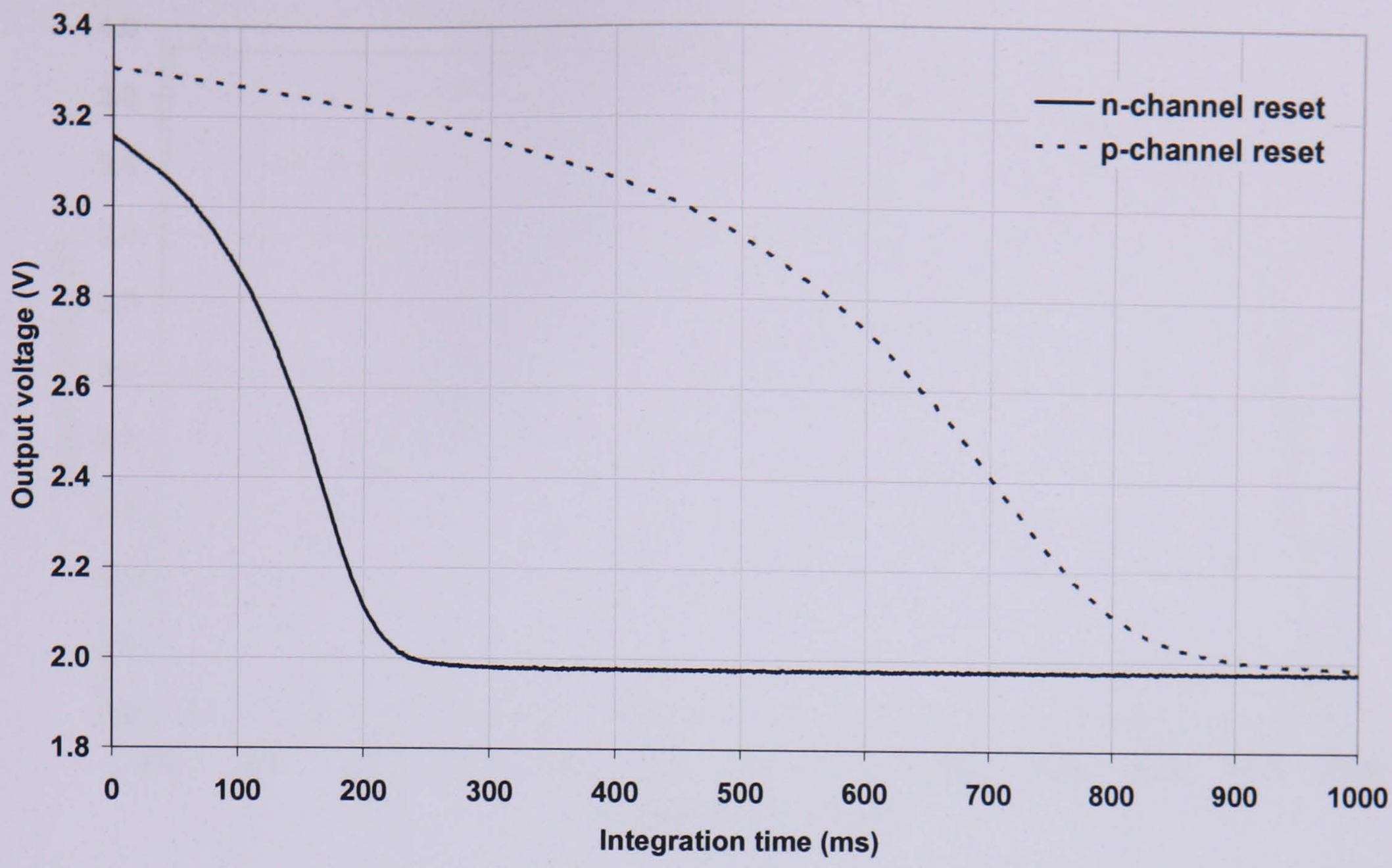


Figure 7.22 The effect of reset transistor polarity on hot carrier induced dark signal

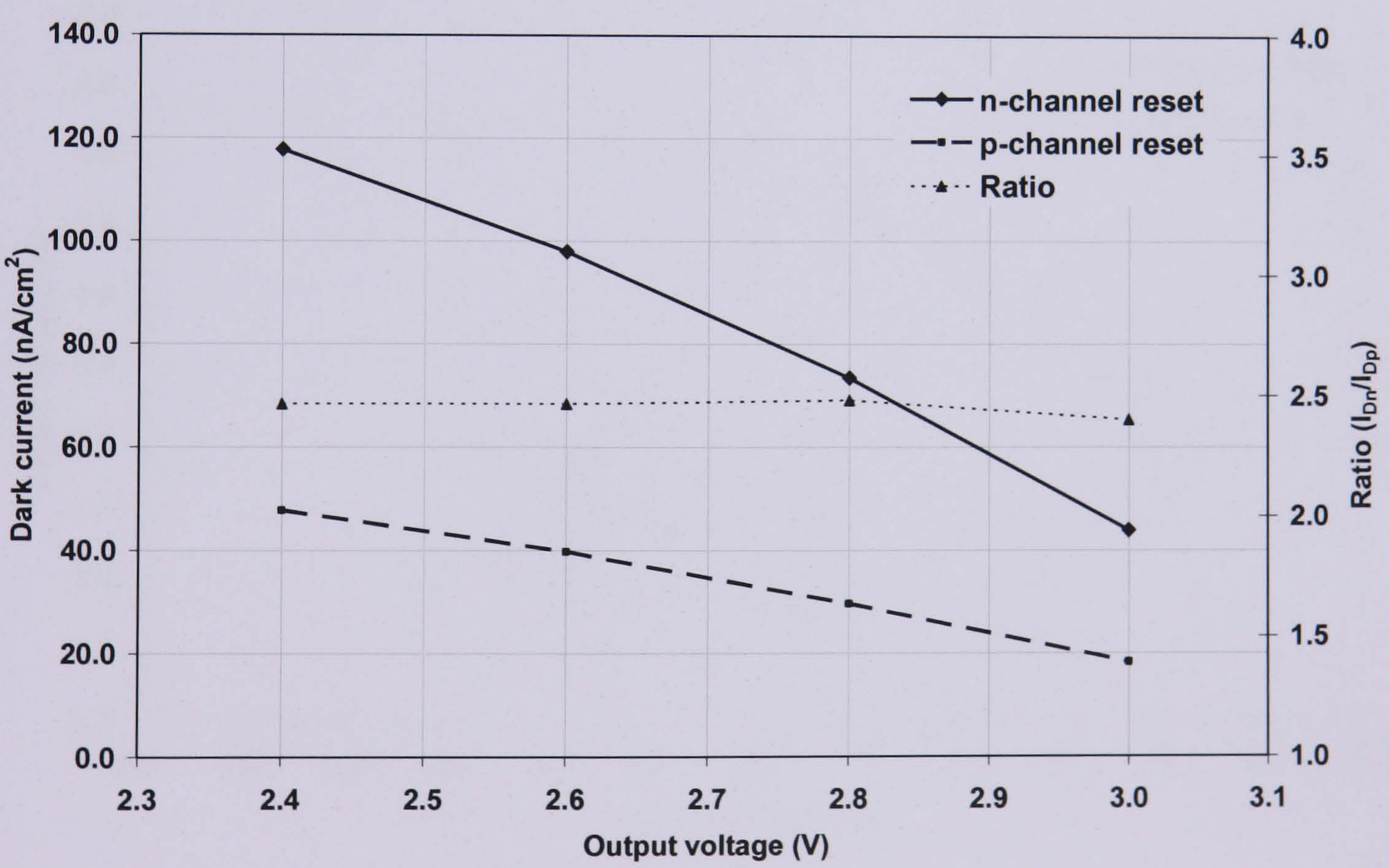


Figure 7.23 The effect of reset transistor polarity on hot carrier induced dark signal

The p-channel reset pixel was also useful to further investigate the effect of the electric field in the follower. This type of pixel allows reset to a higher V_{RD} as shown in **Figure 7.24**, which enables a higher range of V_{DS} values to be investigated.

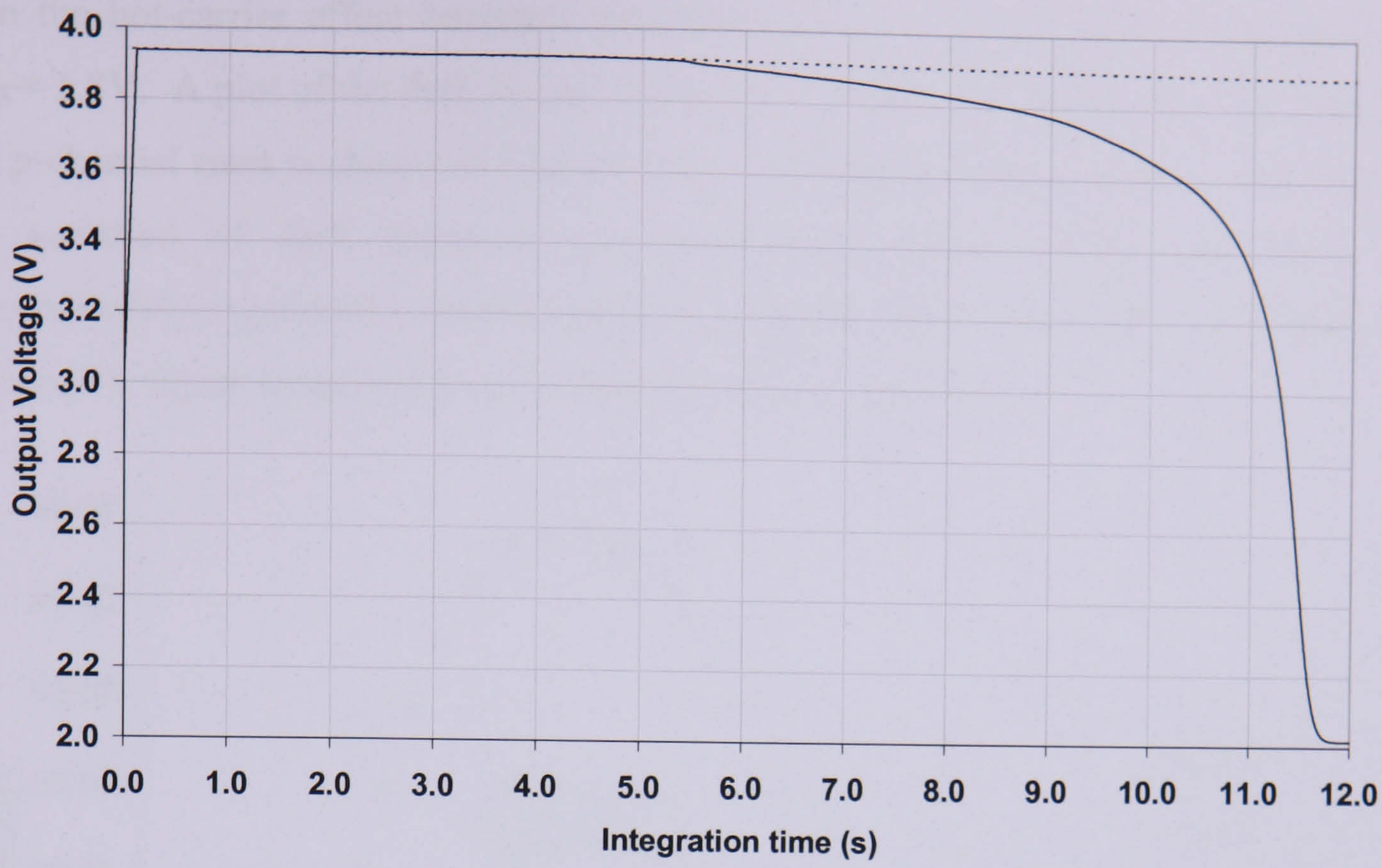


Figure 7.24 p-channel reset pixel output voltage waveform with V_{RD} = 5 V

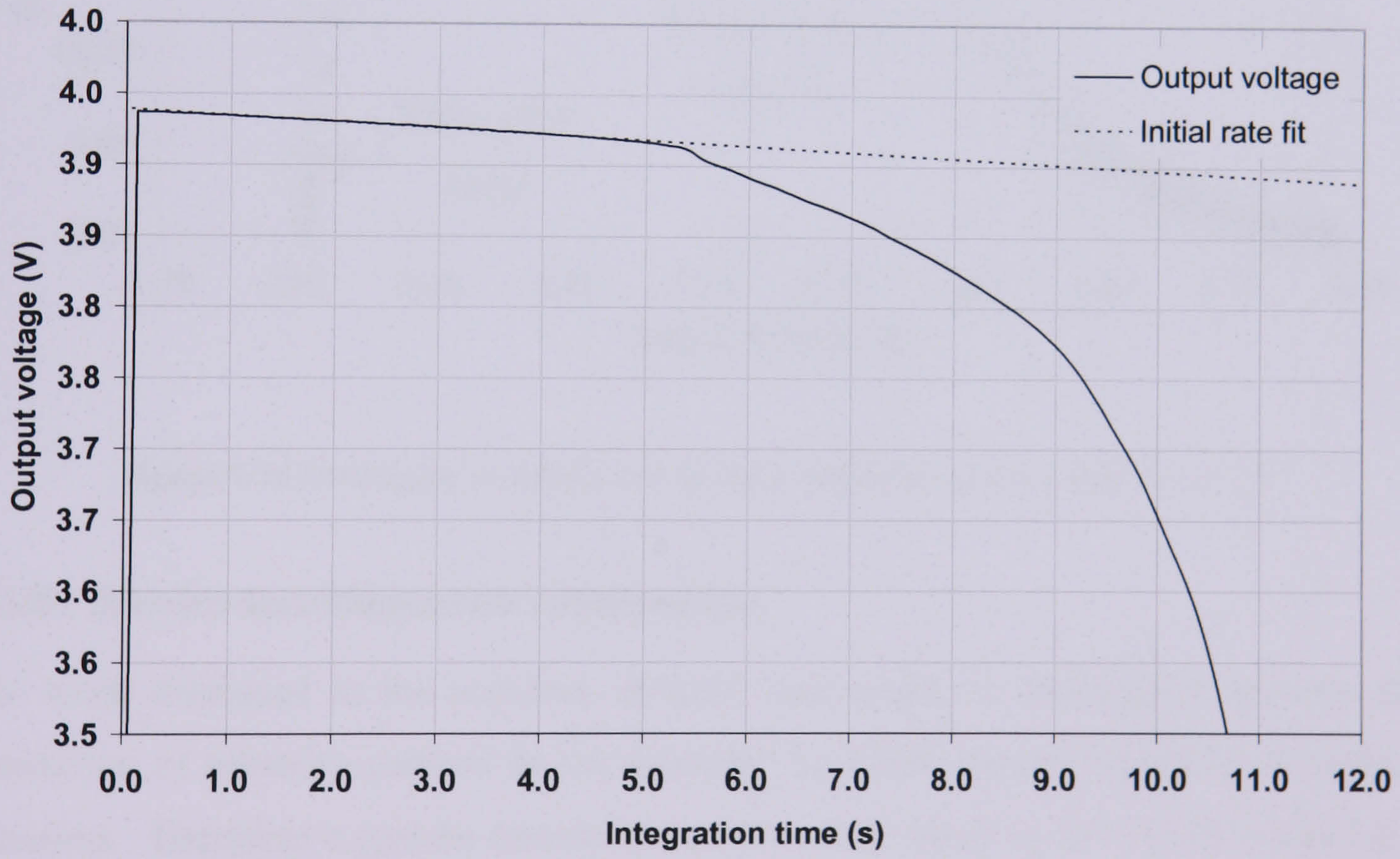


Figure 7.25 p-channel reset pixel output voltage waveform with V_{RD} = 5 V (zoomed)

Figure 7.25 shows a zoomed version of the output waveform shown previously in **Figure 7.24** and provides some additional information on the behaviour of the hot-carrier effect. The data shows a very low initial dark signal of 1 mV/s (13pA/cm^2) but

then the hot-carrier effect becomes activated at V_{out} = 3.95V, which corresponds to V_{DS} = 1.8V. A plot of the dark signal variation over the wider output range provided by the p-channel reset is shown in **Figure 7.26**. The higher range highlights the fact that the variation of dark signal is non-linear with output voltage and shows an approximately exponential dependence on the electric field. This was not obvious with the smaller signal range of the n-channel reset shown previously.

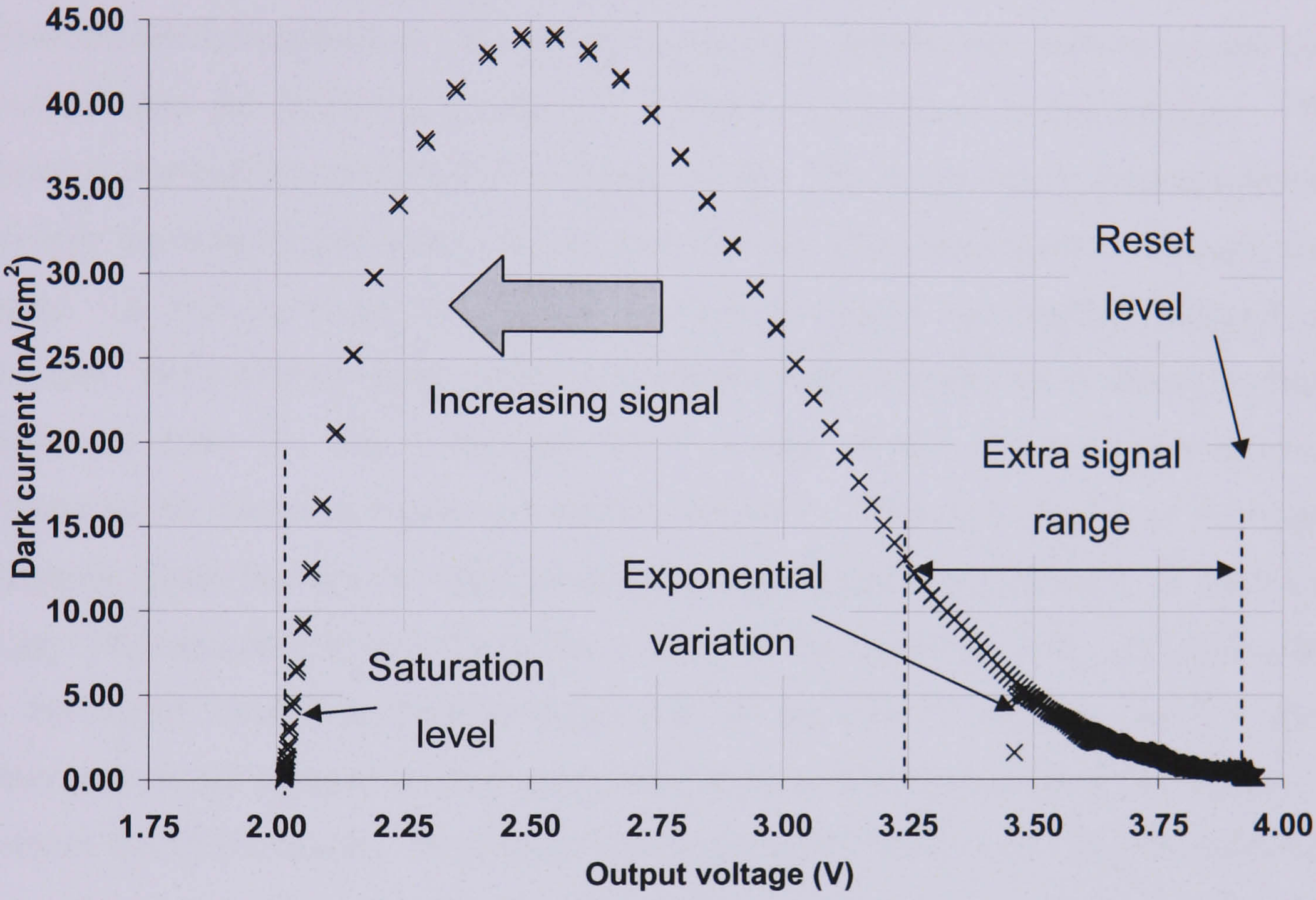
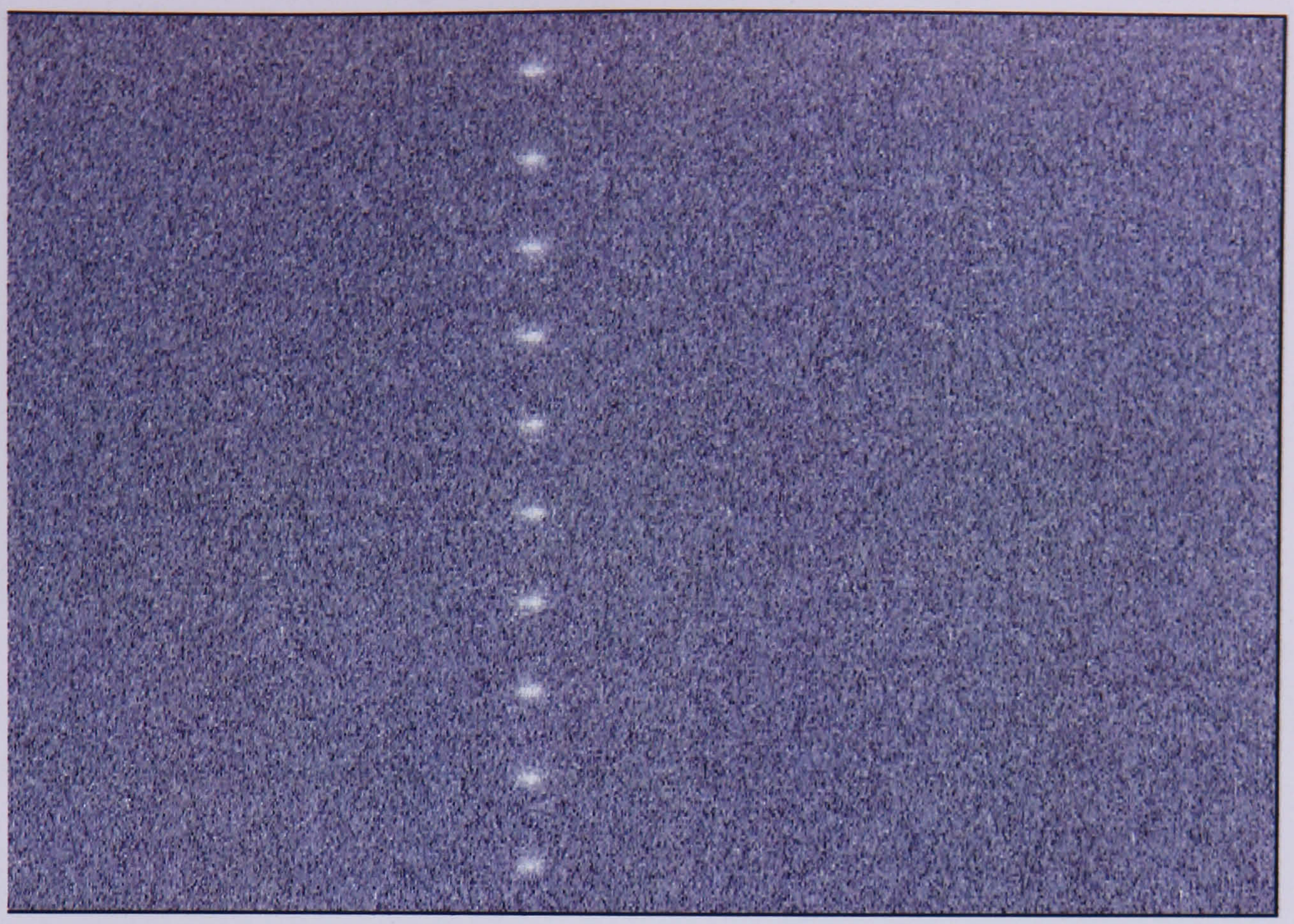


Figure 7.26 Dark signal vs. output voltage for p-channel reset pixel with V_{RD} = 5 V

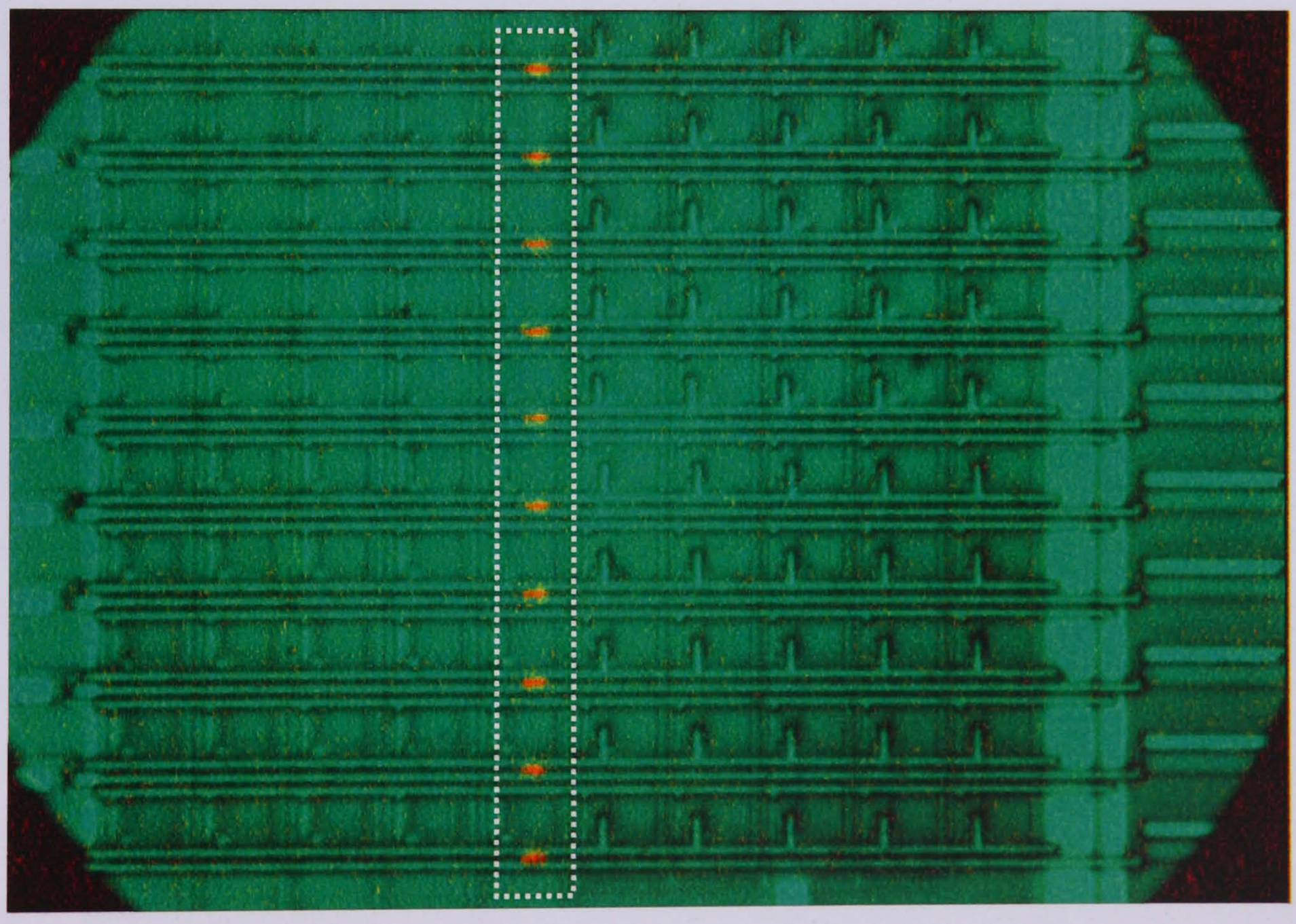
7.5.5. Electro-luminescence observation

The work discussed in the previous sections was unable to distinguish between the generation of minority carriers in the substrate by either impact ionisation or photon emission. Therefore a custom camera system was developed to observe this effect and determine its location. The system consisted of an e2v technologies L3C95 series low light level CCD camera (e2v technologies, 2004) attached to a microscope. The CCD camera uses an extra electron multiplication gain register to amplify the signal generated by the detector and thereby achieve very high sensitivity. The Test Pixels were placed on a special jig (containing the APS drive electronics) to enable precise positioning of the device within the microscope field of view. An image was first taken

under light conditions to align the device correctly and establish the location of pixel structures. The CCD camera was then set up to take low light level images. Temporal and spatial averaging functions built into the camera were also used to improve the image clarity. The Test Pixels device was initialized with a regular reset pulse and a row was permanently selected during image acquisition. The dark image is shown in **Figure 7.27a**. Note that the orientation of the device in the microscope was such that the rows run vertically down the image. Ten distinct glowing regions can be observed above the background noise. Using image-processing software the dark image was then overlaid onto the illuminated image to ascertain the location of the emission. The resultant overlaid image is shown in **Figure 7.27b**. The image clearly demonstrates the ten light emitting regions to be aligned with the row of selected pixels. A single pixel region was then expanded and the schematic of the pixels was precisely aligned and overlaid. The resulting image is shown in **Figure 7.28**. The photon emission is clearly emanating from the region between the V_{DD} and column output interconnections containing the source follower and enable transistors. The drain region of the enable transistor shares the same n+ implant as the source region of the follower. It is difficult to say if the emission is from the follower or the enable transistor. The polysilicon gates in the region should be largely transparent to the photon emission but the metal interconnects are opaque so they may mask some of the vertical photon emission up towards the CCD camera. In addition to measuring the variation in light intensity with V_{DD}, the load current was varied using the load gate voltage. The intensity was observed to increase with increasing load current (load gate voltage). This is expected as the increased current flowing through the pixel implies a greater amount of hot electrons present to emit photons. The variation with reset drain voltage was briefly investigated but the intensity variations were not noticeably visible.



a)



b)

Figure 7.27 Microscope image of the Test Pixels under a) dark conditions and b) externally illuminated with dark image overlaid. Note that the orientation of the device was such that the rows appear to run vertically in the image

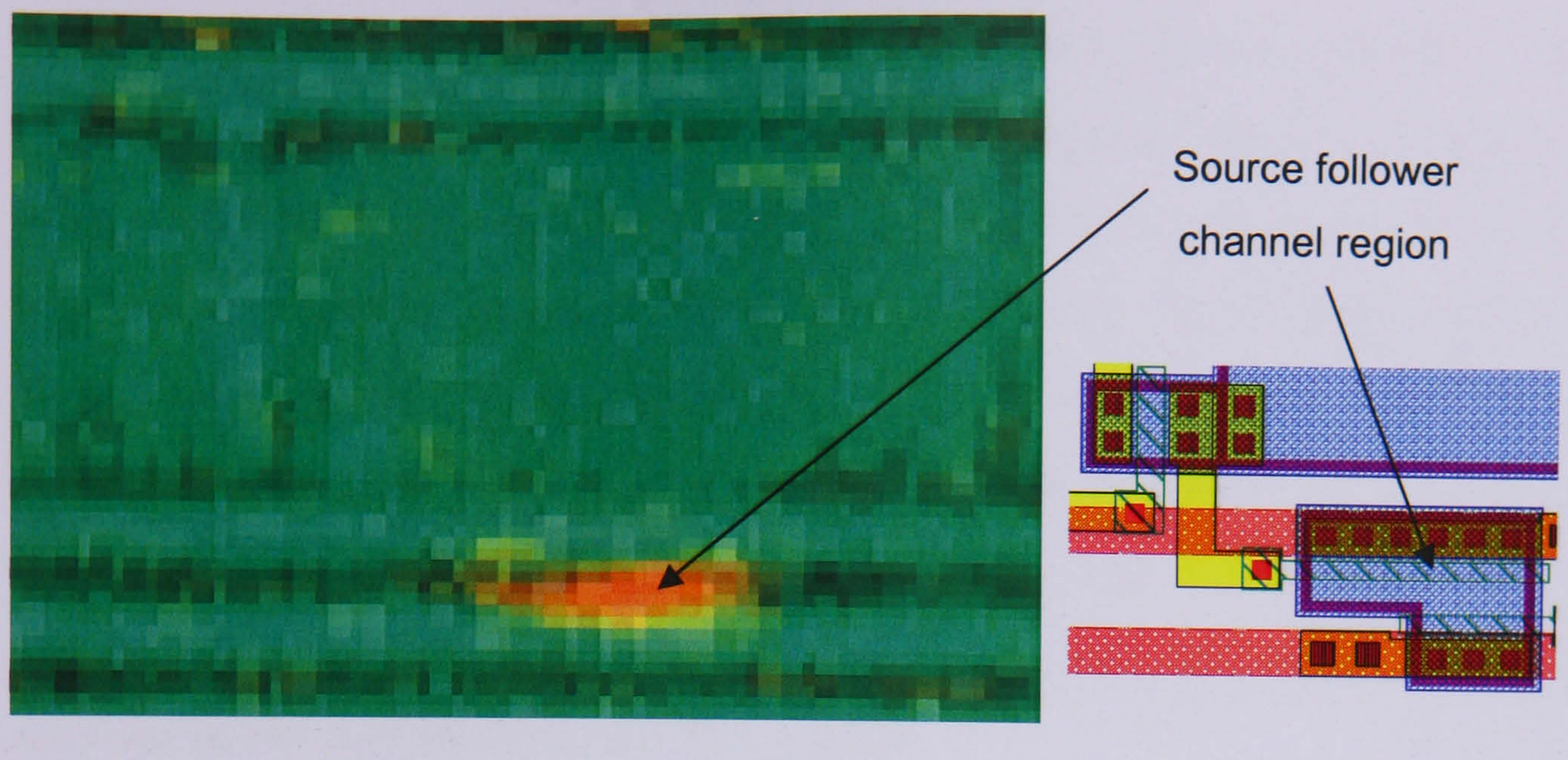


Figure 7.28 Expanded microscope image (left) and equivalent scale CAD layout (right) showing the location of the photon emission from within the source follower channel region

7.5.6. Discussion

This research has demonstrated that there is a significant extra source of dark signal present during read-out of the 3T pixel. For the TS50 process the effect is three orders of magnitude larger than the contribution due to leakage current and is dominant during the read-out phase. The effect appears to be logarithmically dependent on the electric field and linearly dependent on the supply current. However the relationship between output voltage, V_{DS} and electric field needs to be investigated further through circuit and device simulation. The effect may also be 'process dependent' although similar observations in other processes have been reported in the literature, as noted earlier. The magnitude of the effect is dependent on the instantaneous bias conditions of the source follower transistor and the pixel design. During device operation there is an important cross-over time period, whereby the hot-carrier effect arising from the row select pulse is dominant over the leakage effect during the integration period. The hot-carrier effect should get worse as the temperature of the silicon is reduced because the carrier mobility increases. Therefore at low temperatures the effect may dominate over the thermally generated leakage current. Total dark signal from a long integration may be less than from the hot carrier effect during a short readout period. This may explain the behaviour of the dark signal at low temperatures seen previously in the Imaging Arrays.

The observations made with the low light level camera clearly demonstrated photon emission and confirmed the location of the emission to be in the vicinity of the source follower and row select transistors. It is not possible however to estimate the proportion

of dark signal due to impact ionisation and that due to photon emission. The spectrum of photon emission is predominantly infrared in nature therefore it is not possible to fully characterise the spectrum of the emission using the silicon based CCD camera as this has no response for wavelengths above 1100 nm. Future measurements would be best made with camera using an InGaAs or HgCdTe sensor and spectrometer, as these have sensitivity in the IR wavelength range. However the fact that the CCD is sensitive to similar same wavelengths as the APS implies that if the CCD camera does not observe the effect it may not affect the APS either and the longer wavelength photons may not in fact contribute to the dark signal.

The hot-carrier effect has major implications for APS device designs, for example those employing repeated "non-destructive read-out" or intelligent pixels with significant in-pixel logic. Indeed a high dark signal has been observed in devices containing an in-pixel ADC in the past (Kleinfelder et al., 2001). The problem may potentially worsen as image sensor manufacturers continue to use smaller, high-density sub-micron manufacturing processes, a trend driven by optimisation of high speed logic circuits. The smaller, more advanced devices are more susceptible to the effect because of the higher electric fields (Wong, 1996). Suggestions have been made to use p-MOS readout and n-MOS reset circuits because the hot-carrier effect is reduced in p-channel MOS transistors due to the lower mobility (Takayanagi et al., 2003). It is also important to note that when trying to measure the leakage current contribution with Test Pixels one should not operate the follower transistor for longer than necessary otherwise a significant component of the dark current will be due to the hot-carrier effect and results will not be representative of array performance. If multiple samples are required the effect will significantly interfere with the collected photo signal.

7.6. Summary

This chapter has described in detail the contributions to dark signal in the new Test Structures produced using the TS50 process. The dark signal of the Imaging Arrays was studied first and the two different diode structures were found to exhibit similar performance with the magnitude lying between that of an inverted mode and normal mode operation CCD. The variation with temperature was also studied and whereas the variation was found to behave normally at higher temperatures, at lower temperatures the value saturated. A possible reason for the lower temperature saturation was attributed to the hot-carrier effects during the image read-out period. This conclusion was made after the dark signal in the Test Pixels was studied and the devices were found to have a dark signal three orders of magnitude higher than the Imaging Arrays. Further investigation concluded that the increased dark signal was due to operation of the source follower and row select transistors during read-out. The effect was found to be exponentially dependent on the electric field within the follower transistor and linearly dependent on the current supplied to the pixel, thereby pointing to a hot carrier effect. The location of the hot-carrier effect was verified by observing the associated electro-luminescence using a low light level camera system and was confirmed to be from the region containing the row select and source follower transistors. The study therefore concluded that the main source of dark signal during integration was due to leakage currents but during read-out the dark signal was dominated by the hot-carrier effect. The effect has implications for the production of intelligent pixels containing many active transistors and repeated "non-destructive read-out" as the readout clearly alters the measured signal. The next and final experimental chapter describes an investigation into the photo-response and other electro-optical characteristics of the new devices.

Chapter 8: Electro-optical characterisation

Chapter 8 describes an investigation into the electro-optical characteristics of the new Test Structures. The first section outlines the theoretical aspects of quantum efficiency (QE) and cross-talk. An experimental setup developed by the author to measure QE is then described, including the results for the Test Structures. The chapter closes with a comparison of the results obtained, along with analysis of cross-talk measurements performed by engineers at e2v technologies.

8.1. Introduction

The previous experimental chapters have focussed on the electrical characteristics of a CMOS pixel, such as dark signal and noise. This final chapter looks at the electro-optical characteristics of a sensor and, more specifically, the interaction of photons with the sensor and how they are detected by the photodiode structure. The most fundamental of the electro-optical characteristic is quantum efficiency. Ideally, for a given application, the collection efficiency should be high across the wavelength range of interest otherwise a large proportion of the light incident on the sensor will be wasted. The other fundamental parameter is referred to as pixel to pixel cross-talk. Cross-talk should be minimised such that generated charge is collected within the correct pixel, otherwise the spatial resolution of the sensor will be degraded.

8.2. Theoretical background

Overall electro-optical performance is determined by the sensor's ability to:

- Intercept an incoming photon
- Convert the incident photon to an electron-hole pair
- Capture the photo-generated charge within the depletion region of the pixel

The combination of these three processes determines the parameters of QE and cross-talk. A more detailed description of these processes is given in the following sub-sections.

8.2.1. Photon interception

The proportion of photons entering the bulk silicon and reaching the photodiode for detection is dependent on a number of effects. We have seen in previous chapters that

the surface of a CMOS pixel can be complex in nature and this causes a range of effects that influence the QE and optical cross-talk of a device. **Figure 8.1** illustrates the phenomena that can occur when a photon is incident on a pixel.

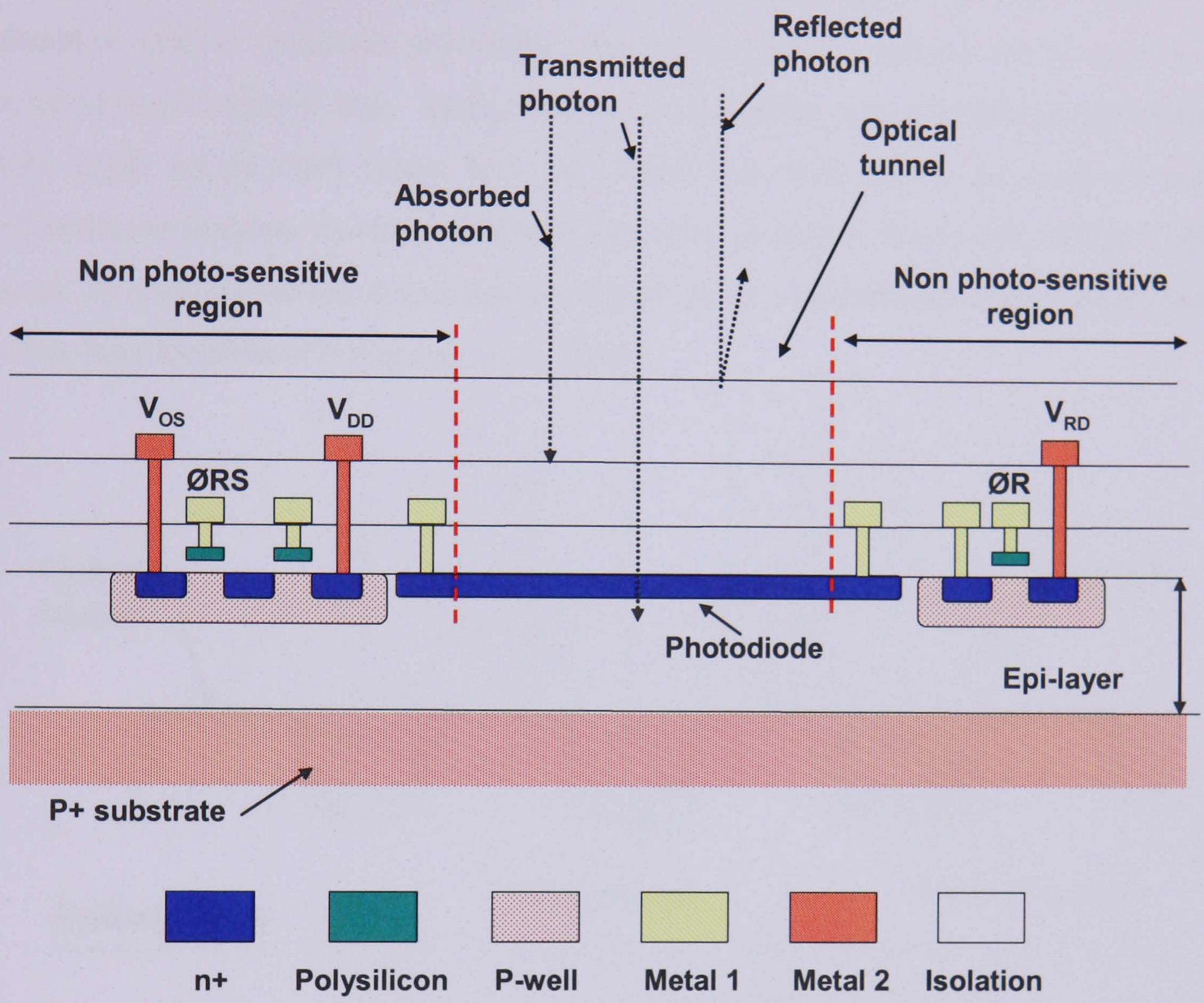


Figure 8.1 Cross section of a CMOS pixel showing the various processes affecting QE

One can see from **Figure 8.1** that the structure creates an 'optical tunnel' through which a photon must pass before interacting with the photodiode structure (Catrysse et al., 2000). Initially an incident photon may be reflected or absorbed by one of the overlying layers such as the metal interconnects or isolation. Absorption by the SiO_2 layers is a particular problem at lower UV wavelengths (< 400 nm). The presence of the thin layers over the pixel can also lead to a range of interference effects including fringing in the optical response of a device over the spectrum. It may also be the case that photons incident from a slight angle may be absorbed or reflected by the walls of the optical tunnel. The effect of the absorption and reflection losses mean less than 100 % of the incident light is able to enter the photosensitive epitaxial layer. The ratio of photosensitive area to pixel area is known as the fill factor, described earlier.

Some of the above problems can be minimised with the use of a microlens (Agranov et al., 2003) as illustrated in **Figure 8.2**. A miniature lens is placed over the surface of each pixel to focus stray light towards the photosensitive area. However the use of such structures requires extra processing steps and if not accurately aligned can introduce optical cross-talk problems, whereby a photon intended for given pixel is diverted to an adjacent one. Such structures are popular in mobile phone type sensors with small pixels (and hence low fill factor) but tend not to be used in higher performance sensors. Another approach has been to reduce the height of the 'optical stack' by using fewer metal interconnect layers, or by using thinner copper metal layers rather than aluminium (Gambino et al., 2006).

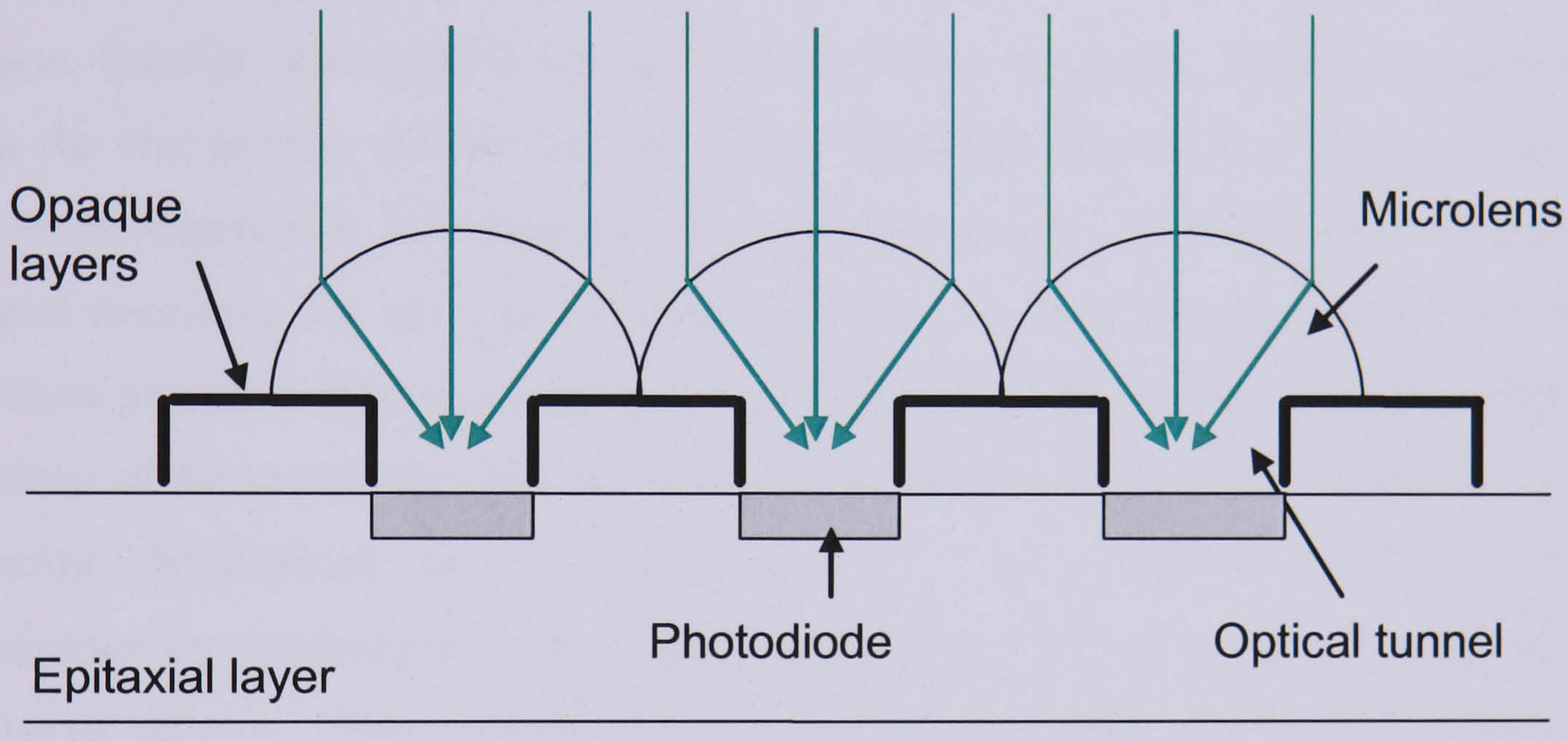


Figure 8.2 The micro-lens principle

The best solution to the fill factor problem for a scientific type device is to illuminate the sensor from the reverse side. This requires that the substrate layer be removed leaving the thin epitaxial layer and is known as back-thinning or backside illumination. The approach was originally employed for scientific CCDs (Shortes et al., 1974) and is now a well-established part of the manufacturing process at companies such as e2v technologies. High performance CMOS sensors will also require thinning, however the process is complex and expensive and is only beginning to be explored for scientific devices (Waltham et al,. 2007).

8.2.2. Photon capture and conversion

If an incident photon with energy greater than the 1.1 eV penetrates the bulk silicon, it will be absorbed and an electron-hole pair will be generated. The absorption depth is

dependent on the photon wavelength (as seen in Chapter 3), with the depth being smaller for blue light, moderate for green light and deep for red light. Infra-red photons with energy less than 1.1 eV will pass directly through the silicon.

8.2.3. Charge capture

If an electron-hole pair is generated in the silicon, then successful collection is dependent on the generation location. If the charge is generated within a photodiode depletion region, the pair will be swept apart by the electric field and the electron is collected by the photodiode. If the charge is generated outside the depletion region it must diffuse towards the depletion region for collection. The charge may diffuse towards the depletion region but may also recombine with a hole before reaching the region, therefore the signal is lost and the QE will be degraded. A further possibility is that the charge may diffuse laterally to the depletion region of an adjacent pixel as shown in **Figure 8.3**. This process is known as electrical cross-talk and will degrade the spatial resolution for any 2-D imaging application because the signal generated by an incident photon will be detected by the wrong pixel. The problem will also affect the contrast of the sensor including performance parameters such as the modulation transfer function (Shcherback and Yadid-Pecht, 2001). The cross-talk problem can be minimised by designing the sensor such that the depletion region extends deep into the epitaxial silicon. This requires the use of high resistivity silicon and higher bias voltages, which has only recently been explored for CMOS sensors (Janesick et al., 2007).

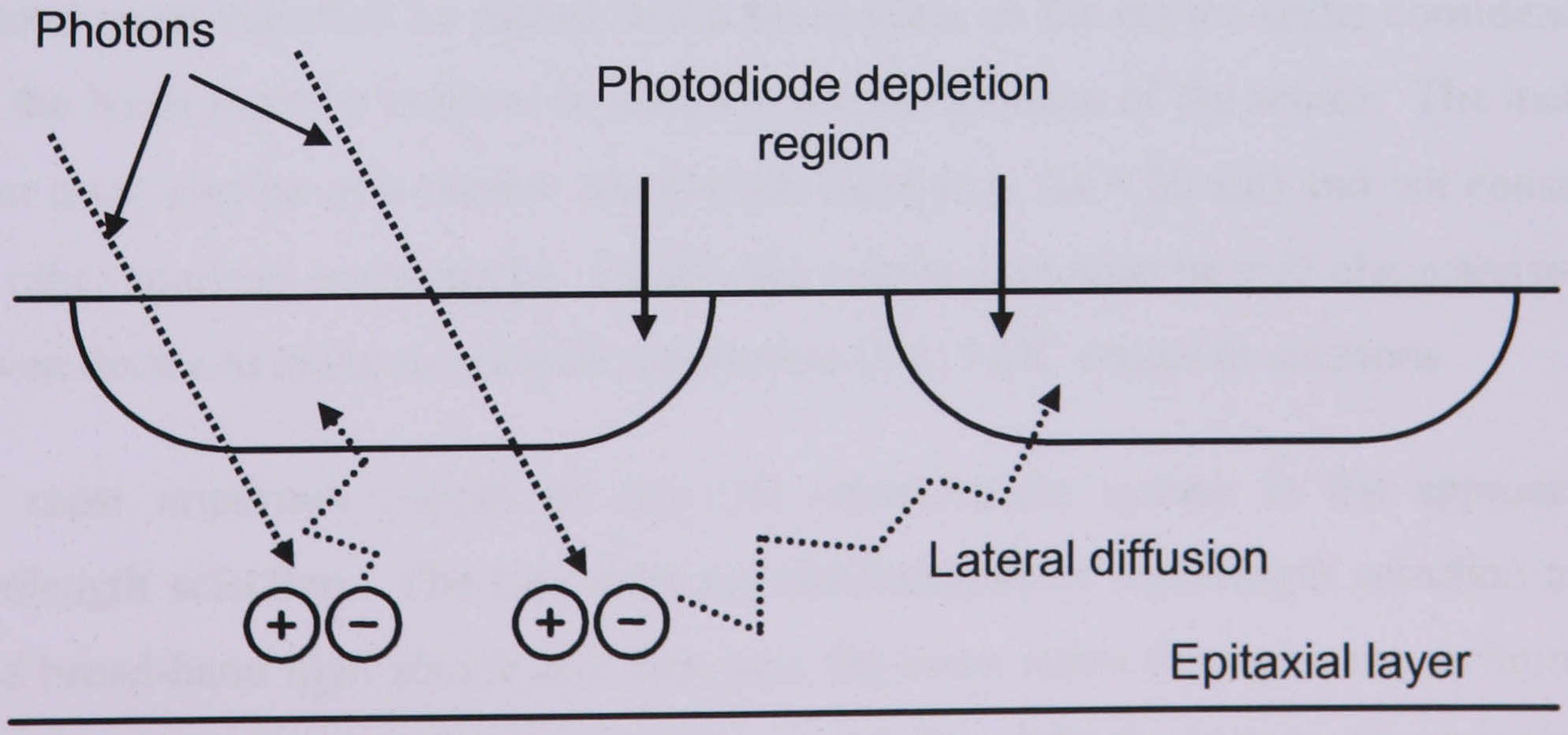


Figure 8.3 Electrical cross-talk due to lateral diffusion of photo-generated charge

8.3. Quantum efficiency characterisation

This section describes the development of an experimental set-up to characterise the QE of the Test Structures.

8.3.1. Experimental method

To calculate QE one must be able to accurately measure the number of photons of a given wavelength incident on a device and the corresponding number of electrons collected in a given time period. It is not possible to directly measure these values; therefore they must be derived from more easily measurable quantities. The basic technique is to illuminate the APS at a given wavelength, λ, and measure the signal S_{out} (ADC counts) collected in a known time period, t_{int}. The total number of electrons generated can then be calculated using the system gain G_S. The number of photons incident on the sensor is then determined by replacing the APS with a calibrated photodiode and measuring the power, P_λ (W/cm^2), of the incident beam. The percentage QE is then given by:

$$\eta = \frac{S_{out} hc}{G_s t_{int} P_\lambda A_P \lambda} \times 100\% \qquad (8.1)$$

where h is Planck's constant, c is the speed of light and A_p is the pixel area (cm^2). Equation 8.1 highlights a number of possible sources of error when making the QE measurement. It is vital that the nature of the light beam used to illuminate the device is identical to the beam used to illuminate the calibrated photodiode. The calibrated detector must therefore be placed in the same plane as the device under consideration, and the beam must be uniform in intensity across the plane of the sensor. The incident beam must also be of a narrow wavelength band (e.g. $\Delta\lambda < 20$ nm) and not consist of any other spurious wavelengths. Finally the system gain must be well characterised for a given device to make an accurate conversion from ADC counts to electrons.

The most important feature of any QE measurement system is the approach to wavelength selection. The two most popular methods of wavelength selection are to use a broad-band light source and then pass the beam either through a monochromator or a narrow band-pass filter. In the case of the author's system, the wavelength selection was done using high quality narrow band-pass filters. However this limited the

number of wavelengths selectable across the range. The use of a monochromator would have allowed a continuous scan across the range, but it would have been more costly and complex to implement.

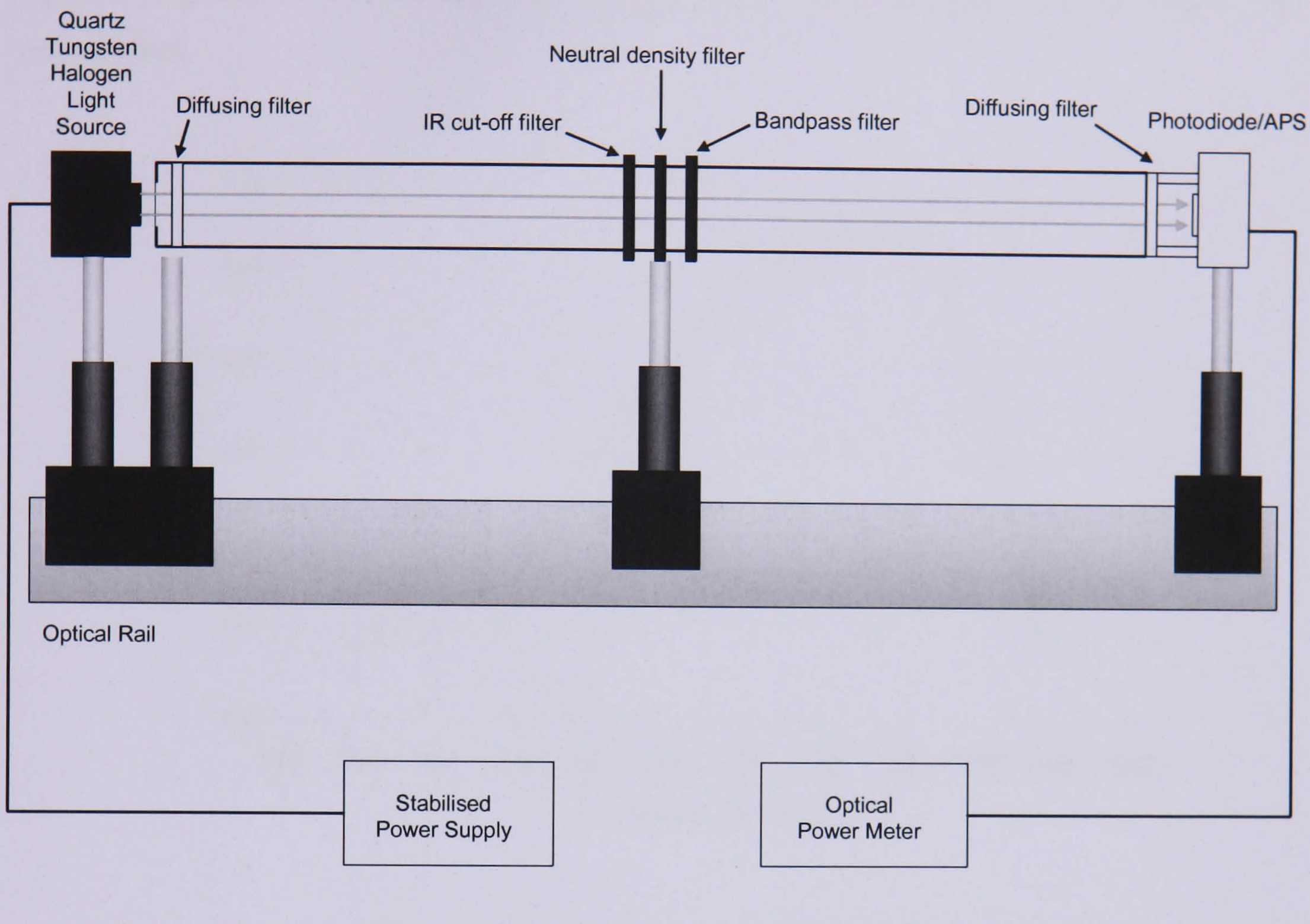


Figure 8.4 Experimental setup for electro-optical characterisation

Figure 8.4 shows the experimental setup used to perform the QE characterisation. A 20 W Quartz Tungsten Halogen (QTH) light source was used for illumination. This had a stability of < 1 % peak-to-peak variation in intensity. A uniform beam was obtained by passing the light output though a perspex diffusing filter and a collimating assembly. Wavelength selection was performed with the use of eight narrow band pass interference filters ranging from 400 to 1000 nm, with a band-width of 10 nm. An infrared cut off filter was also available to block any infra-red radiation above 1100 nm and the level of illumination was controlled using reflective neutral density (ND) filters. The beam was finally passed through a second diffusing filter immediately before hitting the sensor. Baffling was used to interface the sensor to the beam and ensure that only light passing through the filters was detected.

The incident light power was measured using a calibrated 1 cm^2 Newport 818-UV series photodiode, which had an enhanced UV response to improve the accuracy of power

measurements in this part of the spectrum. The diode was used in conjunction with an optical power meter to measure the incident power at a given wavelength. The photodiode responsivity is shown in **Figure 8.5**. The calibration data enabled an adjustable gain factor to be set such that the power measurement at a given wavelength was correct.

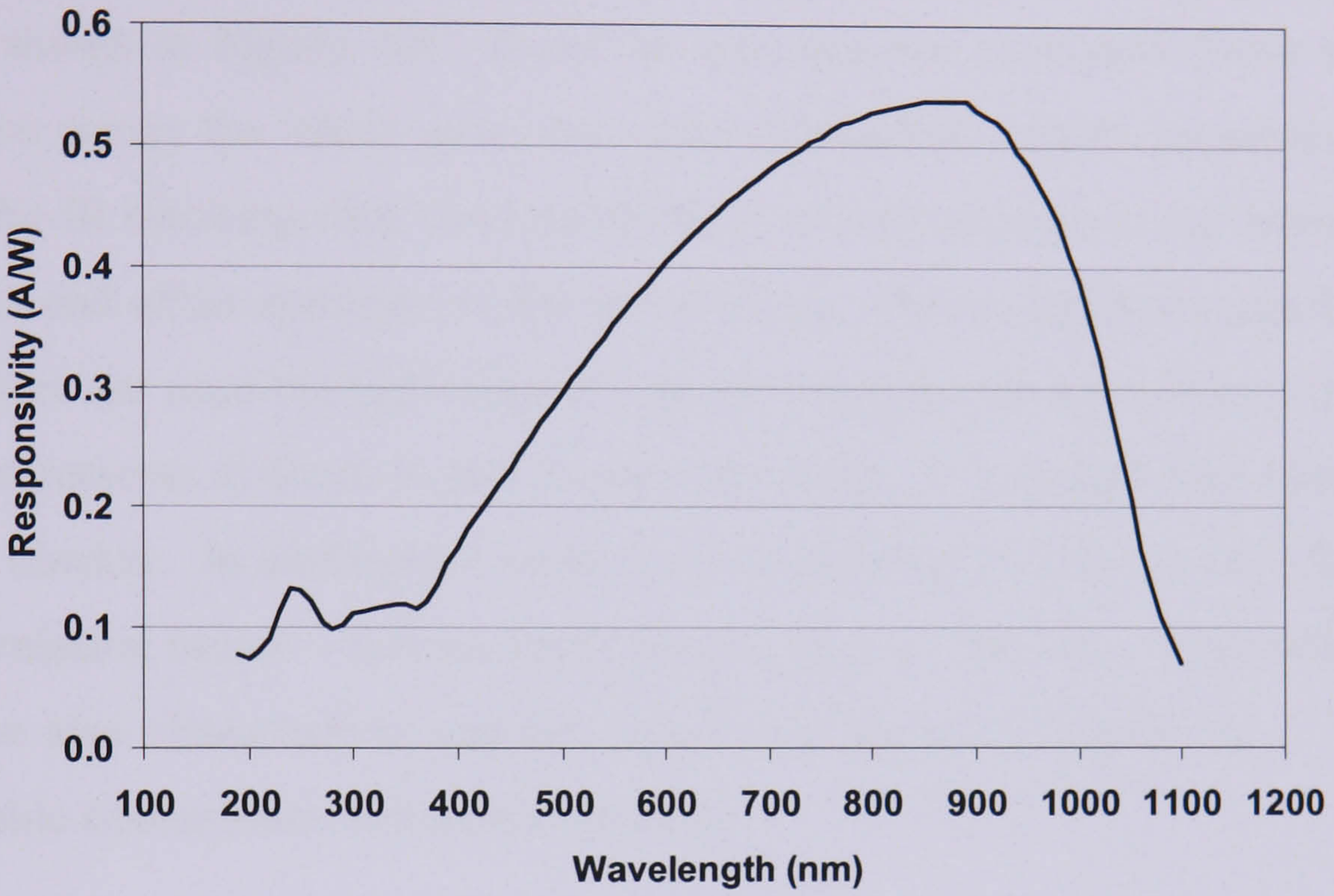


Figure 8.5 Responsivity of the calibrated photodiode

8.3.2. System calibration

Before the filters were used their transmission characteristics were investigated using a calibrated Hitachi U-4100 Spectrophotometer. This was done to ensure spurious wavelengths were not passing through any imperfections, such as pin-holes, caused by surface damage. The transmission of each filter was analysed from a wavelength of 370 to 1200 nm in 0.5 nm steps. The transmission curves for the IR blocking and band-pass filters are shown in **Figure 8.6**. It can be seen that the band-pass filters show good performance across the whole spectrum with well-defined narrow transmission peaks. However the IR blocking filter does not perform as well because it also blocks sections of the lower end of the spectrum at 400 and 450 nm. This means that when the 400 and 450 nm filters are used the light intensity illuminating the sensor will be very low and make measurements difficult in this wavelength range. It was therefore decided not to use the IR blocker. In hindsight it would have been better to have an edge filter with a clear transmission below ~ 600 nm and blocking above ~ 600 nm. The neutral density filters were also characterised and the results are shown in **Figure 8.7**. The filters showed stable transmission across the spectrum.

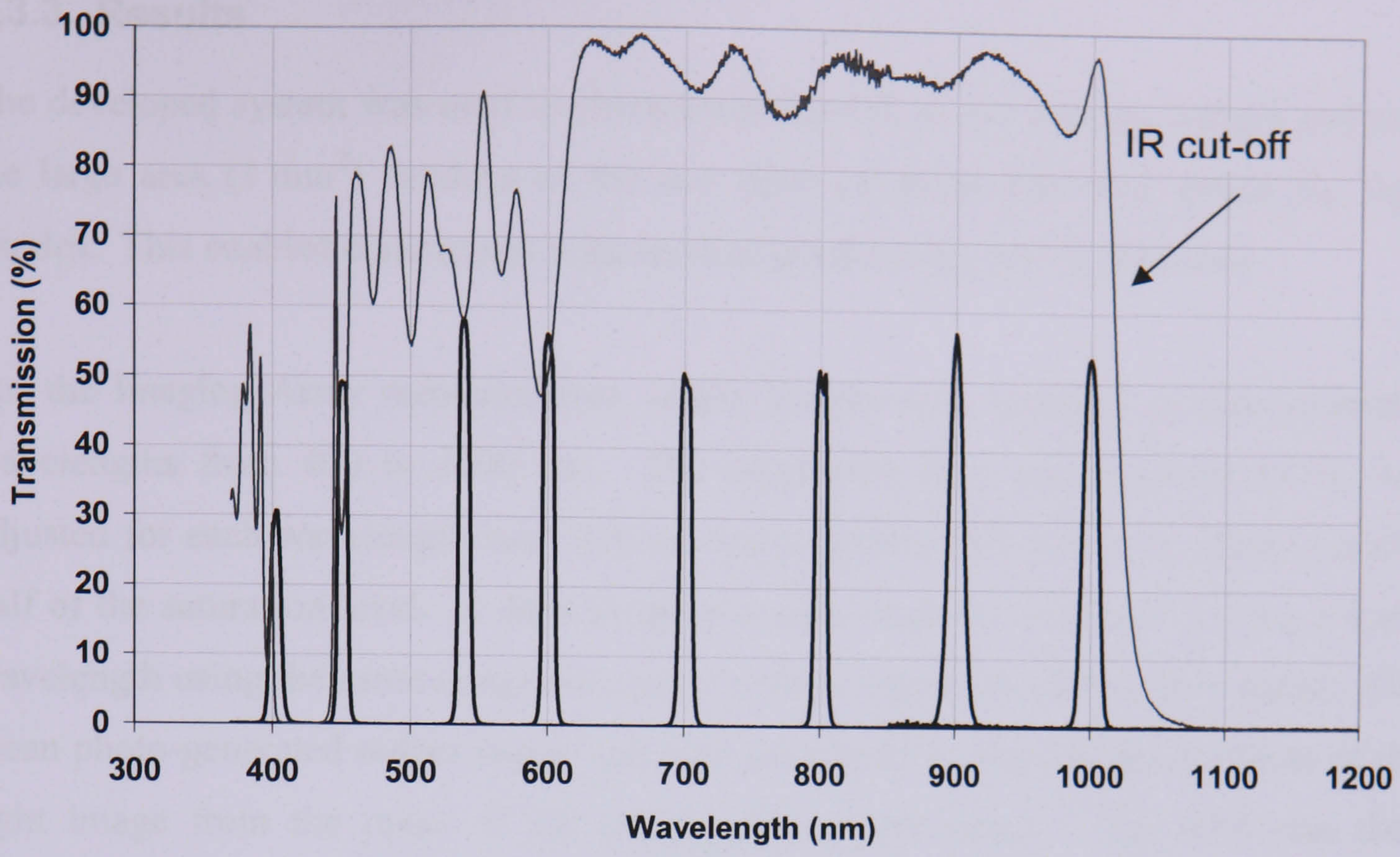


Figure 8.6 Band-pass and IR cut-off filter characterisation

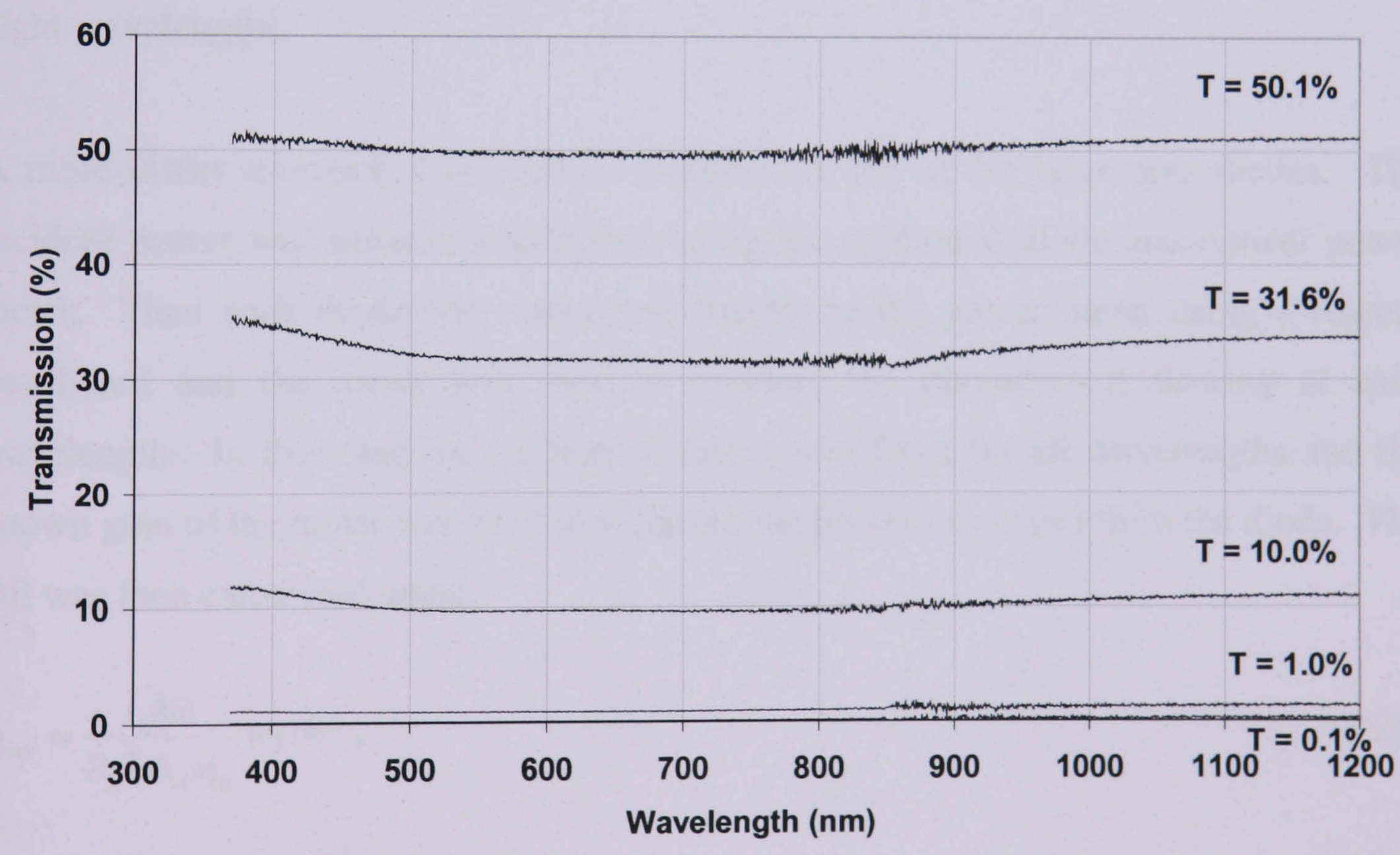


Figure 8.7 Neutral density (ND) filter characterisation

8.3.3. Results

The developed system was used to characterise the QE of the Imaging Arrays and also the large area (1 mm^2) versions of the two types of diode structures within the Test Diodes. This enabled comparison with an ideal pixel having 100 % fill factor.

For the Imaging Array measurements, bright images were acquired at eight different wavelengths from 400 to 1000 nm. The integration time and incident power was adjusted for each wavelength such that the mean pixel signal level was approximately half of the saturation level. A dark image was also acquired from each device at each wavelength using the same integration time to allow subtraction of the dark signal. The mean photo-generated output signal was then calculated by subtracting the mean of the light image from the mean of the corresponding dark image. The APS was then removed and the calibrated photodiode was placed in the same image plane. The incident power for the selected wavelength was then measured using the optical power meter with the appropriate calibration factor entered. This process was repeated for all eight wavelengths.

A more direct approach was used to measure the QE of the large area diodes. The incident power was measured as before using the calibrated diode and optical power meter. Then each diode was connected directly to the power meter using a custom headboard and the meter was used to measure the photocurrent flowing at each wavelength. In this case the calibration factor was fixed for all wavelengths and the known gain of the meter was used to work out the photocurrent (i_P) from the diode. The QE was then calculated using:

$$\eta_{int} = \frac{i_P hc}{P_\lambda \lambda A_P q_e} \times 100\% \qquad (8.2)$$

The results for the Imaging Arrays and large area diodes are shown in **Figure 8.8**. For the Imaging Arrays the QE of CMOS002 was 21-36 % higher than CMOS001 depending on the wavelength. The QE peaked in the range 500 to 600 nm at 21 ± 5 % for CMOS002 and 16 ± 4 % for CMOS001. Both the large area diodes showed similar QE performance across most of the spectrum. The QE peaked at 40 % in the same range as the Imaging Arrays for both diodes.

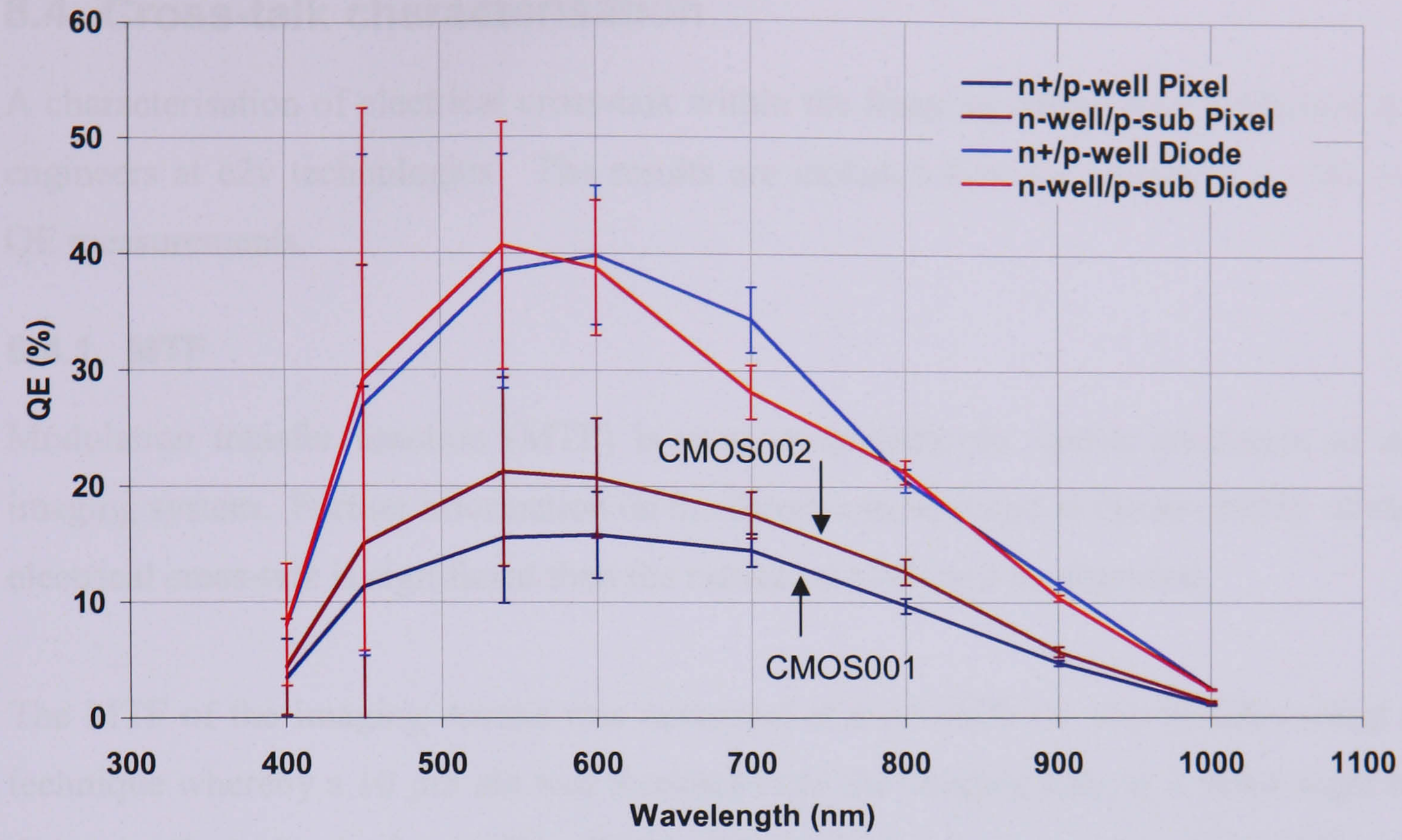


Figure 8.8 Test Structures quantum efficiency measurements

8.4. Cross-talk characterisation

A characterisation of electrical cross-talk within the Imaging Arrays was performed by engineers at e2v technologies. The results are included here for comparison with the QE measurements.

8.4.1. MTF

Modulation transfer function (MTF) is used to quantify the spatial resolution of an imaging system. Further information on the theory can be found in Hecht (2002). If the electrical cross-talk is significant then the measured MTF will be degraded.

The MTF of the Imaging Arrays was measured at three different wavelengths using a technique whereby a 10 μm slit was focussed onto the imaging area, at a small angle to the row (e2v technologies, 2003). **Figure 8.9** shows the slit images for CMOS001 and **Figure 8.10** shows the slit images for CMOS002. The type-001 device shows increased charge spreading compared with the type-002 device and the spreading also visibly increases as the wavelength increases.

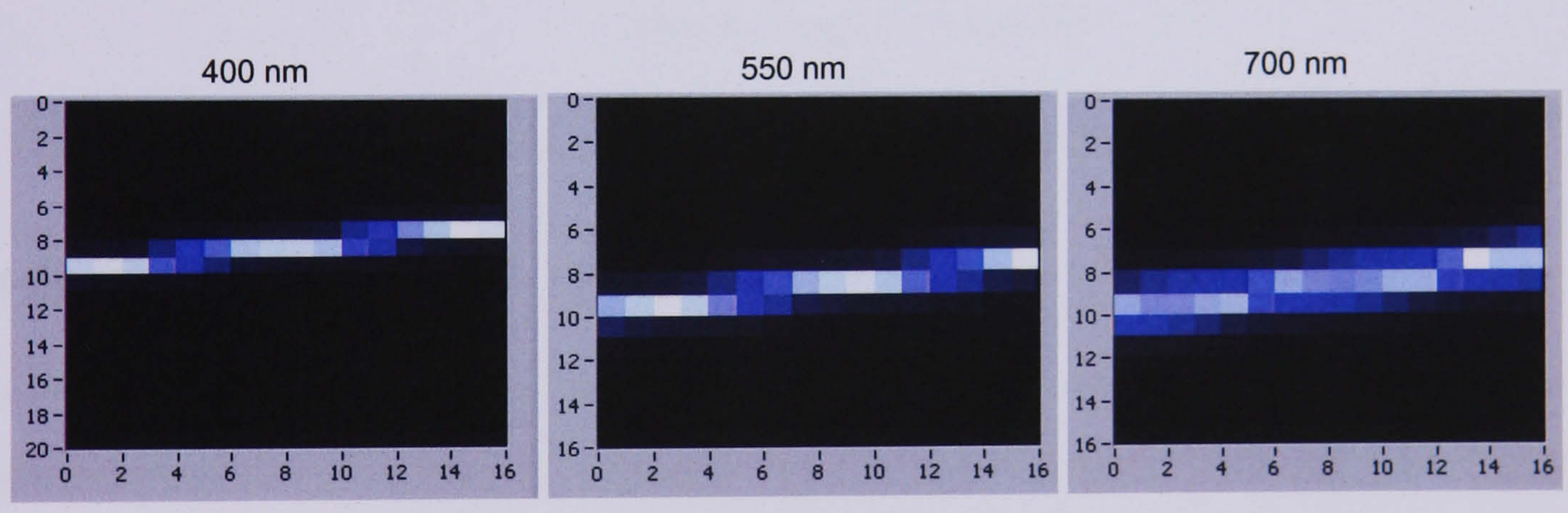


Figure 8.9 Slit images at 400, 550 and 700 nm, acquired with CMOS001 (n+/p-well diode)

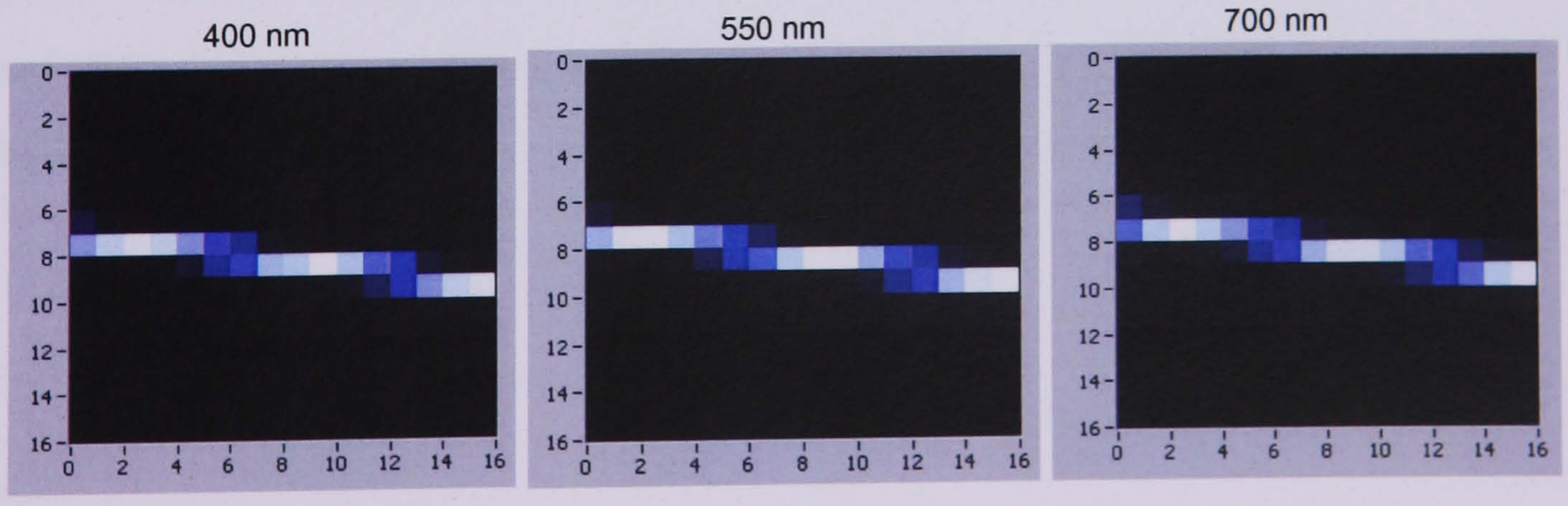


Figure 8.10 Slit images at 400, 550 and 700 nm, acquired with CMOS002 (n-well/p-sub diode)

A specially developed analysis tool was used to process the slit images and produce MTF curves for both devices. **Figure 8.11** shows the MTF versus spatial frequency for the range of wavelengths with correction for the MTF of the measurement optics. The MTF is higher for the type-002 device for all wavelengths.

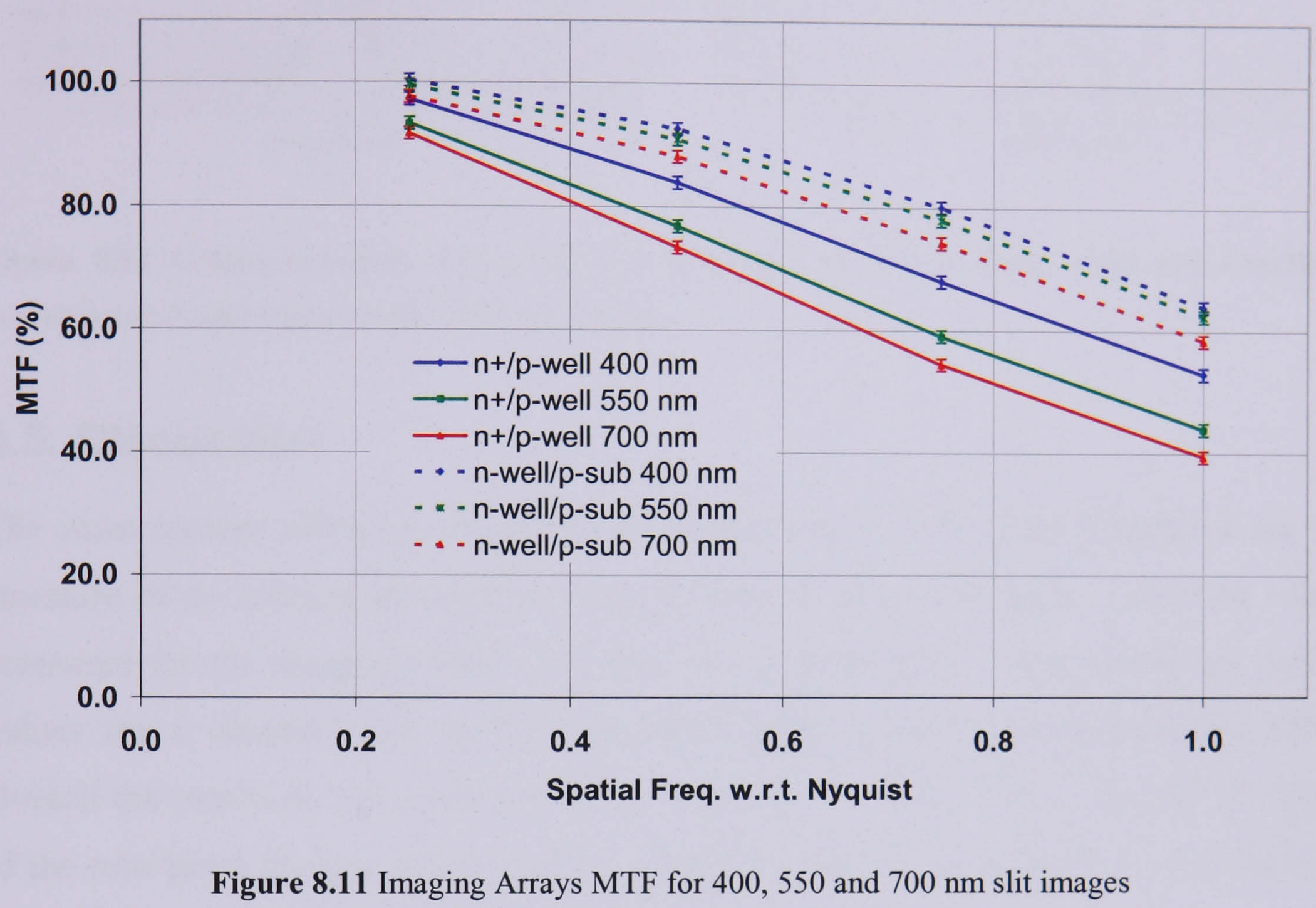


Figure 8.11 Imaging Arrays MTF for 400, 550 and 700 nm slit images

8.4.2. Cross-talk

Row-row and column-column cross talk was investigated by rotating the 10 μm slit to align within a row or column and adjusting the signal level to half full well capacity. **Figure 8.12** shows the normalised response between rows for both Imaging Arrays. Increased column-column cross-talk can be observed in the CMOS001 device as the wavelength increases. The cross talk is lower for the CMOS002 device and not dependent on the wavelength. Similar results for the row-row effect were observed.

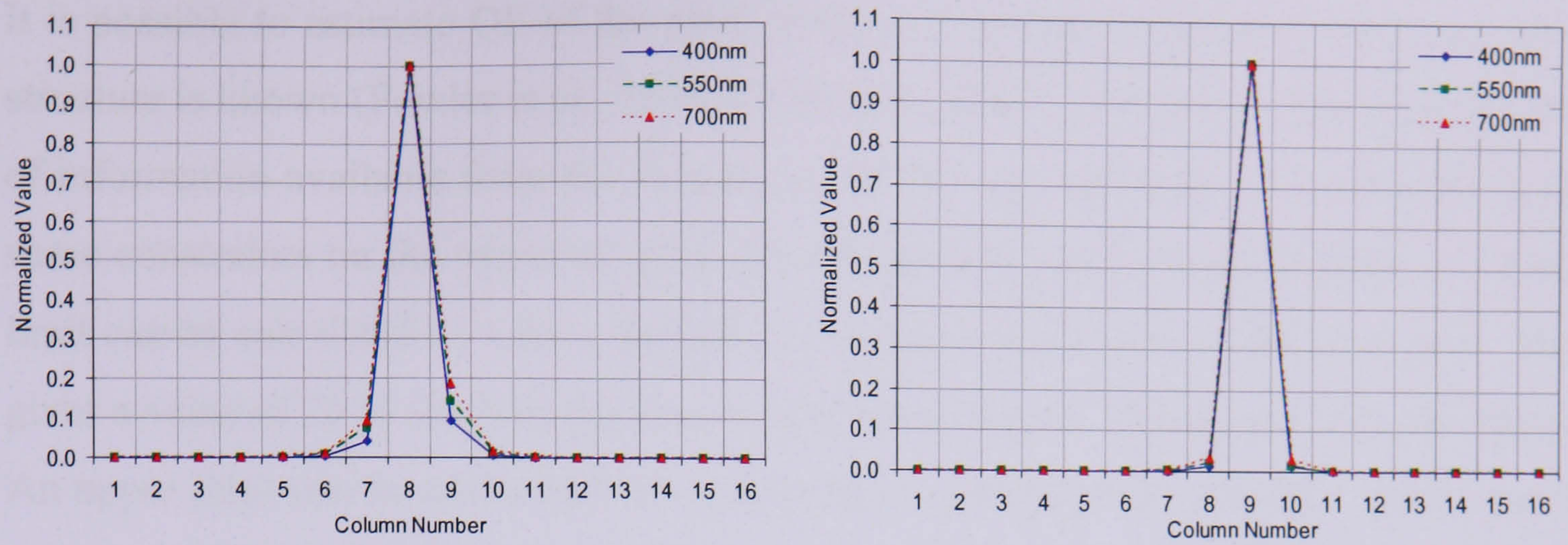


Figure 8.12 Column-to-column cross talk for CMOS001 (n+/p-well diode) (left) and CMOS002 (n-well/p-sub diode) (right), at half full well capacity

8.5. Discussion

The main factors affecting electro-optical performance in the Test Structures are the structure of the photodiode depletion region and the pixel fill factor. The QE values measured for the Imaging Arrays are shown in **Figure 8.13**. Also shown are typical values for a standard e2v CCD77 scientific grade device (e2v technologies, 2006). Overall the results do not compare well with the CCD. This is due to the low fill factor of the new pixel designs and the relatively shallow depletion depth of the two types of photodiode structures compared with the CCD.

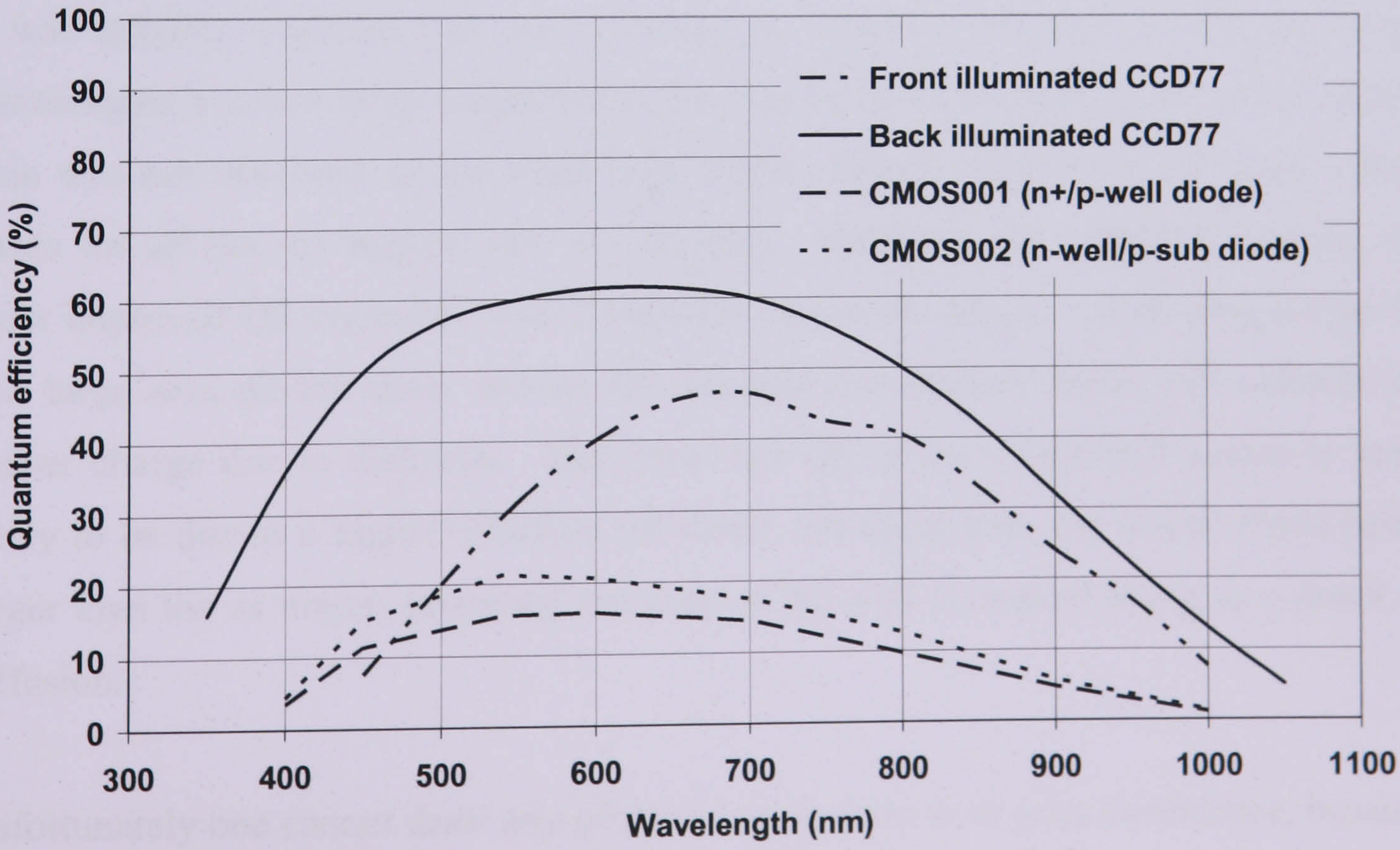


Figure 8.13. Comparison between the Imaging Arrays QE and different variations of e2v CCD77

It is possible to estimate QE of the pixel designs if enough information about the pixel structure is known (Fowler et al., 1998, Chen et al., 2007). However in this case the lack of information available from the foundry made this very difficult. It is possible to put some constraints on the expected pixel QE by estimating the pixel fill factor. A lower limit can be calculated by taking the ratio of the photodiode area to the pixel area. This gives a value of 25 % for both devices as both have 100 μm^2 diodes and 400 μm^2 pixels. An upper limit can be calculated by estimating the extent of the optically dead areas in the pixel. In both designs this was found to be ~ 35 %, giving an upper limit on the fill factor of 65 %. If the values measured for the large area diodes are assumed to be correct then the pixel QE should scale with the fill factor. The ratio between the values measured for the large area diodes and the pixels ranged from 2:1 to 3:1, implying a fill factor ranging from 33 to 50 %. This lies in the lower half of the predicted fill factor range of 25-65 %. One would expect this to be the case because some of the charge generated in the pixel will be collected directly by the readout circuitry rather than the diode. The results from the large area diodes show that a maximum QE of 40 ± 5 % is attainable with this process but it is ultimately limited by the fill factor. If the pixel size cannot be increased, a smaller feature size process would need to be used to ensure a more compact layout of the readout circuitry. Ideally using backside illumination would eliminate the problem.

It was initially expected that the n-well/p-sub diode would improve QE at longer wavelengths because of the deeper depletion depth compared with the n+/p-well diode. This was not observed as the large area diodes showed similar performance within errors for all but the highest two wavelengths. However, the CMOS002 device did show improved QE compared with CMOS001 across the range. It is thought that the two large area diodes show similar QE because the shallow diode still collects the deeper charge due to diffusion. The improved QE of the CMOS002 device is more likely to be due to a higher effective fill factor, resulting from the n-well diode being larger than the as drawn geometry, because of the well formation being as a result of diffusion.

Unfortunately one cannot draw any of these conclusions with great confidence, because the uncertainties in the measurements for wavelengths below 700 nm are too large.

The extra electro-optical characterisation performed by e2v technologies provided a further understanding of the two types of photodiode structures. The measurements showed that the electrical cross-talk was worse for the n+/p-well diode. The charge spreading was visible in the unprocessed slit images obtained from CMOS001, whereas it was not observed in CMOS002. The increased cross-talk was confirmed by the degradation of MTF in the n+/p-well diode and the column (and row) measurements. The degraded performance is due to the shallower depletion depth of the n+/p-well diode, which uses an n+ implant to a depth of only 0.3 μm. If the TS50 fabrication process were to be used in the future then the best candidate for optimal electro-optical performance is the deeper n-well/p-sub diode. However performance could be improved further by using an even deeper diffusion/implant to form the diode. It would also be desirable to use a manufacturing process that utilises high resistivity epitaxial silicon. This would also enable the depletion region to extend further into the silicon for a given reverse bias voltage.

8.6. Summary

This chapter has outlined a study of the electro-optical performance of the new Test Structures. The chapter began by outlining the main parameters affecting electro-optical performance in an active pixel. The approach to measuring quantum efficiency was then described along with a system developed by the author to perform the measurement. The QE was measured across the visible spectrum for pixels within the Imaging Arrays and large area versions of the diodes with 100 % fill factor. The pixel with the deeper depletion diode showed improved QE compared with the shallower depletion version. However the large area versions of the diodes showed similar QE performance suggesting the deeper depletion was not necessarily improving the QE. It is more likely that, due to the manufacturing process, the effective fill factor of the n-well diffusion diode was larger. The QE measurements were compared with cross-talk measurements performed by e2v technologies. These measurements showed that electrical cross-talk was significantly reduced by the deeper depletion diode. The main conclusions are that future designs should maximise fill factor by utilising a smaller feature size or ideally utilise back-side illumination. The photodiode used should also have as large a possible depletion depth to collect efficiently the deeply photo-generated charge within each pixel ensuring good spatial resolution.

Chapter 9: Conclusions and future work

This chapter summarises the key findings of this thesis and highlights some of the developments needed to enable APS devices for scientific imaging applications.

9.1. Sensor design and development

This work, which started in 2004, to develop high performance CMOS APS, was completely new to the author and designers/engineers within e2v technologies. It was thought that the research was being performed into a well established technology, but it was found that the analysis is a lot more complicated than sometimes indicated in the literature. Consequently the completion of this thesis has enabled the author to gain a detailed understanding of CMOS image sensor development, from design through to final characterisation.

In particular, this thesis has highlighted the importance of designing test structures to explore various effects of individual components, rather than producing a specific stand-alone imaging device. It is even more important to design test structures when developing CMOS devices due to the regular changes in process technology, compared with the matured CCD manufacturing process.

The knowledge gained from this thesis has provided an important stepping stone enabling further development of CMOS APS for future high performance scientific applications.

9.2. Responsivity, noise and dynamic range

The main characteristics of the Test Structures manufactured using the TS50 process are summarised in **Table 9.1**.

The key findings from the initial electrical characterisation were that the output responsivity was non-linear with signal, and that the noise was limited by the kTC component caused by resetting the sense node capacitance. The lower capacitance n-well/p-sub diode showed higher responsivity and lower noise performance. These results were as expected due to the fundamental limitations of the 3T pixel design.

In terms of the existing devices, further work is needed to characterise the responsivity non-linearity and the effect of node capacitance on output responsivity and reset noise.

Also further work is needed to investigate whether soft reset is an effective method of reducing the reset noise. In theory the use of a small photodiode would reduce the kTC component due to the reduced capacitance, but this would reduce the collecting area of the photodiode. Other than reducing the node capacitance, lower noise could be achieved by utilising a pixel design with CDS capability. This would require a pixel with a charge transfer capability such as the 4T pinned photodiode and an additional analogue CDS noise cancellation circuit on-chip. However a more recently developed approach could eliminate the extra circuitry by converting the two samples to digital signals and performing the noise cancellation in the digital domain.

Device	**CMOS001**	**CMOS002**
Reset type	n-channel raster	n-channel global
Pixel pitch (μm)	20	20
Pixel area (μm^2)	400	400
Photodiode type	n+/p-well	n-well/p-sub
Implant/well depth (μm)	0.3	1.2
Diode area (μm^2)	100	100
Fill Factor (%)	65 ± 5	65 ± 5
Output responsivity ($\mu V/e^-$)	3.0 ± 0.1	4.7 ± 0.3
Dark current (e^-/pixel/s), 20 °C	1880 ± 100	1830 ± 126
Dark current (pA/cm^2), 20 °C	75 ± 4	73 ± 5
Sense node capacitance (fF)	36 ± 1	23 ± 1
Noise (e^- r.m.s.), 23 °C	87 ± 9	69 ± 5
Full well capacity (ke^-)	400 ± 13	250 ± 16
Dynamic range (dB)	73.3 ± 0.9	71.2 ± 0.8
QE (%), 600 nm	16 ± 4	21 ± 5

Table 9.1 Summary of the Test Structures characteristics

9.3. Dark signal and hot-carrier effects

The major experimental study involved characterisation of the various sources of dark signal in the 3T CMOS pixel. The key findings from the work were as follows:

- During integration the dark signal is dominated by conventional thermally generated leakage currents
- The magnitude of the thermally generated leakage current lay between that of an inverted and non-inverted mode CCD
- During the read-out phase the dark signal is dominated by parasitic currents due to hot-carrier effects caused by activation of the in-pixel source follower transistor
- The hot-carrier induced currents are three orders of magnitude larger than the thermally generated leakage current
- The hot-carrier effects may limit the overall dark signal performance and may be the dominant effect under low temperature operation

Further work is required to investigate the variation of conventional leakage current with photodiode size. The leakage current during integration could be minimised by utilising more recently developed customised structures such as the pinned photodiode.

The observation of the hot-carrier effect was a key finding of this thesis and the effect on active pixels is mentioned very rarely in the literature. The discovery only arose due to the use of smaller scale Test Structures and highlighted the importance of designing the Test Pixels in addition to the Imaging Arrays. The design of the readout circuit must be carefully considered to minimise the hot-carrier effects during readout, especially for devices with "intelligent pixels" containing many active transistors and for applications requiring true "non-destructive read-out".

9.4. Electro-optical performance

The electro-optical performance of the sensor was essentially limited by the fill factor of the pixel and the extent of the depletion region of the photodiode. Ideally the fill factor problem would be eliminated by utilising back-thinned CMOS devices, although minimal work has been done in this area. The alternative is to maximise fill factor by using innovative layout such as the shared transistor pixel designs, or use smaller

feature size processes. Although the problem with the smaller feature sizes used by advanced CMOS processes is that they have low resistivity epitaxial silicon, small depletion depths and large leakage currents.

9.5. Future prospects

The results presented in this thesis demonstrate that, compared with the mature CCD technology, active pixel sensors have some major performance deficiencies in the areas of noise, dark signal and quantum efficiency. These deficiencies are mainly due to the fact that CMOS fabrication processes are optimised for high-speed logic circuits whereas the CCD fabrication process has been optimised solely for imaging applications over forty years. The continued trend for more advanced CMOS processes will degrade the performance currently available with a standard CMOS process.

CMOS APS are already capturing market share in the larger consumer-imaging sector due to the significant developments that have been made during the three years of this study. However it is clear that initial predictions from the early 1990's, that CMOS image sensors would soon replace the CCD, are unfounded. It seems more likely that the active pixel sensor will co-exist with the CCD in the higher-end scientific and astronomical imaging sectors. The APS is most likely to replace the CCD for such applications that require low power, high levels of system integration and radiation hardness. Clearly further developments are required for the active pixel technology to compete with the CCD for the most demanding visible imaging applications, primarily in the areas of achieving backside illumination and deep depletion devices and low noise sampling techniques.

A major problem is that some of the significant developments made by large consumer manufacturers are not easily available to the scientific community due to the low volumes required. So even if the devices developed can compete with the CCD on performance, they will still cost as much to produce removing an initial advantage of the CMOS APS approach.

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