# Power Engineering Letters

## Capacitive Compensation at Nonsinsoidal Buses Based on IEEE Std. 18-1992

A. F. Zobaa, *Member, IEEE*

***Abstract*—This letter presents a proposed method for finding the optimum fixed compensating capacitor to minimize the voltage harmonic distortion at a load bus while holding the power factor at a desired value and constraining the nameplate kilovar of the compensating capacitor, its rated voltage rms, and its rated current rms as constraints according to IEEE Std. 18-1992. Also, the values of the compensating capacitor, which would create resonant conditions, would be omitted from the solution. Finally, the contribution of the newly developed method is demonstrated in an example taken from previous publications.**

***Index Terms*—Harmonics, power factor, power quality.**

### I. Introduction

In case of nonsinusoidal sources, maximum transmission efficiency $(\eta)$, minimum transmission loss $(TL)$, and maximum power factor $(PF)$ do not lead to the same shunt compensator values [1]. When the three criteria are combined into one model and solved by the penalty function approach, the results do satisfy the three criteria by one value of capacitor [2]. There are several measures commonly used for indicating the harmonic content of a waveform with a single number. One of the most common is total harmonic distortion $(THD)$, which can be calculated for either voltage $(VTHD)$ or current $(ITHD)$. $THD$ is a measure of the effective value of the harmonic components of a distorted waveform, that is, the potential heating of the harmonics relative to the fundamental. The rms value of the total waveform is not the sum of the individual components, but is the square root of the sum of the squares. $THD$ is a very useful quantity for many applications, but its limitations must be realized. It can provide a good idea of how much extra heat will be realized when a distorted voltage is applied across a resistive load. Likewise, it can give an indication of the additional losses caused by the current flowing through a conductor. However, it is not a good indicator of the voltage stress with a capacitor because that is related to the peak value of the voltage waveform, not its heating value.

### II. Problem Description

Fig. 1 is a single-phase equivalent circuit of a bus with compensating capacitor, experiencing voltage harmonic distortion

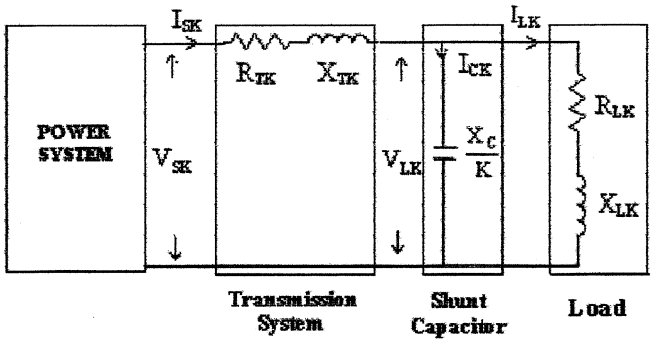


Fig. 1. Single-phase equivalent circuit for K-th harmonic with shunt capacitive compensator.

at harmonic order $K$ because of a voltage source, $\mathrm{v_{SK}}$. The Thevenin voltage source representing the utility supply is

$$\mathrm{v_S(t)} = \sum_{\mathrm{K}} \mathrm{v_{SK}(t)} \tag{1}$$

where $K$ is the order of harmonic present. The K-th harmonic Thevenin source and load impedances are

$$\mathrm{Z_{TK}} = \mathrm{R_{TK}} + \mathrm{jX_{TK}} \tag{2}$$

and

$$\mathrm{Z_{LK}} = \mathrm{R_{LK}} + \mathrm{jX_{LK}}. \tag{3}$$

The approach will be to minimize voltage harmonic distortion on the load by adjusting $X_C$. The voltage harmonic distortion at the compensated load terminals is defined as

$$\mathrm{VTHD} = \frac{\sqrt{\sum_{\mathrm{K}>1} \mathrm{V_{LK}^2}}}{\mathrm{V_{L1}}.}$$

Capacitors shall be capable of continuous operation provided that none of the following limitations are exceeded [3]:

a) 135% of nameplate kvar;
b) 110% of rated voltage rms, and crest voltage not exceeding $1.2 * \sqrt{2}$ of rated rms voltage $(V_{CR})$, including harmonics but excluding transients;
c) 180% of rated current rms including fundamental and harmonic currents.

By the use of penalty function method, the problem of minimizing the voltage harmonic distortion $(VTHD)$ with expressions for the $PF$, the kvar of the compensating capacitor

Manuscript received February 15, 2003.

The author is with the Electrical Power and Machines Department, Faculty of Engineering, Cairo University, Giza 12613, Egypt (e-mail: a.zobaa@eng.cu.edu.eg).

Digital Object Identifier 10.1109/TPWRD.2003.817532

($kvar_C$), its voltage rms ($V_C$), and its current rms ($I_C$) taken as constraints can be reformulated. The algorithm of this method is documented in [4].

After formulating the objective function and the constraints, the problem addressed in this study becomes

$$\begin{aligned} &\text{Minimize } \mathrm{VTHD}(\mathrm{X_C}) \\ &\text{Subject to}: 90\% \le \mathrm{PF}(\mathrm{X_C}) \le 100\% \\ &\qquad \mathrm{kvar_C}(\mathrm{X_C}) \le 135\% \\ &\qquad \mathrm{V_C}(\mathrm{X_C}) \le 110\% \\ &\qquad \mathrm{I_C}(\mathrm{X_C}) \le 180\% \end{aligned} \tag{4}$$

where $\mathrm{X_C}$ is not part of solution of the following equation (the capacitor values determined by this equation are those, which would create a series and parallel resonant conditions)

$$\mathrm{A_3X_C^2} + \mathrm{A_2X_C} + \mathrm{A_1} = 0 \tag{5}$$

where

$$\mathrm{A_1} = \mathrm{X_T}\left[(\mathrm{K}^2\omega_o\mathrm{X_L})^2 + (\mathrm{K}\omega_o\mathrm{R_{LK}})^2\right]$$

$$\mathrm{A_2} = -\omega_o^2\left[\left(\mathrm{R_{LK}^2} + (\mathrm{KX_L})^2 + 2\mathrm{K}^2\mathrm{X_L}\mathrm{X_T}\right)^2\right]$$

and

$$\mathrm{A_3} = \omega_o^2[\mathrm{X_T} + \mathrm{X_L}]$$

where

- $\omega_o$ fundamental frequency of the system;
- $\mathrm{X_L}$ reactive reactance of the load at the fundamental frequency;
- $\mathrm{X_T}$ reactive reactance of the transmission system at the fundamental frequency.

The capacitor values determined by this equation are those, which would create a series and parallel resonant conditions. It represents only the series resonance taking the solution where the square root of the discriminant is positive. Under these conditions, the power factor will reach a minimum. The other solution of (5) corresponds to resonance between the load and the combination of source impedance and the compensating capacitor. It should be pointed out that a parallel resonant circuit at the load implies unity power factor. Consequently, only the series resonant conditions, which would result large harmonic currents, are omitted from the solution procedure. Finally, for known harmonic contents at the source, (5) can be used repeatedly for calculating all capacitor values, which would form resonant circuits at different harmonic frequencies.

## III. Example and Simulated Results

Consider the system under study as the following description [6]: A three-phase load of 5100 kW and 4965 kvar is connected to a supply bus with voltage 4160-V (2400 line-to-ground), 60-Hz frequency, and 80-MVA short circuit capacity. The resistance to reactance ratio of the power system impedance is assumed to be 10%. The voltage is distorted; it contains 5% fifth harmonic, 3% seventh harmonic, 2% eleventh harmonic, and 1% thirteenth harmonic. The system data for equivalent single-phase model at the fundamental frequency are

$$\text{Power system impedance} = 0.021\,63 + \mathrm{j}0.2163\ \Omega$$

TABLE I
Capacitor Limits (IEEE Std. 18-1992)

| Item | Calculated (%) | Limit (%) | Exceeds limit |
|---|---|---|---|
| rms voltage | 101.57 | 110.00 | No |
| rms current | 104.74 | 180.00 | No |
| kvar | 104.22 | 135.00 | No |
| Crest voltage / ($\sqrt{2}$ * $V_{CR}$) | 76.17 | 120.00 | No |

$$\text{Load impedance} = 1.7421 + \mathrm{j}1.696\ \Omega.$$

The rated voltage of the capacitors used is 4160 V.

The results, performance parameters after compensation, of this example using the algorithm of penalty function method [4] are summarized below

$$\begin{aligned} \mathrm{X_C} &= 2.55\ \Omega\ (\text{star connected}) \\ \mathrm{PF} &= 90.00\% \\ \eta &= 99.22\% \\ \mathrm{TL} &= 13.72\ \mathrm{kW} \\ \mathrm{VTHD} &= 5.03\% \\ \mathrm{ITHD} &= 30.44\% \\ \text{Supply current} &= 796.33\ \mathrm{A\ rms} \\ \text{Displacement power factor} &= 94.20\%. \end{aligned}$$

Table I shows that the resultant values come out well within standard limits. If the resultant values are greater than standard limits, it is a good idea [6] to use capacitors with a higher voltage rating. For example, 4800-V capacitors are used for a 4160-V application. In the IEEE Std. 519-1992 [6], the objectives are to limit the maximum individual harmonic voltage to 3% of the fundamental voltage and the total harmonic distortion of the voltage to 5%. The resultant value comes out well within standard limits.

## IV. Conclusions

A mathematical model is developed and a solution method is presented for minimizing the voltage total harmonic distortion at the load bus where it is desired to maintain the power factor at a desired level. It is shown that significant improvement in distortion levels can be achieved. Finally, the use of the presented method guarantees convergence and obtains the optimal capacitor in a unified manner. Ongoing research effort consists of the modification and application of this method to time variations of the load and system impedance.

## References


[1] M. M. Abdel Aziz, E. E. Abou Elzahab, A. M. Ibrahim, and A. F. Zobaa, "Skin effect on optimal power factor," in *Proc. Large Eng. Syst. Conf. Power Eng., LESCOPE 02*, Halifax, NS, Canada, June 2002, pp. 76–78.

[2] ——, "On the economic selection of capacitive compensator sizes in nonsinsoidal conditions," *IEEE Power Eng. Rev.*, vol. 22, no. 10, pp. 47–48, Oct. 2002.

[3] IEEE Standard for Shunt Power Capacitors, 1992.

[4] S. S. Rao, *Engineering Optimization Theory and Practice*: New Age International (P) Ltd., Publishers, 2000.

[5] P. F. Riberio, "Tutorial on harmonics modeling and simulation," in *Proc. IEEE Power Eng. Soc. Winter Meeting*, Tampa, FL, Feb. 4, 1998.

[6] IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems, 1992.