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EMSN: An Energy-Efficient Memristive Sequencer Network for Human Emotion Classification in Mental Health Monitoring

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***Abstract*—Mental health problems are an increasingly common social issue severely affecting health and well-being. Multimedia processing technologies via facial expression show appealing prospects in the consumer field for mental health monitoring, while still suffer from intensive computation and low energy efficiency. This paper proposes an energy-efficiency memristive sequencer network (EMSN) for human emotion classification, which offers an environmentally friendly approach for consumers with low cost and easily deployable hardware. Firstly, two-dimensional (2D) materials are employed to construct an eco-friendly memristor, the efficacy and reliability of which are confirmed through performance testing. Then, a sequencer block is proposed using memristive circuits. Notably, it is a core component of the EMSN, consisting of a bidirectional long short-term memory circuit, normalisation circuit module, and multi-layer perception module. After combining some necessary function modules, the EMSN can be achieved. Furthermore, the proposed EMSN is applied for human emotion classification. The experimental results demonstrate that the proposed EMSN has advantages in computational efficiency and classification accuracy compared to existing mainstream methods, indicating an advancement in consumer health monitoring.**

***Index Terms*—Human emotion classification, memristive circuit, two-dimensional (2D) materials, sequencer network.**

I. Introduction

Human emotion and feeling are fundamental to human experience, health and well-being, influencing cognition, memory, and targeted activity behavior such as learning, communication, and rational decision-making [1]. Mental health problems caused by negative emotions usually lead to diseases such as depression, addiction, and heart attack, which may severely affect quality of life [2]. Mental health monitoring is particularly urgent and important, especially for the development of sound mind and body. Considering facial expression is one of the most natural and universal signals for consumers to convey their emotional states and behavior intentions, multimedia processing technology using facial expression plays a vital role to understand and analyse mental states in consumer health monitoring [3]. Advanced research on artificial intelligence and psychology technology, numerous artificial neural networks, such as multilayer neural networks (MNNs) [4], convolutional neural networks (CNNs) [5-7], long short-term memory (LSTM) networks [8-10], and transformer networks [11], have been conducted on automatic human emotion classification to establish the relationship between facial expression and consumer mental health. Nevertheless, such multimedia processing approaches rely on conventional Von Neumann architecture, which requires physical separation of the processor and the memory. Meanwhile, this computing architecture fails to adequately accommodate the efficient parallel computation, active data access, and low-power consumption.

Neuromorphic computing is inspired by the functioning of the brain [12]. It has been used to establish an abiotic computing system in which the functioning resembles the human brain and to create ultra-low-power computers that possess autonomous learning and cognitive capabilities. Hence, this strategy makes it possible to achieve circuit implementation of different multimedia processing systems. So far, a number of neuromorphic computing systems have been proposed using different consumer electronics devices, such as spintronic devices, ferroelectric devices, and complementary phase-change memory devices [13]. Memristors are two-terminal electronic devices that exhibit non-volatility, high density, long retention, and long endurance and are potential candidates for neuromorphic computing [14]. Memristor was developed by Leon O. Chua in 1971 [15]. It is the fourth basic circuit element and is also linked to the physical devices introduced in 2008 by R. Stanley Williams and his team at Hewlett-Packard Labs [16]. With the development of memristor technology, this neuromorphic computing device has been proved effective in

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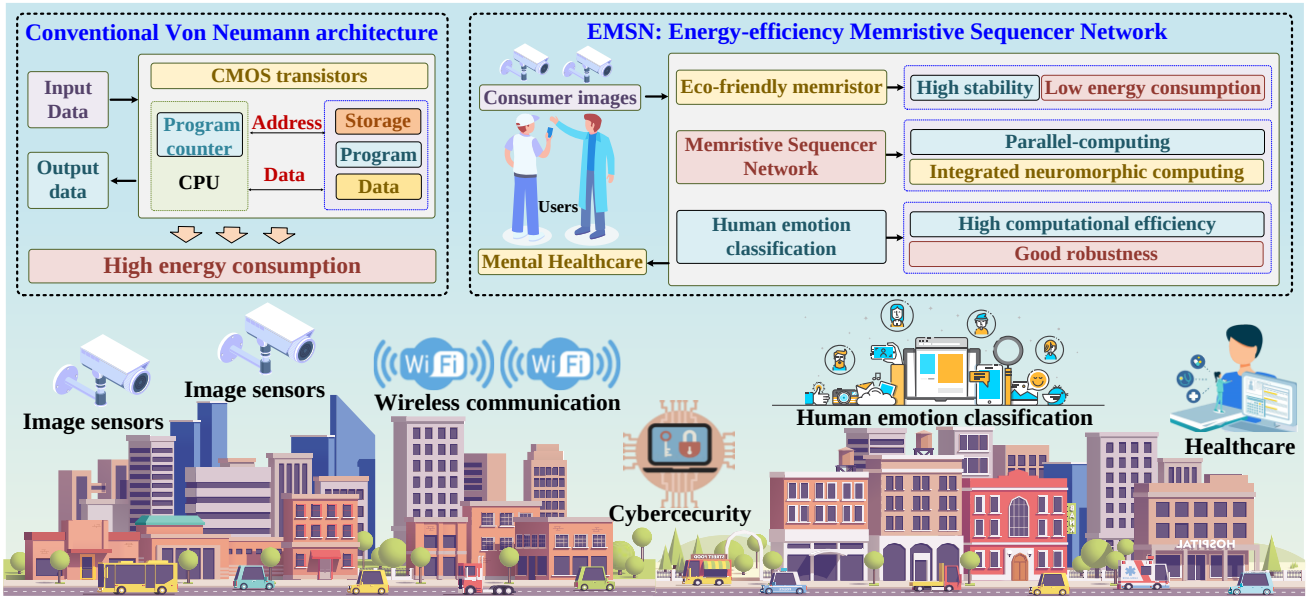

Fig. 1. Systemic comparison of von Neumann based multimedia processing systems and the proposed EMSN

the fields of artificial intelligent and computer vision [17-19]. A fully hardware-based memristive multilayer neural network demonstrated a recognition accuracy of 93.63% on a handwritten digit dataset [17]. The full-circuit implementation of the transformer network in accordance with the memristor was proposed, it can be used to realize character recognition [18]. A multimodal neuromorphic sensory-processing system for smart home applications was proposed in [19], offering an environmentally friendly method with easily deployable hardware. However, the current neuromorphic computing systems still suffer from some limitations. At the device level, the device variations may cause inaccurate encoding of network weights in neuromorphic computing because of immature fabrication technology and unstable material performance. Therefore, the neuromorphic computing devices with high stability are required. At the system level, efforts are needed to develop high performance processing algorithms that can realize a high-accuracy, consumer-friendly, and energy-efficient neuromorphic computing system.

Sequencer networks [20], one of the most important models for computer vision, have achieved state-of-the-art recognition accuracy and exceeded previous results in image classification. Despite the merits of sequencer network, the corresponding hardware implementation of sequencer network has not been developed due to the complex calculation process and data storage. In this work, we propose an energy-efficiency memristive sequencer network (EMSN), aiming at solving von Neumann bottleneck (mainly refer to high energy consumption) emerging in consumer health monitoring. The systemic comparison of von Neumann based multimedia processing systems and the proposed EMSN is provided in **Fig. 1**. The main contributions of this work are summarised below:

1) An Ag-Au/M_OSe_2-doped Se/Au-Ag memristor with high stability is prepared. It is a promising candidate to emulate high-accuracy neuromorphic computing for consumer health monitoring.

2) The circuit design of EMSN is proposed, which avoids the separation of weight representation and computing, enabling a parallel-computed and highly integrated neuromorphic computing.

3) The correctness of the proposed EMSN is verified by human emotion classification. The results show that the proposed EMSN outperforms the existing state-of-the-art methods with high computational efficiency and good robustness.

The rest of this paper is structured as follows. Section II describes the fabrication and performance testing of the Ag-Au/M_OSe_2-doped Se/Au-Ag memristor. Section III demonstrates the overall architecture and the circuit-level design. In Section IV, the proposed system is applied to human emotion classification for verification. Finally, Section V presents the conclusion and future direction of the study.

II. Memristor Fabrication and Performance Testing

A. Fabrication of Ag-Au/$MoSe_2$-doped Se/Au-Ag Memristor

The fabrication of the Ag-Au/M_OSe_2-doped Se/Au-Ag memristor relies on the hydrothermal synthesis and the magnetron sputtering methods [21]. Specifically, the hydrothermal synthesis method is adopted to fabricate $MoSe_2$-doped Se microwires, and the magnetron sputtering method is used to prepare the Ag-Au electrodes (as shown in **Fig. 2**).

Step 1: Solution A is prepared by dissolving 0.1 moL Se powder and 0.1 moL ammonium molybdate $(NH_4)_6M_{O7}O_{24}\cdot H_2O$ into 25 mL deionised water.

Step 2: Solution B is prepared through the addition of 0.05 g surfactant (hexadecyl trimethyl ammonium bromide) to Solution A, after which it is continuously sonicated for 3 hours with the assistance of a magnetic stirrer.

Step 3: Solution B is placed in a 25 mL Teflon-lined container, after which it is heated in a muffle furnace for 48 hours at 227°C.

Step 4: Following 3 times centrifugation, the $MoSe_2$-doped Se microwire is secured from the heated Solution B.

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Step 5: The magnetron sputtering technique is employed to generate the Au electrode (space = 400 μm, area = 2,500 μm^2) on the Si/SiO_2 substrate.

Step 6: A four-probe test is used to select the $MoSe_2$-doped Se microwire, after which the microwire ends are fixed in the Au electrode and coated with a layer of Ag adhesive, thereby preparing the Ag-Au/$MoSe_2$-doped Se/Au-Ag memristor.

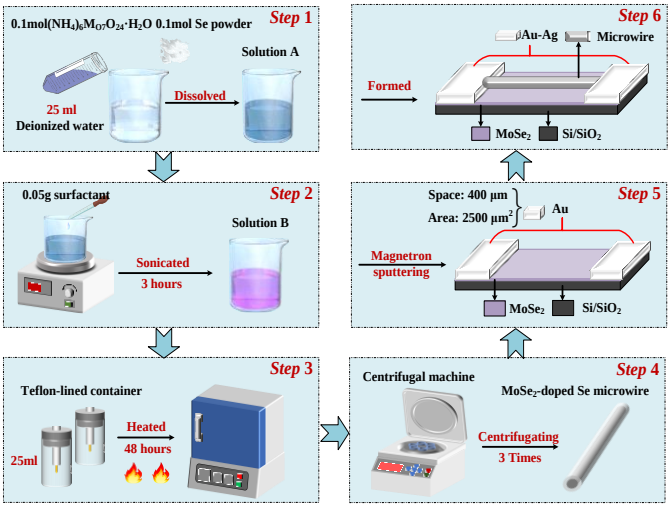

Fig. 2. The fabrication flow of Ag-Au/$MoSe_2$-doped Se/Au-Ag memristor

B. Performance Testing

The performance testing of Ag-Au/$MoSe_2$-doped Se/Au-Ag memristor is carried out through an electrochemical workstation (CHI-600D). The electrical characteristics are measured with ±3 V scanning voltages with a scan rate of 0.05 V/s, as shown in **Fig. 3**.

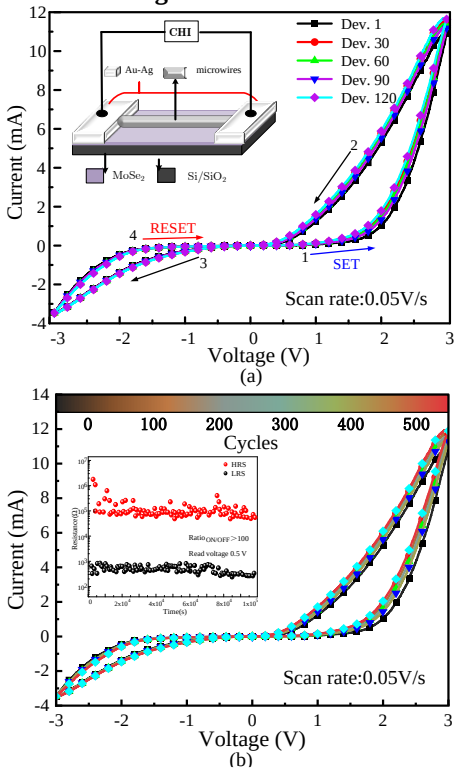

Fig. 3. The performance testing of Ag-Au/ M_oSe_2-doped Se/Au-Ag (a) device-to-device analysis; (b) cycle-to-cycle analysis

The measured I–V curves acquired by 120 memristors are indicative of extensive overlap. In addition, the inset comprises a structural depiction of the fabricated memristor. The findings from the testing indicate that Ag-Au/$MoSe_2$-doped Se/Au-Ag memristors possess robust device-to-device steadiness, as demonstrated in **Fig. 3(a)**. The overall I–V curves are asymmetrical in the positive and negative voltage regions, indicating that the fabricated memristors exhibit electronic resistive switching memory behavior. Specifically, in the first stage, the memristors remain in the high-resistance state (HRS). The scanning voltages rise from 0 V to 3 V. For this reason, the device currents are virtually unaltered up to the point that the scanning voltages surpass 1.5 V, after which the device currents begin rising up to the maximum 3 V. This indicates that the "SET" process is finished. The memristors continue to demonstrate a low-resistance state (LRS) in the second and third stages, when the scanning voltages decrease from 3 V to −3 V. In the fourth stage, the current progressively declines in accordance with changes in the scanning voltage from −3 V to 0 V. The memristor alters from LRS to HRS when the scanning voltage exceeds −1.5 V, thereby indicating completion of the "RESET" process.

The stability of the memristor can be examined by measuring the I–V curves for the 1^{st}, 10^{th}, 50^{th}, 200^{th}, and 500^{th} cycles, whereby the inset comprises the resistance variation curve under 0.5 V reading voltage for 10^5 seconds (**Fig. 3(b)**). It can be maintained the extensive overlap in the I–V curves and the resistance ratio that is present between the HRS and LRS, indicating that the fabricated memristor is sufficiently stable.

III. Circuit Design of Memristive Sequencer Network

A. The Architecture of Sequencer Network

According to [22], Visual Transformer (ViT) and its variants based on a self-attention module have proved effective in many computers vision tasks. Several works have tried to replace the self-attention module with other modules (e.g., the global filter) [23]. Following this trend, the sequencer network replaces the self-attention layer with bidirectional long short-term memory (BiLSTM). The specific structure of the sequencer network can be seen in **Fig. 4**.

The sequencer network can be divided into two parts: the sequencer block and the other necessary function modules (e.g., the layer normalisation module). Notably, the sequencer block is the basic component of the sequencer network and consists of two parts: a BiLSTM2D layer and a multi-layer perceptron.

The BiLSTM2D layer consists of a vertical BiLSTM layer and a horizontal BiLSTM layer, which can effectively be spatial and global information to memory. The mathematical expression of BiLSTM2D is given by:

$$\begin{cases} H_{vertical} = \mathrm{BiLSTM}(X_w) \\ H_{horizontal} = \mathrm{BiLSTM}(X_h) \end{cases} \tag{1}$$

$$BiLSTM\,2D = concatenate\left(H_{vertical}, H_{horizontal}\right) \tag{2}$$

where X_w and $X_h \in R^{H\times W\times C}$ are the input to the vertical BiLSTM layer and the horizontal BiLSTM layer, respectively; H and W denote the number of sequences in the vertical and horizontal directions, respectively; C represents the channel dimension; $H_{vertical}$ and $H_{horizontal} \in R^{H\times W\times 2D}$ are the output of the vertical

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BiLSTM layer and the horizontal BiLSTM layer, respectively; $D = C/4$ is the hidden dimension. BiLSTM(·) refers to the BiLSTM layer. It consists of two parallel LSTM layers: one takes the input in a forward direction (LSTM$_{forward}$), while the other takes it in a backward direction (LSTM$_{backward}$).

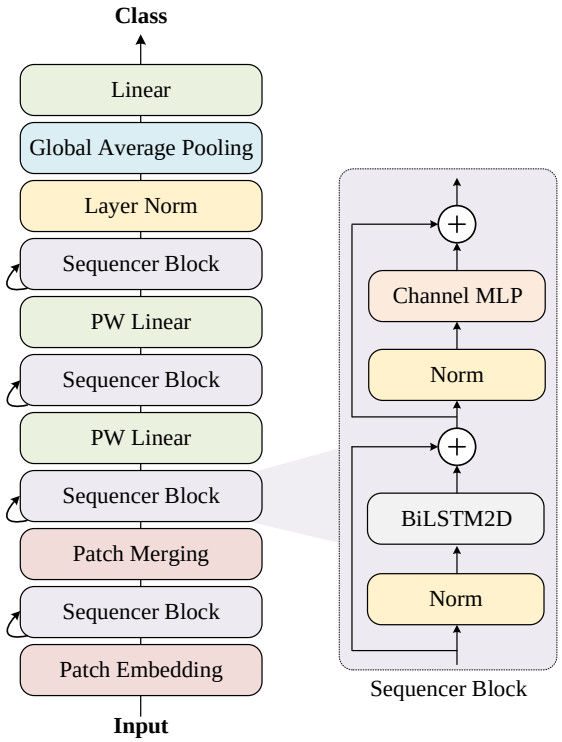

Fig. 4. The structure of sequencer network

Specifically, we assume $\vec{x}$ to be the input series, and $\overleftarrow{x}$ is the rearrangement of $\vec{x}$ in reverse order. Then, the outputs of these two LSTM layers can be written by:

$$\begin{cases} \vec{h}_{forward} = \mathrm{LSTM}_{forward}\left(\vec{x}\right) \\ \overleftarrow{h}_{backward} = \mathrm{LSTM}_{backward}\left(\overleftarrow{x}\right) \end{cases} \tag{3}$$

$$BiLSTM = \mathrm{concatenate}\left(\vec{h}_{forward}, \overleftarrow{h}_{backward}\right) \tag{4}$$

where LSTM(·) denoting the LSTM layer can be mathematically expressed by:

$$\begin{aligned} i_t &= \sigma\left(W_{x,i}x_t + W_{h,i}h_{t-1} + b_i\right) \\ f_t &= \sigma\left(W_{x,f}x_t + W_{h,f}h_{t-1} + b_f\right) \\ c_t &= f_t \odot c_{t-1} + i_t \odot \tanh\left(W_{x,c}x_t + W_{h,c}h_{t-1} + b_c\right) \\ o_t &= \sigma\left(W_{x,o}x_t + W_{h,o}h_{t-1} + b_o\right) \\ h_t &= o_t \odot \tanh\left(c_t\right) \end{aligned} \tag{5}$$

where i_t denotes the input gate that controls the storage of input x_t; f_t denotes the forget gate that controls the previous cell state c_{t-1}; o_t denotes the output gate that controls the cell output h_t from the current cell state c_t; σ and Θ are the logistic sigmoid and Hadamard product, respectively; weight matrixes W ($W_{x,i}$, $W_{x,f}$, $W_{x,c}$, $W_{x,o}$, $W_{h,i}$, $W_{h,f}$, $W_{h,c}$, $W_{h,o}$) are learnable parameters; and b (b_i, b_f, b_c, b_o) is the bias of LSTM.

The multi-layer perceptron consists of two-layer linear transformations with a ReLU activation function in between, it can be written by:

$$MLP\left(L_{o1}\right) = \max\left(L_{o1}W_1 + b_1\right)W_2 + b_2 \tag{6}$$

where $MLP(\cdot)$ denotes the multi-layer perceptron operation; L_{o1} is the input of the multi-layer perceptron; weight matrixes (W_1, W_2, b_1, b_2) are all learnable parameters.

The output of the last sequencer block is entered into the linear classifier by one-layer normalisation and a global average pooling layer.

B. Overall Circuit Architecture

The structure of the proposed EMSN with sequencer blocks and necessary function modules is illustrated in **Fig. 5**.

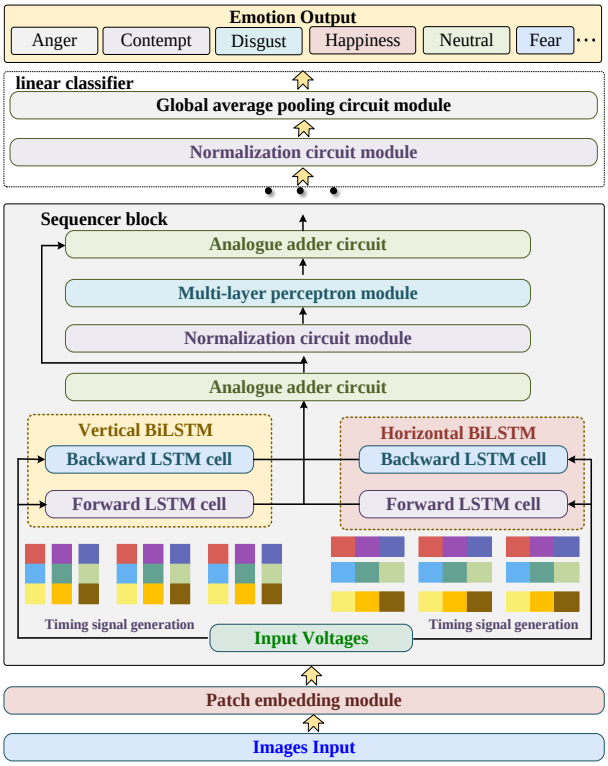

Fig. 5. The structure of the proposed EMSN

The sequencer block circuit is the fundamental element of EMSN, which consists of three modules: BiLSTM2D circuit module, normalisation circuit module, and multi-layer perceptron module. The necessary function modules contain three function circuits: patch embedding module, global average pooling circuit module, and timing signal generation module. Specifically, the input images are converted into voltage signals via a digital-to-analogue converter. Voltage signals are rearranged into voltage blocks by the patch embedding module, and each signal is controlled by a timing signal. The corresponding row signal can be applied to other modules when the efficacy of the timing signal is evident. Once the last sequencer block is calculated, the linear classifier will output a set of voltage signals.

C. Circuit Design of Sequencer Block

1) BiLSTM2D circuit module

According to (1) – (5), the LSTM cell is the key to realising the BiLSTM2D circuit module, which mainly consists of four LSTM units to generate i_t, f_t, o_t, and c_t. The LSTM cell is designed using the memristive synapse arrays and some peripheral circuits, as shown in **Fig. 6(a)**. Notably, the sneak

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path is a major obstacle to securing an increase in memristive synapse array size [24]. A potential approach is adopting selector, a type of nonlinear resistive device that conducts current only when the applied voltage exceeds a certain threshold (ON state); otherwise, selector allows little current to go through (OFF state) [25]. In this way, the memristive synapse arrays with the one-selector–one-Ag-Au/$MoSe_2$-doped Se/Au-Ag memristor (1S1M) configuration can conduct matrix-vector multiplication for each LSTM unit. The selector and memristor can be stacked on top of each other, giving a higher density potential than the one-transistor-one-memristor (1T1M) scheme. The input voltage $V_x^t(n)$ ($n\in[1, N]$) belongs to time step t, and the hidden state voltage $V_h^{t-1}(m)$ ($m\in[1, M]$) belongs to time step $t-1$. The V_{bi}, V_{bf}, V_{bc}, and V_{bo} are the bias voltages of the input gate, forget gate, previous cell state, and output gate, respectively.

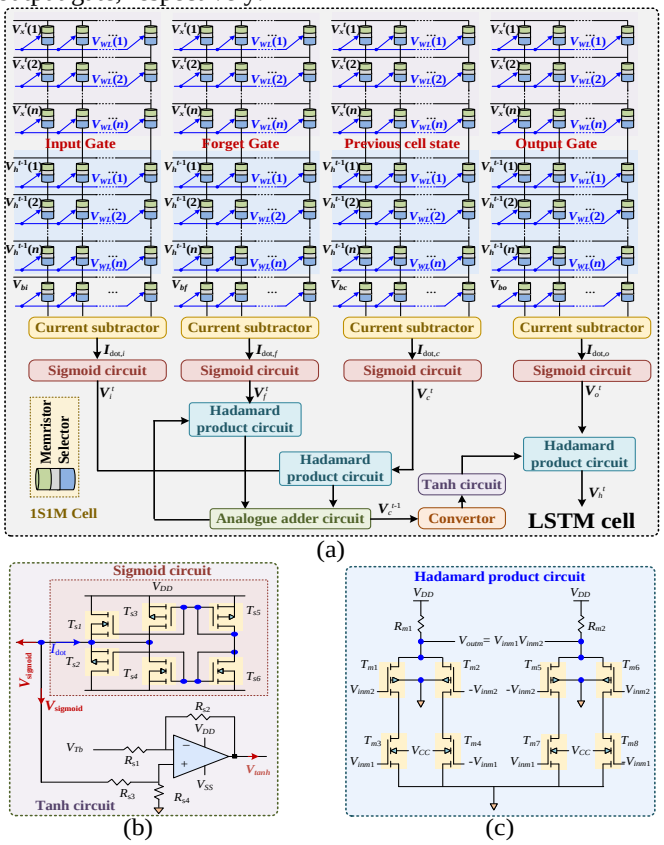

Fig. 6. Circuit design of BiLSTM2D circuit module (a) LSTM cell; (b) activation circuits; (c) Hadamard product circuit

In **Fig. 6(a)**, the weight of the LSTM unit is represented by the difference in conductance of two memristors in the memristive synapse array. The dot product currents I_{dot} from the current subtractors [26] are fetched into the corresponding activation circuit (i.e., sigmoid activation circuit and tanh activation circuit, labelled by the red/green rectangle in **Fig. 6(b)**). Specifically, the sigmoid activation circuit is composed of six transistors T_{s1}–T_{s6}. The output voltage $V_{sigmoid}$ and input current I_{dot} of the sigmoid activation circuit are located in the same node. Since the tanh function has the same shape as the sigmoid function, we use the output voltage of the sigmoid activation circuit as the input voltage of the tanh activation circuit that consists of an amplifier A_1 with four resistors R_{s1}–R_{s4}. Then, the output voltages V_i^t, V_f^t, V_o^t of the input gate, forget gate, and output gate can be produced from the activation circuits. Furthermore, the Hadamard product circuit is used to perform a pointwise operation, which consists of eight transistors T_{m1}–T_{m8} and two resistors R_{m1} and R_{m2}, as shown in **Fig. 6(c)**. V_{inm1} and V_{inm2} are the inputs of the Hadamard product circuit, and $V_{outm} = V_{inm1}\cdot V_{inm2}$ is the output of the Hadamard product circuit. Finally, the cell state voltage V_c^t and the cell output voltage V_h^t can be obtained after several steps of activation, multiplication, and summation, which are implemented by the activation circuit, Hadamard product circuit, and analogue adder circuit [26]. The calculation for V_i^t, V_f^t, V_o^t, V_c^t, V_h^t in **Fig. 6(a)** is provided below:

$$V_i^t = \sigma\left(\sum_{n=1}^{N}\left(G_{x,i}^{+}-G_{x,i}^{-}\right)V_x^t(n) + \sum_{m=1}^{M}\left(G_{h,i}^{+}-G_{h,i}^{-}\right)V_h^{t-1}(m) + I_{bi}\right)$$

$$V_f^t = \sigma\left(\sum_{n=1}^{N}\left(G_{x,f}^{+}-G_{x,f}^{-}\right)V_x^t(n) + \sum_{m=1}^{M}\left(G_{h,f}^{+}-G_{h,f}^{-}\right)V_h^{t-1}(m) + I_{bf}\right)$$

$$V_c^t = V_f^t \odot V_c^{t-1} + V_i^t \odot \tanh\left(\sum_{n=1}^{N}\left(G_{x,c}^{+}-G_{x,c}^{-}\right)V_x^t(n) + \sum_{m=1}^{M}\left(G_{h,c}^{+}-G_{h,c}^{-}\right)V_h^{t-1}(m) + I_{bc}\right) \quad (7)$$

$$V_o^t = \sigma\left(\sum_{n=1}^{N}\left(G_{x,o}^{+}-G_{x,o}^{-}\right)V_x^t(n) + \sum_{m=1}^{M}\left(G_{h,o}^{+}-G_{h,o}^{-}\right)V_h^{t-1}(m) + I_{bo}\right)$$

$$V_h^t = V_o^t \odot \tanh\left(V_c^t\right)$$

Based on this, the circuit design of BiLSTM2D can be obtained. It consists of four LSTM cells: backward LSTM cell in the vertical BiLSTM, forward LSTM cell in the vertical BiLSTM, backward LSTM cell in the horizontal BiLSTM, and forward LSTM cell in the horizontal BiLSTM.

2) Normalisation circuit module

The normalisation circuit module is composed of an inverting amplifier with two resistors R_{N2} and R_{N1}, two analogue switch circuits, and a voltage buffer circuit. The inverting amplifier can linearly generate a stable voltage. The analogue switch circuit is used as the comparator, and the specific circuit implementation is shown in **Fig. 7(a)**. The analogue switch circuit is connected to the voltage buffer to reduce the loading effect from the upper circuit into the output of the normalisation circuit. We can normalise the upper circuit output to the range of $-V_N$ to V_N using the normalisation circuit module.

3) Multi-layer perceptron module

The multi-layer perceptron module consists of two memristive synapse arrays with a ReLU activation circuit in between, labelled by the yellow rectangle in **Fig. 7(b)**. The memristive synapse array with the 1S1M configuration is responsible for the linear transformation. The ReLU activation circuit is composed of a current rectifier, a voltage follower, and an amplifier (labelled by the blue rectangle in **Fig. 7(b)**). The current rectifier provides a compact design to generate rectified

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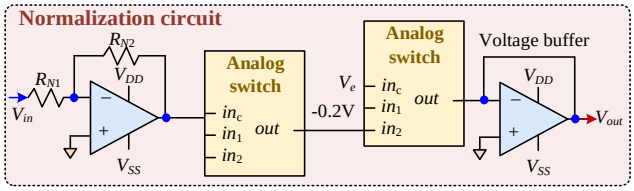
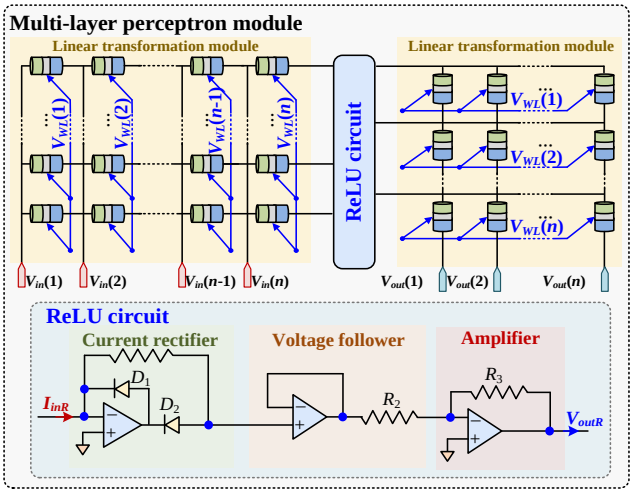
voltage V_{R1} from the input current I_{inR}. The voltage follower can generate a stable voltage V_{R2} and isolate the upper stage circuit. By setting the input resistance and feedback resistance of the amplifier, the required ReLU activation function can be obtained. The output voltage V_{outR} of the ReLU activation circuit is defined as:

$$V_{outR} = \begin{cases} \frac{R_1 R_3}{R_2} I_{inR}, I_{inR} \geq 0 \\ 0, I_{inR} < 0 \end{cases} \quad (8)$$



(a)



(b)

Fig. 7. Circuit design of peripheral circuits (a) normalisation circuit module; (b) multi-layer perceptron module

D. Circuit Design of Necessary Function Modules

1) Patch embedding module

Fig. 8(a) illustrates the structure of the patch embedding module, which consists of an input data control unit and static random-access memory groups. The input images from the datasets are converted to voltage signals by the digital-to-analogue converter and sent to the input data control unit that selects the required number of voltage signals. Then, the selected voltage signals are stored in the static random-access memory groups. Depending on the size of the input images, the patch embedding module selects a parallel or serial processing type and rearranges the voltage signals into blocks, followed by subsequent processing.

2) Global average pooling circuit module

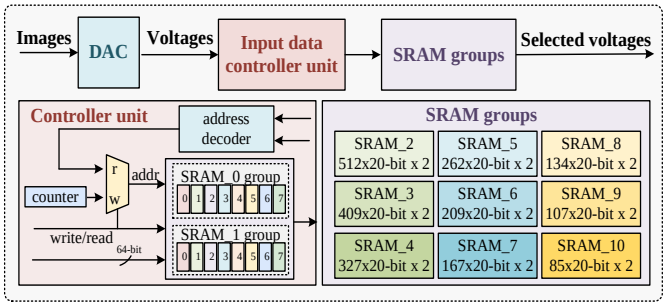
Global average pooling (GAP) involves a convolution operation in which the convolution kernel values are equal. In addition, the GAP is unique, whereas the window and feature map sizes are equal. Accordingly, it is possible to determine the GAP circuit design. Instead of adopting a memristive synapse array, this study employs a basic summing circuit, as shown in **Fig. 8(b)**. The formula presented below indicates the mathematical meaning of the entire circuit:

$$V_{GAP,out} = \sum_{j=1}^{N} \left(V_{GAP,in} \times R_{j,i} \right) / \sum_{j=1}^{N} R_{j,i}, j = 1,...,N \quad (9)$$

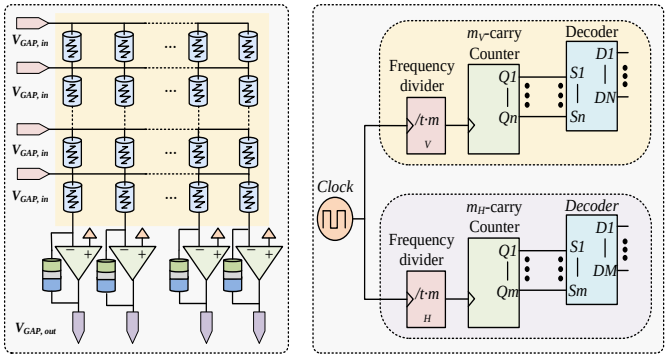
where $V_{GAP,in}$ and $V_{GAP,out}$ are the input voltage and output voltage of the GAP circuit module, respectively; and $R_{j,i}$ is the resistance in row j and column i.

3) Timing signal generation module

The proposed EMSN needs timing signals to schedule the input matrix and save the calculated results in sequence. The timing signal generation module is composed of a vertical timing generator and a horizontal timing generator, which exploits two sets of timing signals, the vertical timing signal *VLs* and the horizontal timing signal *HLs*, as shown in **Fig. 8(c)**. The number of channels is m_V and m_H, respectively. For the *VLs* (*HLs*) signals, the clock frequency is reduced by m_V (m_H) × t times by the frequency divider. Then, the output signals are counted by the m_V (m_H) counter. Finally, the decoder decodes the counting result into timing signals.



(a)



(b) (c)

Fig. 8. Circuit design of necessary Function Modules (a) patch embedding module; (b) global average pooling circuit module; (c) timing signal generation module

The necessary circuit parameter settings of the proposed EMSN are provided in Table I.

TABLE I
THE NECESSARY CIRCUIT PARAMETERS SETTING

Parameters	Values	Parameters	Values	Parameters	Values
T_{s1}	20μ/0.18μ	T_{m8}	2μ/0.22μ	R_{s4}	1kΩ
T_{s2}	20μ/0.18μ	T_{N1}	3μ/0.18μ	R_{N1}	1kΩ
T_{s3}	19μ/0.18μ	T_{N2}	30μ/0.18μ	R_{N2}	1kΩ
T_{s4}	18μ/0.18μ	T_{N3}	36μ/0.18μ	R_{N3}	10kΩ
T_{s5}	20μ/0.18μ	T_{N4}	36μ/0.18μ	R_{r1}	10kΩ
T_{s6}	20μ/0.18μ	T_{N5}	6μ/0.18μ	R_{r2}	10kΩ
T_{m1}	1.6μ/0.3μ	T_{N6}	6μ/0.18μ	R_{r3}	1kΩ
T_{m2}	1.6μ/0.3μ	T_{N7}	45μ/0.3μ	V_{Tb}	0.5V
T_{m3}	2μ/0.22μ	T_{N8}	18μ/0.3μ	V_{DD}	1.8V
T_{m4}	2μ/0.22μ	T_{N9}	18μ/0.3μ	V_S	-1.8V
T_{m5}	1.6μ/0.3μ	R_{s1}	1kΩ	C_N	1pF
T_{m6}	1.6μ/0.3μ	R_{s2}	1.7kΩ	$R_{j,i}$	1kΩ
T_{m7}	2μ/0.22μ	R_{s3}	1kΩ	-	-

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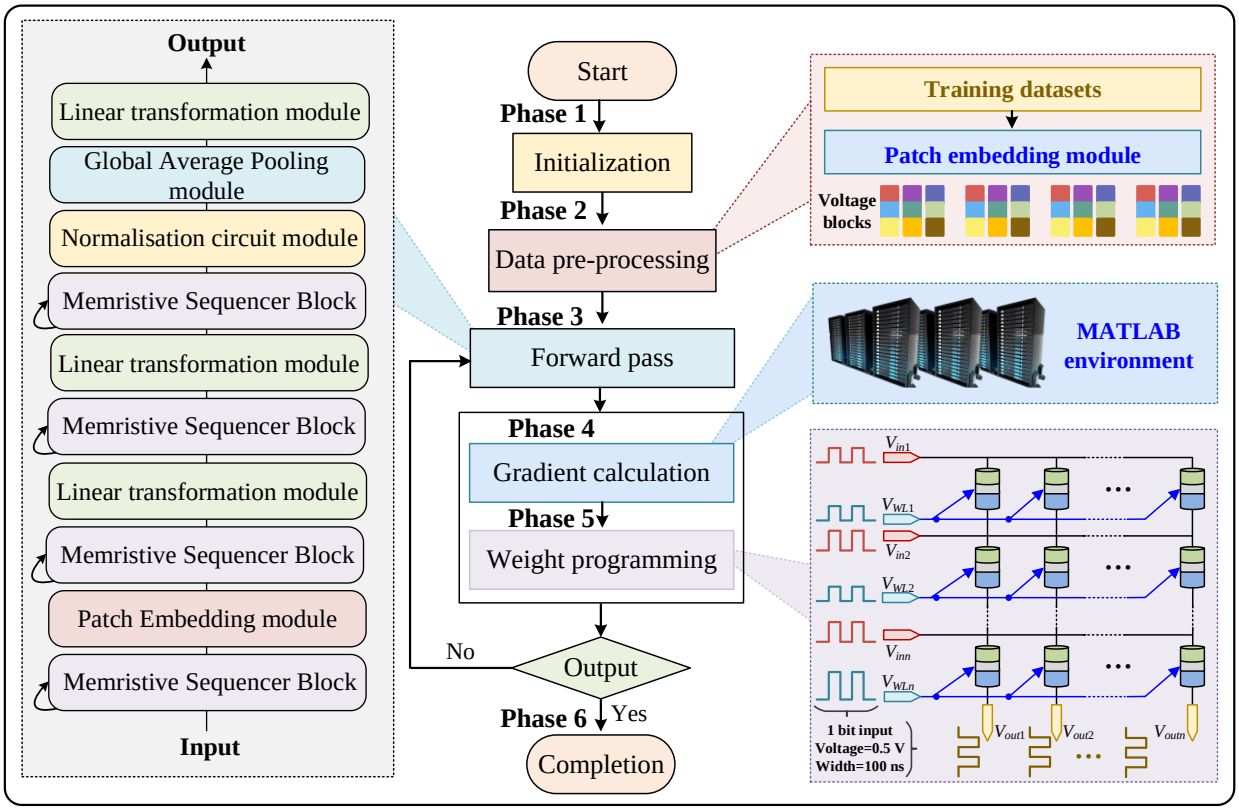

Fig. 9. The flow chart of hardware friendly training phase

IV. Application in Human Emotion Classification

Facial expression plays an important role in daily life, enabling the mental health state of an individual to be conveyed and inferred. In this section, the proposed EMSN is applied to human emotion classification to provide an efficient and fast solution for health monitoring and disease management. To verify the feasibility and effectiveness of the proposed system, a series of experiments are carried out by comparing the proposed system with competitors.

A. Database and Evaluation Metrics

The proposed system is evaluated on two human emotion classification datasets: the FER2013 dataset and the extended Cohn–Kanade dataset (CK+) [27]. The FER2013 dataset is a large-scale and unconstrained database, which comprises 35,887 greyscale face images of size 48 48. Following previous works, 3,589 samples are distributed in a validation dataset, 3,589 in a testing dataset, and the remaining 28,709 in a training dataset. Each face has one of seven emotion labels: “angry”, “disgust”, “fear”, “happy”, “sad”, “surprised” and “neutral”. The CK+ dataset consists of 593 video sequences from 123 subjects. Each video sequence in CK+ dataset has segmented from neutral frame to peak frame of facial expressions about 10-60 frames. The last frame of each sequence is labelled with one of seven expressions (“angry”, “disgust”, “fear”, “happy”, “sad”, “surprised” and “neutral”). To collect sufficient images for training, we extract the neutral frames and the final three frames with peak formation from the labelled sequence to generate 1,236 expression images. Following previous works, 309 samples in a testing dataset, and the remaining 927 in a training dataset. Then, the common performance metric of average accuracy is used to evaluate the overall performance.

B. Hardware Friendly Training Method

The neural network is trained, and the entire process can be divided into two parts: the feedforward computation and back propagation. The feedforward computation is carried out in the proposed EMSN; the back propagation (mainly referring to the weight updating) is performed in MATLAB 2018b. The specific training method with six phases is illustrated in **Fig. 9**.

Phase 1. Initialisation: At the beginning, the conductances of all Ag-Au/$MoSe_2$-doped Se/Au-Ag memristors in the 1S1M array are initialised to an appropriate value by setting the voltage across the memristors.

Phase 2. Data pre-processing: The input images from the training datasets are converted to voltage blocks within the range of [−3, 3] via the patch embedding module.

Phase 3. Forward pass: The voltage blocks are injected into the proposed EMSN, after which the corresponding output voltage can be achieved.

Phase 4. Error backpropagation: The error backpropagation through the stochastic gradient descent approach by a factor of 10^{-4} is adopted to compute the intended conductance update values. This is performed in the MATLAB environment (R2018b).

Phase 5. Weight update: The conductance is updated on a row-by-row or column-by-column basis, as proposed in [28]. Evidence exists of the effectiveness of the two-pulse scheme as

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a means of realising linear and symmetric memristor conductance updates.

Phase 6. Completion: after the entire EMSN settles, the training process is completed; otherwise, return to **Phase 3**.

This hardware friendly training method combines the advantages of the energy efficiency of the 1S1M synapse array in performing the analogue MAC operation and the digital logic for realising the rest of the training process.

C. Human Emotion Classification Results and Analysis

The proposed EMSN is used to demonstrate human emotion classification. **Fig. 10** illustrates the circuit progresses of the training and testing processes when identifying the expressions of emotion of the FER2013 dataset and the CK+ dataset. The corresponding output voltage can be achieved with seven states (assigned to corresponding emotion expressions), as shown in **Fig. 10(a)** and **Fig. 10(b)**. Once the training process is completed, the classifier will output a set of voltage signals representing a probability distribution. The classification result is determined by the largest output voltage in each period.

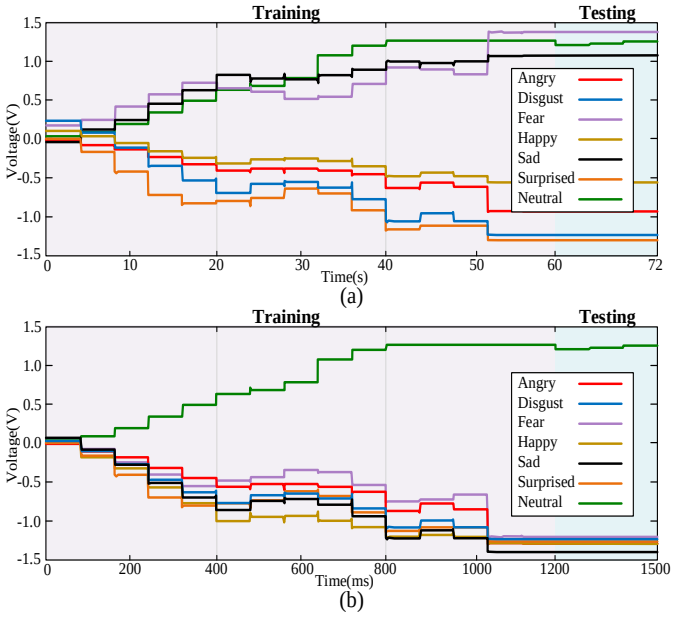

Fig. 10. The corresponding results obtained by the proposed EMSN (a) FER2013 dataset; (b) CK+ dataset

The proposed EMSN is compared with the state-of-the-art methods on the FER2013 dataset and the CK+ dataset, as shown in Table II.

TABLE II
COMPARISON OF DIFFERENT STATE-OF-THE-ART METHODS IN HUMAN EMOTION CLASSIFICATION

References	FER2013		CK+	
	Acc.	Time	Acc.	Time
[29]	70.19	457.52	94.47	160.37_2
[30]	73.96	502.77	97.10	221.22
[31]	72.47	$\mathbf{389.23_2}$	97.83	178.29
[32]	72.36	$\mathbf{455.16_3}$	97.35	202.53
[33]	$\mathbf{74.98_2}$	524.76	98.89_3	193.86
[34]	$\mathbf{84.30_1}$	523.82	$\mathbf{99.30_1}$	164.52_3
[35]	74.09	495.38	-	192.33
[36]	74.21	535.43	97.72	220.84
This work	$\mathbf{74.66_3}$	$\mathbf{28.42_1}$	$\mathbf{98.91_2}$	$\mathbf{13.92_1}$

Note: the subscript 1, 2, 3 represent the corresponding ranking results.

From Table II, the proposed network ranks in the top three on the FER2013 dataset and slightly outperforms other competitors [29-32, 35, 36]. On the CK+ dataset, it outperforms state-of-the-art methods in the human emotion classification task [29-33, 35, 36]. Meanwhile, [33, 34] are slightly superior to the proposed method in terms of accuracy, while inferior to time consumption. The results demonstrate that the trade-off between the accuracy and time consumption can be well balanced in the proposed memristive sequencer network. **Fig. 11** shows the confusion matrixes of the proposed EMSN on the FER2013 testing dataset and the CK+ testing dataset. As shown in **Fig. 11,** the "sad" emotion expression is confused with the "neutral" emotion for the FER2013 dataset. The most difficult expression of emotion is "fear", which has the lowest recognition rates for both the CK+ and FER2013 datasets. Although the training data are unbalanced, the proposed network overcomes this problem and improves the overall performance.

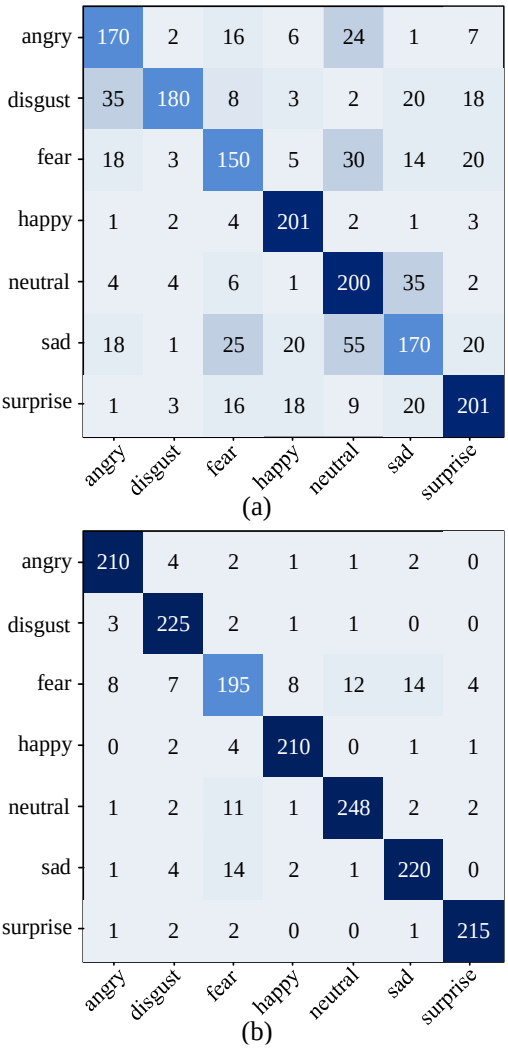

Fig. 11. Confusion matrix (a) FER2013 dataset; (b) CK+ dataset

D. Computational Efficiency

Due to the speed advantage of the hardware implementation of the sequencer network, the proposed system has benefits in computational efficiency in terms of time, power. The time consumption of the proposed EMSN is analysed by comparing

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it with a competitor on the FER2013 dataset and the CK+ dataset, as shown in **Fig. 12**. The proposed network is faster (approximately 10–20 times) than other software-based neural networks. The explanation for this difference may be that parallel-computing via 1S1M memristive synapse arrays is more efficient.

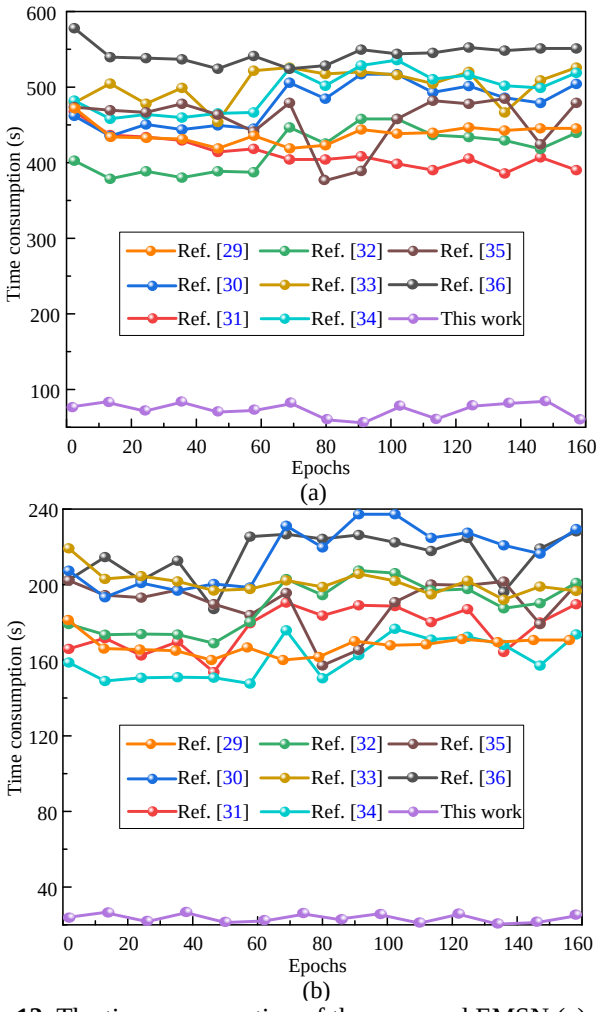

Fig. 12. The time consumption of the proposed EMSN (a) FER2013 dataset; (b) CK+ dataset

TABLE III
THE ENERGY CONSUMPTION OF EMSN

Module	Power consumption/pJ
BiLSTM2D circuit module	226.73
Normalization circuit module	27.22
Multi-layer perceptron module	78.22
Patch embedding module	327.45
Global average pooling circuit module	10.66
Timing signal generation module	11.27
Total	2057.98

Table III presents the energy consumption for each circuit module and the entire circuit. The energy consumption for 1-bit computing is 2,057.98 pJ, and the power consumption for 1-bit computing is 20.58 mW with 0.5 V and 100 ns read voltage. The circuit is executed using 180-nm CMOS technology, and the total area of the proposed system is approximately 48.63 μm^2. In addition, the benefits of the proposed network include time, power, and area advantages. These are indicative of the cost-saving and energy-efficient character of the proposed system.

E. Robustness Analysis

For practical applications, it is necessary to analyse the robustness of the proposed EMSN for human emotion.

1) Anti-noise analysis

Considering that the standard deviation of reading and writing noise may be inevitable in signal transmission and processing, we added reading and writing noise to the proposed network. The human emotion classification accuracy is demonstrated in **Fig. 13(a)**. When the standard deviation of reading and writing noise is over 20%, the classification accuracy can be kept over 70% and 90% on the FER2013 dataset and CK+ dataset, respectively. The experiment results demonstrate that the proposed network has good anti-noise ability.

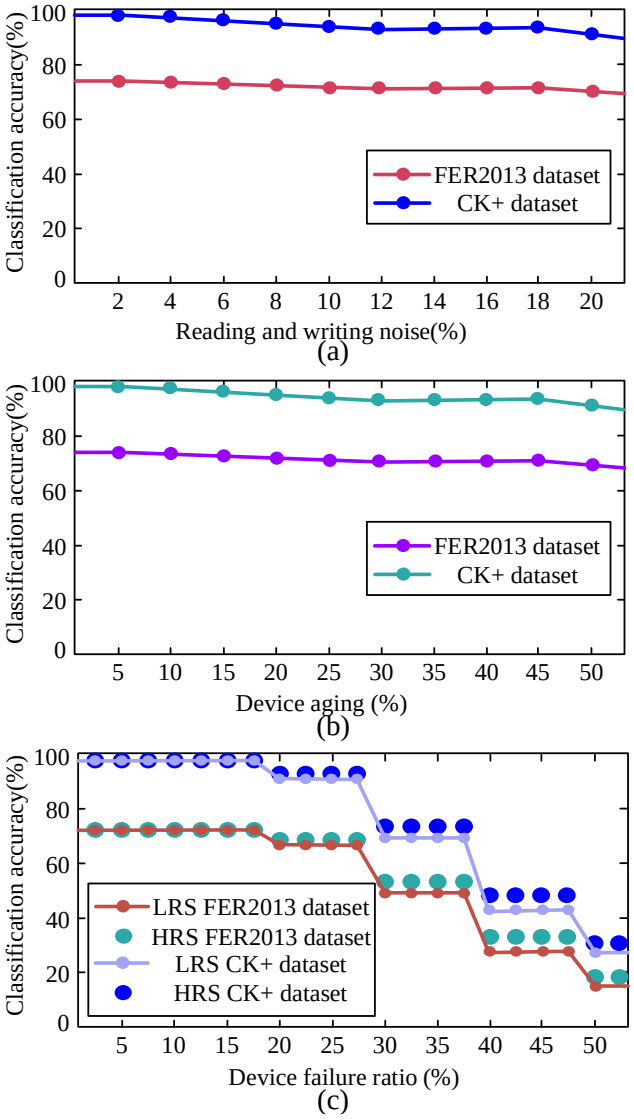

Fig. 13. Robustness Analysis of the proposed EMSN (a) anti-noise analysis; (b) device aging analysis; (c) device failure analysis

2) Device aging and failure analysis

Device aging or failure may lead to the conductance drifting or deviating from the correct state [37]. As shown in **Fig. 13(b)**, when the percentage of aging reaches about 50%, the classification accuracy can be kept over 70% and 90% on the

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FER2013 dataset and CK+ dataset, respectively. The experiment result illustrates that device aging does not affect the classification accuracy of the proposed system. The effect of device failure on the classification accuracy of the proposed network is illustrated in **Fig. 13(c)**. When the memristor is in LRS/HRS and the failure ratio reaches about 25%, the classification accuracy can be maintained at an acceptable level (over 67% and 88% on the FER2013 dataset and CK+ dataset, respectively). Once the memristor failure ratio exceeds 30%, the accuracy decreases sharply to about 20%. Thus, the experiment shows that the proposed EMSN can tolerate up to 25% failed devices within the architecture.

The reason maybe that the adjustment of the network weight is rather an overall value of 1S1M synapse array than an exact value of each memristor. Therefore, the performance of the proposed network will not be strongly affected by reading and writing noise, device aging, and device failure.

V. Conclusion

In this work, we investigate an energy-efficiency memristive sequencer network. Firstly, a kind of eco-friendly memristor is fabricated using 2D materials, and the corresponding testing performance is conducted to make sure its efficiency and stability. Then, the memristor-based sequencer block consisting of BiLSTM2D circuit module, normalization circuit module, and multi-layer perceptron module is proposed. Based on this, the circuit design of the proposed EMSN can be achieved after combining some other necessary function circuit modules (i.e., patch embedding module, global average pooling circuit module, and timing signal generation module). Furthermore, the proposed EMSN is applied for human emotion classification. The experimental results demonstrate the good performance of the proposed EMSN, especially in classification accuracy, computational efficiency, and robustness. This work provides a new way to achieve the deep integration of multimedia processing and neuromorphic computing, which is expected to promote the development of consumer electronics applications.

Notably, the energy-efficient memristive sequencer network is still in an infancy stage with abundant opportunities and challenges. To further develop and apply this work into the real life, several aspects can be considered in future research: At the algorithmic level, the main training process in this work is completed via software platform. The desired memristive conductance obtained by MATLAB environment (R2018b) is directly mapped to the proposed network without read or write to memristive synapse array. Thus, the general learning circuit module will be designed to perform back-propagation operation. At system level, the human perception function is not considered in this work, the perception data directly comes from existing human emotion classification datasets. This work will be extended to integrate the brain-inspired approach, wearable technology, and nanotechnology for consumer health monitoring. Specifically, the brain-inspired system for sensing and processing multimodal information in real-time manner will be developed. The entire system is expected to be integrated into a wearable device for consumer health monitoring.

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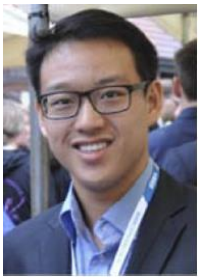

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