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Design and Implementation of a Flexible Neuromorphic Computing System for Affective Communication via Memristive Circuits

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***Abstract*—Neuromorphic computing is expected to realize fast and energy-efficient artificial neural networks and address the inherent limitations of von Neumann architectures in dedicated communication applications. To realize this vision, we identify the existing challenges in neuromorphic computing and provide a specific solution from the perspectives of device, circuit, and system. At the device level, we fabricate a metal oxide-based memristor with high stability, low power, and good scalability, serving as the fundamental component of neuromorphic computing system. At the circuit level, the basic circuit units and necessary peripheral circuits are designed to realize efficient vector-matrix multiplication and different functions, including nonlinear activation operation, subtraction operation, added operation, etc. At the system level, a flexible neuromorphic computing system with a hardware-friendly training approach is proposed, it can perform affective communication with good trade-off between accuracy and time consumption. This study is expected to achieve the deep integration of nanotechnology, energy-efficient integrated circuits, and neuromorphic computing systems into communication applications.**

***Index Terms*—Metal oxide-based memristor, basic circuit units, neuromorphic computing system, affective communication**

I. INTRODUCTION

Neuromorphic computing is a computing paradigm inspired by biological brain, which enables fast and energy-efficient Artificial Neural Network (ANN) hardware implementation for highly sophisticated tasks [1]. Notably, neuromorphic computing system shows the ability to cache countless amounts of data and constantly conduct computing, offering promising solutions to break the von Neumann bottleneck, which are attracting increasing interest in recent years [2]. So far, a number of neuromorphic computing systems have been proposed using different electronics devices, such as spintronic devices, ferroelectric devices, complementary, phase-change memory devices, etc. [3]. Memristors are two-terminal electronic devices that exhibit non-volatility, high density, long retention, and long endurance, which are potential candidates for neuromorphic computing [4]. Recently, memristor-based neuromorphic computing systems with different learning algorithms have been developed to realize specialized neural networks, such as Long Short-term Memory (LSTM) networks, Spiking Neural Networks (SNNs), Convolutional Neural Networks (CNNs), which can be extended to realize a variety of applications e.g., affective communication. In [5], a LSTM network was fabricated using memristor crossbar arrays, which can store a large number of parameters and offer in-memory computing capability. In [6], a high-performance and uniform memristor crossbar array was fabricated for the implementation of CNN with parallel-computing capability. [7] presented a hardware design of ANN based on memristor crossbar array. The whole circuit system can be used to complete the sentiment analysis task with high accuracy and low power consumption. In [8], a bionic memristive system with the functions of emotional learning and generation was constructed, which can perform affective computing based on multimodal information. [9] presented a multimodal neuromorphic sensory-processing system via memristor circuits, offering an environmentally friendly method with easily deployable hardware.

Despite these advantages, the existing memristor-based neuromorphic computing systems still suffer from several limitations. The key challenges can be identified from the perspectives of device, circuit, and system. At the device level, due to the non-uniformity of the function layers and electrodes, the device-to-device and cycle-to-cycle performances have shown some variations, which may lead to the imprecise encoding of network weights in the neuromorphic computing. At the circuit level, the general basic circuit units are still lacking, which makes the existing neuromorphic computing systems are intensive and non-configurable. Considering the diversity of neural networks, the universality and flexibility of neuromorphic computing systems are hard to guarantee, which may lead to additional resource consumption. At the system level, most neuromorphic computing systems do not provide the complete circuit design, and the training process always relies on some computer/software aided strategies. In addition, the traded-off between testing accuracy and time consumption is hard to balance.

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Citation information: DOI10.1109/MCOM.001.2200272,

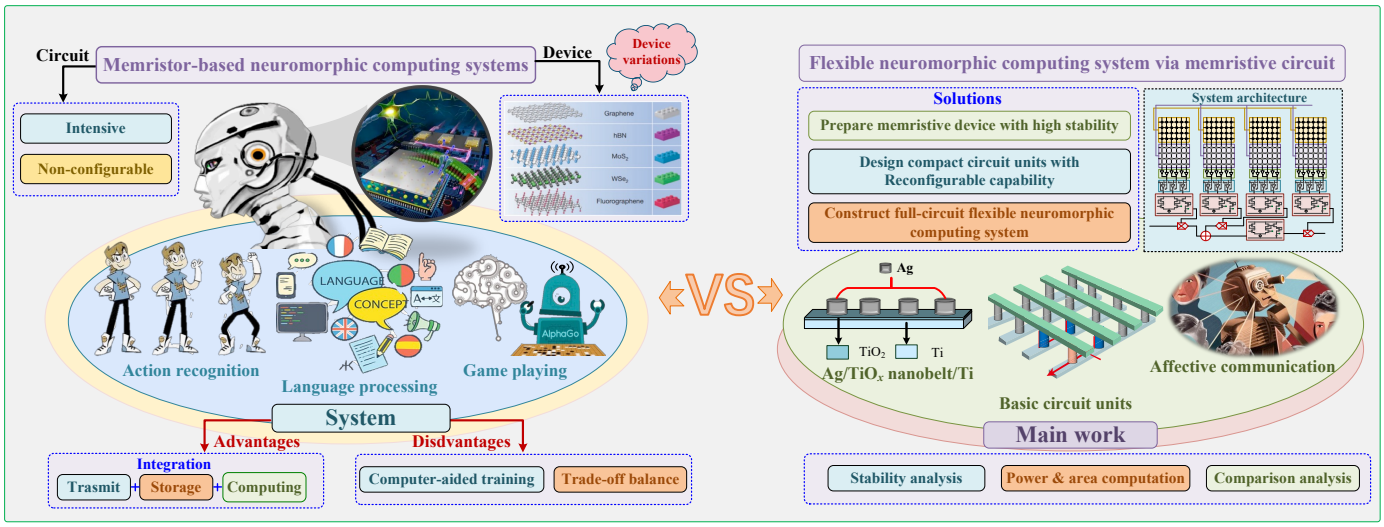

Fig. 1 Memristor-based neuromorphic computing system architecture.

To address these common issues, the potential remedies are provided below: From the perspective of the device, since the device stability is critical to the neuromorphic computing accuracy, the highly reliable dynamic memristive devices are required. From the perspective of the circuit, since the general basic circuit units are important for the construction of flexible neuromorphic computing systems, compact basic circuit units with reconfigurable capability are required. From the perspective of the system, efforts are needed to develop hardware-friendly training algorithms that can realize a compact, high-accuracy, and energy-efficient neuromorphic computing system. For clarity, the drawbacks of the existing memristor-based neuromorphic systems and the corresponding solutions are provided in Fig. 1.

Based on this, we explore and propose a flexible and energy-efficient neuromorphic computing system for affective communication. The main contributions brought about in this work are the following:

1) A metal oxide-based memristor with high stability, low power, and good scalability is prepared. It can serve as a promising candidate to emulate high-accuracy neuromorphic computing in communication technology.

2) A flexible neuromorphic computing system based on general basic circuit units and necessary peripheral circuits is proposed, which aims at solving computationally hard problems with configuration and universality unattainable.

3) Based on the proposed neuromorphic computing system, a full hardware implementation of affective communication is developed, which provides a success case study for balancing the trade-off between accuracy and time consumption. Importantly, we also discuss the future direction of neuromorphic computing using advanced manufacturing and integration technologies.

II. Memristor Fabrication and Testing

A. Fabrication of Ag/TiO$_x$ nanobelt/Ti Memristor

Metal oxide materials offer an attractive option for the fabrication of relatively inexpensive neuromorphic devices with low-energy switching and high stability [10]. In this paper, the Ag/TiO$_x$ nanobelt/Ti memristor is prepared based on hydrothermal synthesis method and magnetron sputtering method, in which the former is used to prepare TiO$_x$ nanobelt and the latter is used to prepare Ag electrodes.

Step 1: deionized water and ethyl alcohol are employed to clean the surface of the Ti substrate for 3 seconds.

Step 2: the Ti substrate is transferred to a muffle furnace and annealed at 200 °C for 3 hours.

Step 3: 2.0g NaOH is dissolved in 20mL deionized water, stirred for 30 minutes at room temperature until it is completely dissolved.

Step 4: 2.0g TiO$_2$ powder is dispersed in prepared NaOH solution, and then continuously stirred by a magnetic stirrer for 3 hours to fabricate the precursor.

Step 5: the mixed precursor is transferred to a 50mL hydrothermal reactor. At the same time, a heat-treated Ti substrate is inserted into the hydrothermal reactor.

Step 6: after hydrothermal reaction at 200℃ for 48 hours, a blue-gray film is grown on the surface of the Ti substrate.

Step 7: the TiO$_x$ nanobelt arrays can be obtained by cleaning the bluish-gray film with 10% hydrochloric acid for 90 seconds and deionized water for 10 minutes.

Step 8: the TiO$_x$ nanobelt samples are thermally processed at 80°C for 24 hours to remove possible residual HCL.

Step 9: the relative humidity is controlled at the range of 95%~100%. Magnetron sputtering is used to fabricate Ag electrodes on the TiO$_x$ nanobelt. Then, the Ag/TiO$_x$ nanobelt/Ti memristor is achieved.

B. Performance Testing

Since the non-uniformity of the function layers and electrodes may lead to the imprecise encoding of network weights in the neuromorphic computing, it is necessary to investigate the stability of the Ag/TiO$_x$ nanobelt/Ti memristor through an electrochemical workstation (CHI-660D). The electrical characteristics, mainly referring to the ampere-volt data is measured (at ± 6V scanning voltages), as shown in Fig. 2.

From Fig. 2, the I–V sweep curves obtained by 140

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Citation information: DOI10.1109/MCOM.001.2200272,

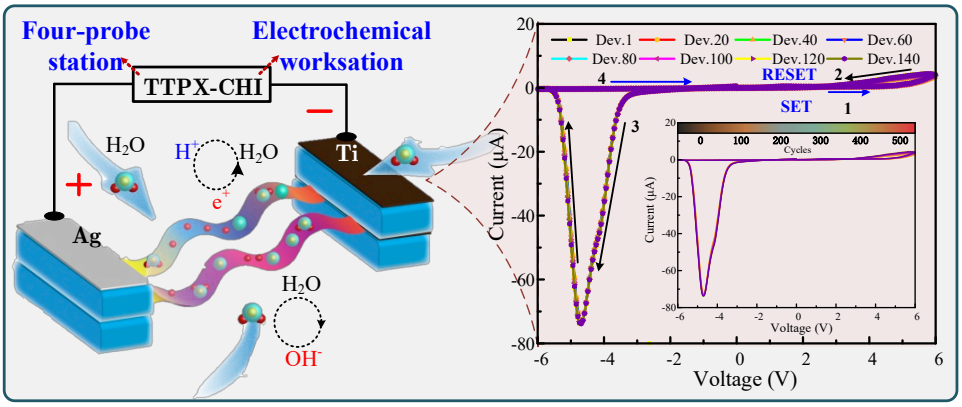

Fig. 2 Performance testing of Ag/TiO_x nanobelt/Ti memristor.

memristors show high degree of overlap, demonstrating that the Ag/TiO_x nanobelt/Ti memristor has good device-to-device stability. Meanwhile, the prepared memristor also exhibits resistive switching behavior. Specifically, in stage 1, the memristor keeps in the High Resistance State (HRS). As the scanning voltage increases from 0V to 3V, there is very little change in the device current until the applied voltage exceeds 3V, the current starts to increase with the scanning voltage and reaches a maximum, meaning that the memristor changes from HRS to Low Resistance State (LRS) , and the "SET" process is completed; in stage 2, when the scanning voltage decreases from 3V to 0V, the memristor remains in LRS; in stage 3, memristor remains in LRS as the scanning voltage is reversed from 0V to -3V; in stage 4, the current gradually decreases as the scanning voltage changes from -3V to 0V. When the scanning voltage is higher than -3V, the memristor changes from LRS to HRS, meaning that the "RESET" process is completed. Furthermore, 500 highly overlapped I–V profiles are observed in the inset of Fig. 2, indicating that the Ag/TiO_x nanobelt/Ti memristor has excellent cycle-to-cycle stability.

III. Flexible Circuit Design Scheme for Neuromorphic Computing System

Neuromorphic computing is one of the potential candidates to understand neuronal communications and functionalities, enabling specialized ANN hardware implementation. Our motivation is to design a flexible neuromorphic computing system via memristive circuits, aimed at solving computationally hard problems with configuration and universality unattainable. Take LSTM network as an example, we presented two basic circuit units and used a hardware-friendly training approach, which can perform the standard LSTM network and its eight variants with less total area and power consumption.

A. Basic Circuit Units

A typical LSTM cell contains three gates, i.e., the forget gate, the input gate, and the output gate, as shown in Fig. 3. Specifically, x_t is the input vector at the present step, h_t and h_{t-1} are the output vectors at the present and previous time steps, respectively. σ is the logistic sigmoid function, which yields i_t, f_t, and o_t for the input gate, forget gate, and output gate. c_t denotes the cell state. Weights $\boldsymbol{W}$, recurrent weights $\boldsymbol{U}$, and bias $\boldsymbol{b}$ are all network parameters for the implementation of cell activation and each gate.

The LSTM cell can be characterized by two main phases, i.e., the linear matrix operation and the gated nonlinear activation. Correspondingly, the specific hardware implementation of neuromorphic computing system with LSTM framework can also be separated into two basic circuit units, i.e., the linear matrix operation circuit and nonlinear activation circuit, using 2-μm Complementary Metal-Oxide-Semiconductor (CMOS) technology.

The linear matrix operation circuit: the memristor crossbar array, biasing circuit, and the auxiliary circuit jointly constitute the linear matrix operation circuit. Notably, the memristor crossbar array (labeled by the orange/purple rectangle in Fig. 3) is responsible for matrix-vector multiplication. The memristors installed at the crossbar array intersection are represented by their conductance $G_{w,ij}$ and $G_{u,ij}$. Notably, weights $\boldsymbol{W}$ and recurrent weights $\boldsymbol{U}$ can be calculated by the difference of the conductance.

$R_{a1, a2, a3, a4}$ and $R_{b1, b2, b3, b4, b5)}$ are regular resistors in auxiliary circuit and biasing circuit, respectively. V_b is the additional input of the biasing circuit (labeled by the blue rectangle in Fig. 3), representing the bias parameter in LSTM. The output V_{ob} can be achieved by the linear matrix operation.

The nonlinear activation circuit: an appropriate design scheme for the nonlinear activation function in LSTM is presented in Fig. 3 (labeled by the red rectangle). The voltage V_{ob} is interconnected to one side of an N-Metal-Oxide-Semiconductor (NMOS) source-coupled pair, biased with a current sink $I_{\max}$. The output current I_{out} can be achieved by the production of the current sink $I_{\max}$ and the normalized current I_n. According to Ohm's law, the output voltage V_{out} can be obtained. Notably, the proposed circuit is a general activation circuit, which can realize almost all the activation functions by tuning circuit parameters.

B. Hardware-friendly Training Method

The specific hardware-friendly training method with six phases is illustrated below:

Phase 1. Initialization: mainly aims at the memristor crossbar array and the voltage $V_{h,t}$. At the beginning of the training, the resistances of all the electronic devices installed at the intersections of the crossbar array can be initialized to an intermediate value between LRS and HRS. The voltage $V_{h,t}$ can be initialized to random value within the range of [0, 1].

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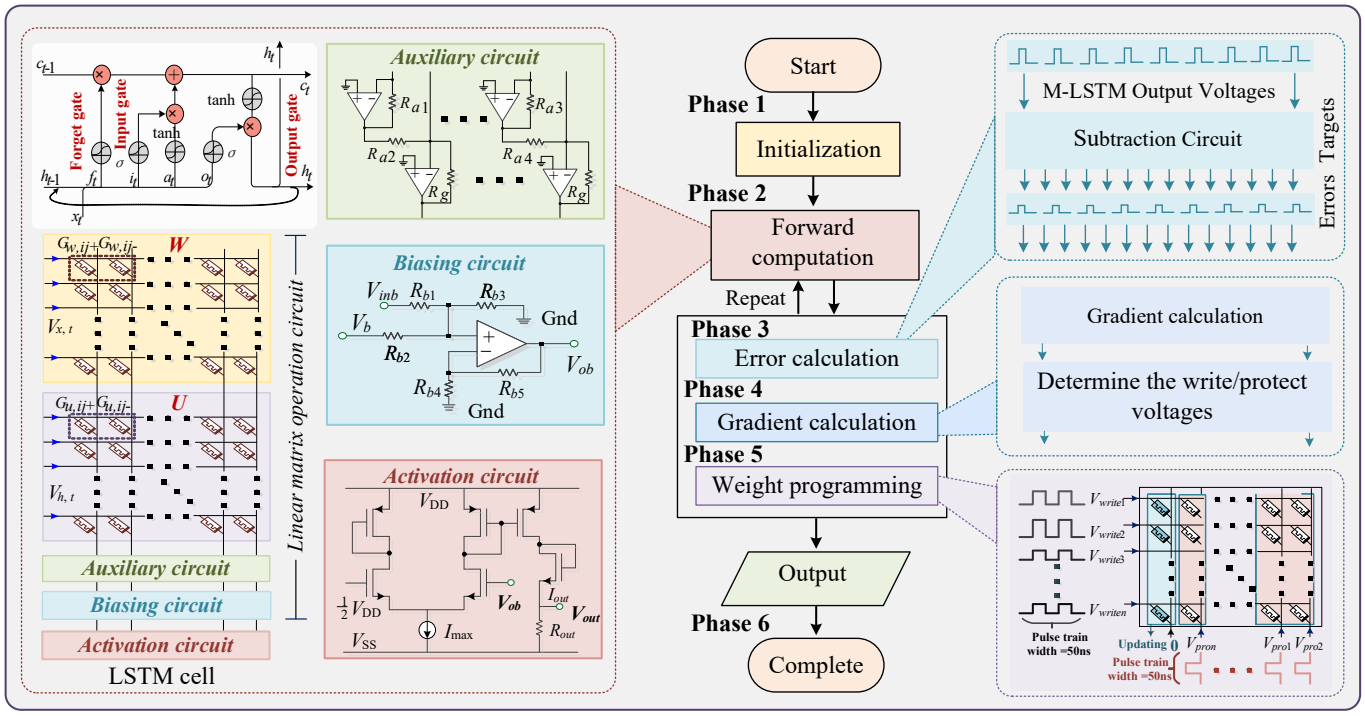

Fig. 3 Hardware-friendly training scheme for neuromorphic computing system with LSTM framework.

Phase 2. Forward computation: the voltages $V_{x,t}$, $V_{h,t}$ and $V_{b,t}$ are injected to the LSTM cell, the vectors a_t, i_t, f_t, and o_t can be achieved. Then, the elements in vectors a_t, i_t, f_t, o_t, and c_{t-1} are jointly used to calculate the new vector $V_{h,t}$.

Phase 3. Error calculation: according to the subtraction circuit [11], the errors between outputs and targets can be obtained.

Phase 4. Gradient calculation: the obtained errors are applied into the gradient calculation circuit [11], the desired weights can be obtained immediately.

Phase 5. Weight programming: we adjust write voltage V_{write} and protect voltage V_{pro} in crossbar array, offering controllability in weight programming. Specifically, when the desired weights are obtained, the expected conductance and the relevant write voltage V_{write} can be calculated and applied to the corresponding row of the target memristor pair with a pulse width of 50ns. At the same time, the remaining memristors are kept unchanged under a protect voltage V_{pro}. The corresponding conductance will change to the desired value within a short time, and the weight programming is completed.

Phase 6. Completion: until the entire neuromorphic computing system settles, the training process is finished, otherwise, return to the **Phase 2**.

Actually, the energy-efficient hardware implementation of training methods is complex and challengeable, especially when the inevitable variations occur in the interconnected analog circuit components. Compared with the conventional memristor-based neuromorphic computing that always use a computer/software aided method to perform the weight updating, all the computations can be completely realized by hardware circuit in this work, which offers benefits in terms of communication overhead, convergence speed, and power consumption.

C. *Flexible Design Scheme*

Different with the existing memristor-based neuromorphic computing systems, the proposed two basic circuit units and hardware-friendly training method can not only be used to construct the standard LSTM network, but also be extended to the implementation of its variants, including No Forget Gate (NFG), No Input Gate (NIG), No Output Gate (NOG), No Input Activation Function (NIAF), No Output Activation Function (NOAF), Gated Recurrent Unit (GRU), Peephole LSTM, and ConvLSTM, as demonstrated in Fig. 4.

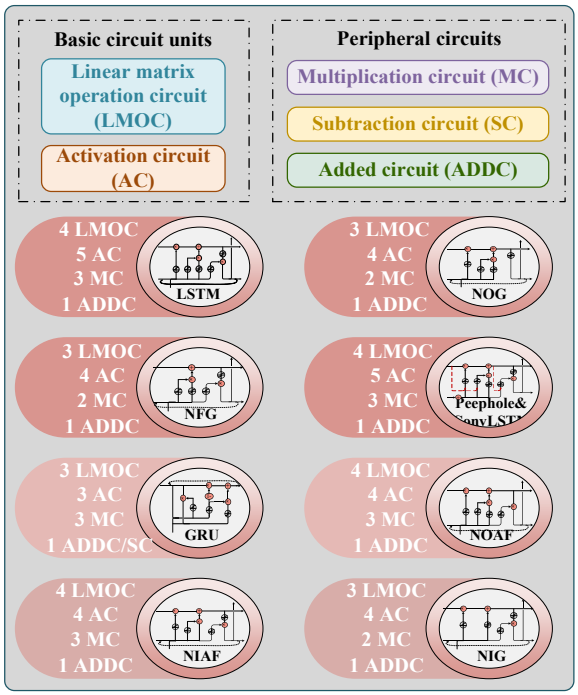

Fig. 4 Flexible design scheme for the LSTM variants.

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Table 1. Comparison of representative memristor-based neuromorphic computing systems

Reference	Device			Circuit		System	
	Materials	R_{on}/R_{off} ratio	Stability	Area	Power	Hardware-based design	Flexibility
[4]	Egg Albumin	~10^4	High stability	200.22μm^2	/	Totally	Common
[5]	Pt/TaO_x/Ta	/	/	500.22μm^2	270.17mW	Totally	Common
[6]	TiN/ TaO_x/HfO_x/TiN	/	Good stability	7.04×10^{-2}mm^2	7.44mW	Totally	Common
[7]	Pt/TiO_2/Pt	10^2~10^3	/	/	/	Partially	Common
[8]	Memristor model	/	/	/	/	Totally	Common
[9]	2D material	~10^2	High stability	0.64mm^2	1.21mW	Partially	Common
This work	Ag/TiO_x nanobelt/Ti	~10^4	High stability	74.83μm^2	100.99μW	Totally	Good

Note: the selection criterion of references is provided below: content relevance, total cited times, journal academic impact, and timeliness.

From Fig. 4, the specific design scheme can be realized by the two proposed basic circuit units and necessary peripheral circuits (including the multiplication circuit, the subtraction circuit, and the added circuit). For different LSTM variants, the corresponding circuit structure can be regarded as a recombination of the two basic circuit units and peripheral circuits, which is compact and flexible compared with the existing memristor-based neuromorphic computing systems. The specific comparison is discussed from the perspective of computing device, circuit and system, as shown in Table 1.

From Table 1, different material-based memristors can be used to realize the neuromorphic computing systems. Compared with other competitors, the prepared memristor with high stability has a wide resistance range to accommodate a large number of resistance states, which enables broad applications in neuromorphic computing. Meanwhile, the proposed circuit has advantages in terms of area overhead (achieving minimum value: 74.83μm^2) and power consumption (achieving minimum value: 100.99μW), which indicates that the proposed system is cost saving and energy-efficient. Furthermore, different with [4-9], this work provides a flexible scheme with fully hardware-implemented training strategy that can realize a specialized ANN and its variants, indicating a more universal application.

IV. Application in Affective Communication

Realization of affective communication indicates that computers could sense, recognize, and respond to human emotion, which is a great breakthrough in intelligent computing [12]. For validation, the proposed neuromorphic computing system is used to perform affective communication as present in this sub-section.

A. Algorithm description

The entire process can be divided into two phases, i.e., the training phase and the classification phase. Notably, three classical text datasets, i.e., the Internet Movie Database (IMDB) dataset (50% data for training and the remaining 50% data for testing), Stanford Sentiment Treebank (SST-2) dataset (72% data for training, 19% data for testing, and the remaining 9% data for validating), and Yelp-2 dataset (94% data for training and the remaining 6% data for testing) and a synthetic dataset generated by the Easy Data Augmentation (EDA) method are used in this part. The specific algorithm description is provided as follows:

Training phase:

Step 1: The training data (i.e., the character strings) should be firstly preprocessed, by removing all the punctuations and additional spaces, converting capital letters to the corresponding small ones, etc.

Step 2: A well-trained word2vec model [13] is used to convert the preprocessed text data into the embedding vectors. Notably, these embedding vectors can be deemed as the text features in affective communication. Then, the input voltages can be obtained through the Min-Max normalization.

Step 3: The input voltages are injected to the proposed neuromorphic computing system, and the training process begins. Notably, the specific training method is described in the Section III-B, here we do not repeat all details again.

Step 4: When the training is completed, a well-trained neuromorphic computing system is generated. Then, the validation data is applied to verify the performance of the constructed system.

Classification phase:

Step 1: Similarly, a text data is firstly preprocessed, all the punctuations and additional spaces are removed, and the capital letters is converted to the corresponding small ones.

Step 2: A well-trained word2vec model is used to convert the preprocessed text data into the corresponding feature vectors. After the Min-Max normalization, the feature vectors can be changed to the input voltages within the same size.

Step 3: The input voltages are injected to the well-trained system, and the classification result 0/1 (the low value 0 represents sadness, while the high value 1 represents happiness) can be obtained.

B. Experimental Results and Analysis

To verify the flexibility and feasibility, the LSTM variants realized by the proposed system are applied to perform affective communication. Meanwhile, some existing state-of-the-art methods (including circuit-based and soft-based methods) [7, 12, 14, 15] are also introduced for comparison purpose. Furthermore, four common performance metrics, i.e., the Accuracy, F1-Score, Recall, and time consumption are applied for objective evaluation. The specific comparison information is collected in Fig. 5.

From Fig. 5, all the methods (no matter the circuit implementation or the soft implementation) have proved effective in affective communication. It can be seen that the proposed neuromorphic computing system with LSTM configuration outperform the two existing circuit-based methods in terms of Accuracy, F1-Score, Recall, and time consumption. Meanwhile,

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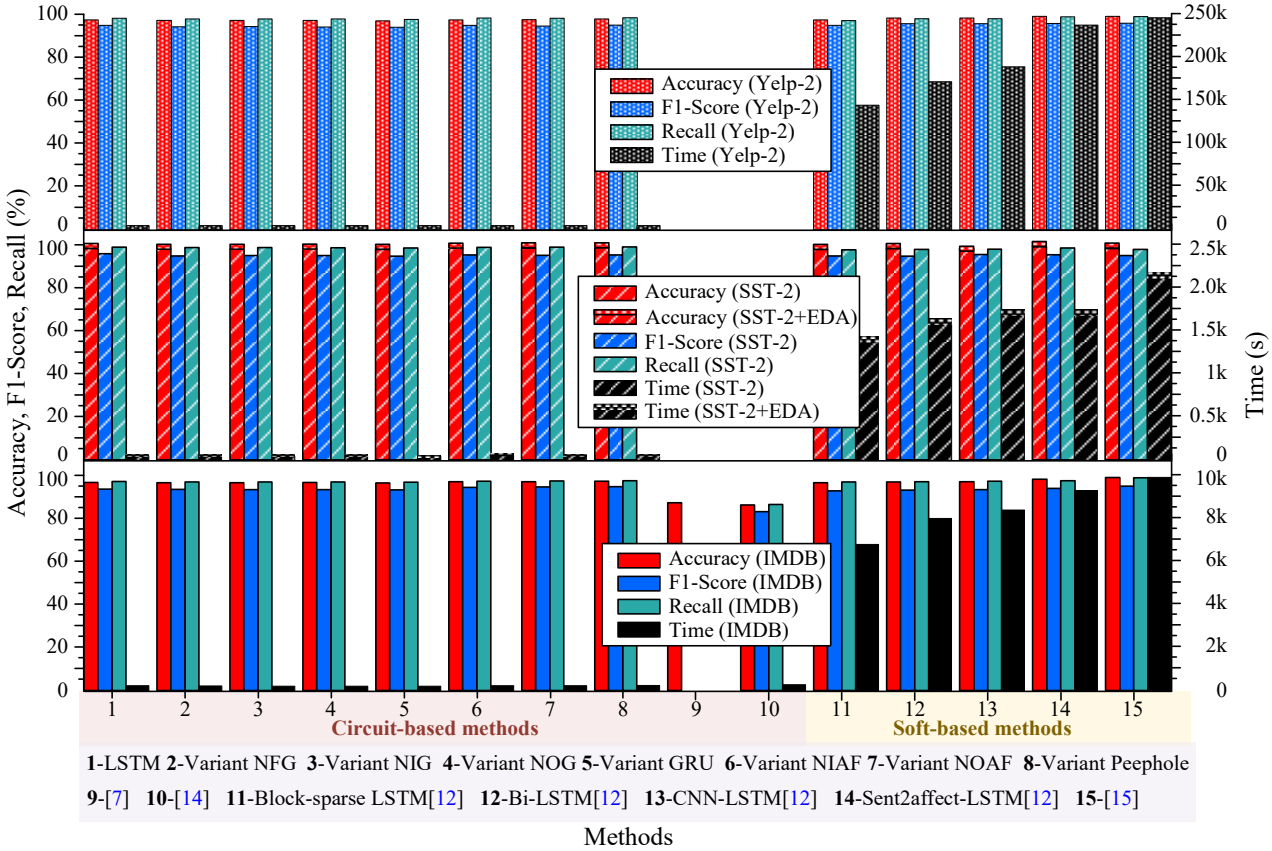

Fig. 5 Comparison of different state-of-the-art methods

almost all the soft-based methods are slightly superior to the proposed method in terms of Accuracy, F1-Score, and Recall (within an acceptable range of 5%), while inferior to time consumption (approximately 30~35 times). The results demonstrate that the trade-off between the accuracy and time consumption can be well balanced in the proposed neuromorphic computing system.

V. Conclusion

The main hindrance for existing neuromorphic computing systems produces device variation, lacking general basic circuit units, non-configurable system architecture, and inferior trade-off between accuracy and time consumption. To address these issues, a flexible neuromorphic computing system via memristor circuits is investigated in this paper. Specifically, the Ag/TiO_x nanobelt/Ti memristor is prepared and the corresponding stability analysis is conducted. Then, two basic circuit units and a hardware-friendly training method are proposed. Based on these, a flexible neuromorphic computing system with less area overhead and power consumption is proposed, which can realize the standard LSTM network and eight common types of LSTM variants, indicating a more universal application. Furthermore, the proposed system is applied to the affective communication, achieving good trade-off between accuracy and time consumption. This paper is expected to inspire research to design and implement novel neuromorphic computing systems by integrating advanced nanotechnology, material science, and artificial intelligence in order to support the development of communication applications.

VI. Future Work

Memristor-based neuromorphic computing is an interdisciplinary field of research, covering devices, circuits, architectures, algorithms and integration technologies. It is in a fast-growing stage with abundant opportunities and challenges.

At the device level: Considering the existing memory devices are almost fabricated by metal oxide materials, which makes the carbon peak and carbon neutrality hard to achieve. Highly reliable, low-cost and eco-friendly memory devices are required. Meanwhile, the corresponding physical mechanism should be thoroughly comprehended and analyzed to improve device performance.

At the circuit level: Considering the design of large-scale neuromorphic computing system is still complex and challengeable, the complexity of basic circuit units should be further reduced in the future. Meanwhile, with better understanding of brain functionalities, brain-inspired learning circuits should be designed. These are expected to improve the performance of online learning in neuromorphic computing.

At the system level: Considering daily requirement has become more diversified, the smarter neuromorphic computing system should be further design and implemented to deal with more complex tasks such as multimodal affective communication and telecommunication.

VII. Acknowledgment

This work was supported in part by the National

Natural Science Foundation of China under Grant 62001149, Natural Science Foundation of Zhejiang Province under Grant LQ21F010009 and Fundamental Research funds for the provincial Universities of Zhejiang under Grant GK229909299001-06.

REFERENCES

[1] J. Xu, K. Ota and M. Dong, "Saving Energy on the Edge: In-Memory Caching for Multi-Tier Heterogeneous Networks," in IEEE Communications Magazine, vol. 56, no. 5, pp. 102-107, 2018.
[2] W. Lu, L. Liang, B. Kong, et al., "AI-Assisted Knowledge-Defined Network Orchestration for Energy-Efficient Data Center Networks," in IEEE Communications Magazine, vol. 58, no. 1, pp. 86-92, 2020.
[3] A. Shrestha, H. Fang, Z. Mei, et al., "A Survey on Neuromorphic Computing: Models and Hardware," in IEEE Circuits and Systems Magazine, vol. 22, no. 2, pp. 6-35, 2022.
[4] X. Ji, Z. Dong, C. S. Lai, et al., "A Brain-Inspired In-Memory Computing System for Neuronal Communication via Memristive Circuits," IEEE Communications Magazine, vol. 60, no. 1, pp. 100-106, 2022.
[5] C. Li, Z. Wang, M. Rao, et al., "Long Short-term Memory Networks in Memristor Crossbar Arrays, "Nature Machine Intelligence, vol. 1, no. 1, pp. 49-57, 2019.
[6] P. Yao, H. Wu, B. Gao, et al., "Fully Hardware-implemented Memristor Convolutional Neural Network," Nature, vol. 577, no. 7792, pp. 641-646, 2020.
[7] S. Wen, H. Wei, Y. Yang, et al., "Memristive LSTM Network for Sentiment Analysis," IEEE Transactions on Systems, Man, and Cybernetics: Systems, vol. 51, no. 3, pp. 1794-1804, 2021.
[8] Z. Wang, X. Wang and Z. Zeng, "Memristive Circuit Design of Brain-Like Emotional Learning and Generation," in IEEE Transactions on Cybernetics, Early Access, 2022.
[9] Z. Dong, X. Ji, G. Zhou, et al., "Multimodal Neuromorphic Sensory-Processing System with Memristor Circuits for Smart Home Applications," IEEE Transactions on Industry Applications, Early Access, 2022.
[10] M. S. Islam and L. Vj, "Nanoscale Materials and Devices for Future Communication Networks," in IEEE Communications Magazine, vol. 48, no. 6, pp. 112-120, 2010.
[11] F. Kiani, J. Yin, Z. Wang, et al., "A Fully Hardware-based Memristive Multilayer Neural Network," Science advances, vol. 7, no. 48, pp. eabj4801, 2021.
[12] Y. Wang, W. Song, W. Tao, et al, "A systematic Review on Affective Computing: Emotion Models, Databases, and Recent Advances," Information Fusion, Early Access, 2022.
[13] K. W. Church, "Word2Vec," Natural Language Engineering, vol. 23, no. 1, pp. 155-162, 2017.
[14] K. Smagulova, O. Krestinskaya, and A. P. James, "A Memristor based Long Short-term Memory Circuit," Analog Integrated Circuits and Signal Processing, vol. 95, no. 3, pp. 467-472, 2018.
[15] S. Mai, Y. Zeng, S. Zheng, et al., "Hybrid Contrastive Learning of Tri-modal Representation for Multimodal Sentiment Analysis," IEEE Transactions on Affective Computing, Early Access, 2022.

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