TSSM: Three-State Switchable Memristor Model Based on Ag/TiO_x Nanobelt/Ti Configuration

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Memristive technologies are attractive due to their nonvolatility, high density, low power, nanoscale geometry, nonlinearity, binary/multiple memory capacity, and negative differential resistance. For memristive devices, a model corresponding with practical behavioral characteristics is highly favorable for the realization of its neuromorphic system and applications. In this paper, we propose a novel memristor model based on the Ag/TiO_x nanobelt/Ti configuration, which can reflect three different states (i.e. original stage, transition stage, and resistive switching state) of the physical memristor with a satisfactory fitting precision (greater than 99.88%). Meanwhile, this work gives (1) an insight onto the electrical characteristics of the memristor model under different humidity conditions; (2) the influence of the water molecular concentration on the memristor behavior, which is of importance for the memristor fabrication and subsequent applications. For verification purposes, the proposed three-state switchable memristor is applied to the memristor-based logic implementation. The experimental results demonstrate that the constructed circuit is able to realize basic Boolean logic operations with fast response speed and high efficiency.

Keywords: Memristor; Ag/TiO_x nanobelt/Ti configuration; humidity conditions; logic implementation.

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1. Introduction

In 1971, Leon Chua originally predicted the existence of memristor based on the completeness of circuit theory [Chua, 1971]. About forty years later, Hewlett Packard (HP) researchers announced the physical implementation of memristor [Strukov *et al.*, 2008]. As the fourth fundamental circuit element, memristor possesses numerous unique properties such as nonvolatility, high density, low power, nanoscale geometry, nonlinearity, binary/multiple memory capacity, and negative differential resistance (NDR), which makes it a powerful candidate in many potential applications including intelligent computing, biomimetic sensing systems, high-density resistive random access memory, signal processing [Ho *et al.*, 2010; Jo *et al.*, 2010; Yang *et al.*, 2012], etc. Especially, the interest in the memristor-based neuromorphic system has skyrocketed recently [Wang *et al.*, 2017a; Dong *et al.*, 2018a; Yao *et al.*, 2020]. Correspondingly, the memristive device materials, fabrication processing, and internal structures have also been developed concurrently.

Memristors can be viewed as ion-electron coupled devices whose resistance transition behavior is accompanied by electron transport, ion migration, along with its redox reactions [Duan *et al.*, 2014]. To meet the performance and functional requirements of memristors, the study and development of high performance memristive systems have been the key scientific concern. Currently, several materials have been utilized to fabricate memristors, including inorganic metal oxides, chalcogenides, nitrogen, carbon, and organic materials. Among the inorganic metal oxides, binary oxides such as HfO_x [Li *et al.*, 2019], NiO_x [Gul, 2019], and TiO_x [Zhao *et al.*, 2019a] are receiving increasing interest as they offer high potential scalability, low-energy switching, thermal stability. Meanwhile, some ternary or composite materials are also considered for the memristor fabrication, such as $BiMnO_3$ [Guan *et al.*, 2019], $BiFeO_3$ [Sun *et al.*, 2020], $FeWO_4$ [Barcaro & Fortunelli, 2019], and $La_{0.7}Sr_{0.3}MnO_3$ [Riminucci *et al.*, 2019]. The memristive effects have been observed in chalcogenides (MoS_2 [Krishnaprasad *et al.*, 2019], $MoSe_2$ [Mao *et al.*, 2019], and Ag_2S [Oliveira *et al.*, 2019], oxides of nitrogen (TiN [Zhou *et al.*, 2019a] and SiN [Gismatulin *et al.*, 2019]) and even in lower carbon oxides (graphene oxides [Romero *et al.*, 2019]). Notably, using several common organic materials in memristive devices raises a lot of expectation for future applications due to their flexibility, durability, and degradability. For example, Sun *et al.* treated orange peel to prepare memristors that exhibits superior switching endurance accompanied by an OFF/ON resistance ratio (storage density window) of about 450 [Qi *et al.*, 2019]. The resistive switching (RS) devices based on natural silk protein with configurable functionality are demonstrated in [Wang *et al.*, 2015]. The results suggest that silk protein possesses the potential for sustainable electronics and data storage.

It is noted that many memristors have been consecutively fabricated utilizing different materials and mechanisms. However, the uncertainty of conductive filaments formation/disruption or the oxygen vacancies migration leads to a significant difference between devices, posing a substantial challenge to the device system integration. Currently, memristors applied in most integrated applications are always their mathematical models, on account of the complicated fabrication processing and high fabrication cost. With the increasing development of memristor theory, a variety of memristor mathematical models have been proposed. The breakthrough for memristors and RRAM devices provided by the HP model is discussed in [Zhao *et al.*, 2019a]. Linear/nonlinear ion drift effects [Biolek *et al.*, 2009; Kvatinsky *et al.*, 2012], which form the basics of the mechanism of these devices, are considered. The Pickett–Abdalla model [Panda *et al.*, 2018] which laid the foundation for SPICE compatible physics-based models is covered in-depth. Its various features which have been adopted and refined by the Yakopcic model [Yakopcic *et al.*, 2013; Kvatinsky *et al.*, 2012; Wang *et al.*, 2017a] are also covered. Although these models correspond with the basic characteristics of memristors, there are several practical behavioral characteristics that are not highlighted when we consider the ion mobility theory, especially humidity [Zhou *et al.*, 2018, 2019a]. Using the first-principles calculations, Li determined that the water molecules in the air can interact directly with the oxygen vacancies on the surface of TiO_2 or indirectly with the oxygen vacancies on the sub-surface [Li & Gao, 2014]. Messerschmitt *et al.* fabricated $Pt/SrTiO_{3-\delta}/Pt$ devices and plotted their I–V characteristic curves at different moisture levels. It was discovered that the saturation current of the devices is four orders of magnitude larger than that of the devices in the air

when the air humidity is high, indicating that the moisture in the air can regulate the performance of the device [Messerschmitt *et al.*, 2015]. Valov *et al.* demonstrated that water molecules in the air break down with surface oxygen vacancies during which the reduction of the latter at the cathode has a significant effect on the formation of ions through anodic oxidation and formation of conductive filaments through migration [Tappertzhofen *et al.*, 2013]. The memristor behavior of transition metal oxides (TiO_x) on a nanometer scale was studied in [Zhou *et al.*, 2020]. The interplay-induced memristor evolution stage involving an original stage (nonstandard faradic capacitance, NFC), transition stage (battery-like capacitance, BLC), and resistive switching state (RS) were discovered in the Ag/TiO_x nanobelt/Ti device under different moisture levels. Therefore, the Ag/TiO_x nanobelt/Ti device [Zhou *et al.*, 2020] is selected as the research object, and the main contributions of this paper are as follows:

(1) According to the actual device data, a three-state switchable memristor model (TSSM) based on the Ag/TiO_x nanobelt/Ti device is proposed, which can reflect three different states (i.e. NFC, BLC, and RS) of the physical memristor with a satisfactory fitting precision (greater than 99.88%).
(2) Through the investigation of the electrical characteristics of the memristor model under different humidity conditions, the influence of the water molecular concentration on the memristor behavior is explored, which is of importance for the memristor fabrication and subsequent application.
(3) Unlike the physical Ag/TiO_x nanobelt/Ti device, the proposed TSSM model can be applied into different memristor-based applications (e.g. logic implementation) directly, irrespective of strict laboratory conditions.

The rest of this paper is organized as follows. In Sec. 2, the preparation process of Ag/TiO_x nanobelt/Ti memristor is introduced, and the specific physical mechanism and the memristive characteristics in different air humidities are described. In Sec. 3, the mathematical and circuit models are built up based on the measured memristor data, and its validity and effectiveness are verified by theory and quantitative analysis. In Sec. 4, the electrical characteristics of the proposed model under external excitation are compared and analyzed through a series of circuit simulations. For verification, a classical logic implementation using the proposed TSSM model is performed in Sec. 5. Section 6 summarizes the entire paper.

2. Experiment Section

2.1. *Memory device fabrication*

In this paper, the TiO_x nanobelts were synthesized using hydrothermal method. Specifically, the Ti metal substrates were sequentially cleaned by deionized water and ethyl alcohol for 30 min to remove surface contaminants. Then, the Ti metal substrates were thermally processed in air at 200*C for 3 h. Next, the 2.0 g sodium hydroxide (NaOH) was dissolved in 20 ml deionized water and stirred at room temperature for 30 min. The precursor solution was prepared by adding 2.0 g TiO_2 nanopowders (the nano-sphere with an average diameter of 20 nm) to the NaOH solution. After hydrothermal reaction at 200°C for 48 h, a blue-gray film was grown on the surface of the Ti substrate. The TiO_x nanobelt arrays can be obtained by cleaning the bluish-gray film with 10% hydrochloric acid (HCL) for 90 s and deionized water for 10 min. After that, the TiO_x nanobelts samples were thermally processed at 80°C for 24 h to remove possible residual HCL. The Ag electrode with a diameter of 200 μm was sputtering through for 3 min in the presence of 0.5 Pa Ar reactive gas and 20 W sputtering power. Therefore, Ag/TiO_x nanobelt/Ti memristors could be fabricated.

All calculations in this work were performed using the density functional theory (DFT) calculations as implemented in the Vienna Abinitio Simulation Package (VASP). The electron-ion interaction calculations are based on the Projector Augmented Wave (PAW) method. The generalized-gradient approximations (GGAs) in use in modern electronic-structure theory were utilized to describe the exchange-correlation interactions.

The TiO_x nanobelts were studied using the high-resolution transmission electron microscopy (HR-TEM). The average width, average length, and standard deviation of nanobelts were determined using the field emission scanning electron microscopy (FE-SEM). The chemical component of TiO_x nanobelts was done using X-ray photoelectron spectroscopy (XPS) and X-ray diffraction (XRD) (D500, Siemens) with a glancing angle of 5° was

used to determine the crystallinity of the TiO_x nanobelts. It is noted that the entire preparation process of the Ag/TiO_x nanobelt/Ti device is refered to in [Zhou *et al.*, 2020].

2.2. *Memristive effect of Ag/TiO_x nanobelt/Ti at different humidities*

All electric measurements were performed from a cavity of a probe system (Lake Shore, TTPX) in the electrochemical workstation (CHI, 660D). Under laboratory conditions, the air relative humidity was commonly 35%–45%. Dry air with a relative humidity of 0% (20% O_2, 80% N_2, and H_2O (g) < 5 ppm) were artificially synthesized by flowing air into three interconnected heated-glass delivery tubes filled with dry CaO nano-powders. Then the dry air could be injected into the cavity with background vacuum of 5×10^{-4} Pa. Moisture air (RH = 95%–100%) can be obtained by flowing laboratory air into a gas-washing bottle filled with deionized water.

A schematic diagram for the NFC, BLC and RS states of a scene including the H2O adsorption, splitting and interplay between ions and electrons is demonstrated in Fig. 1(a). The consecutive I–V curves under the bias voltage scan rate of 1 v/s and the bias voltage sweep sequence

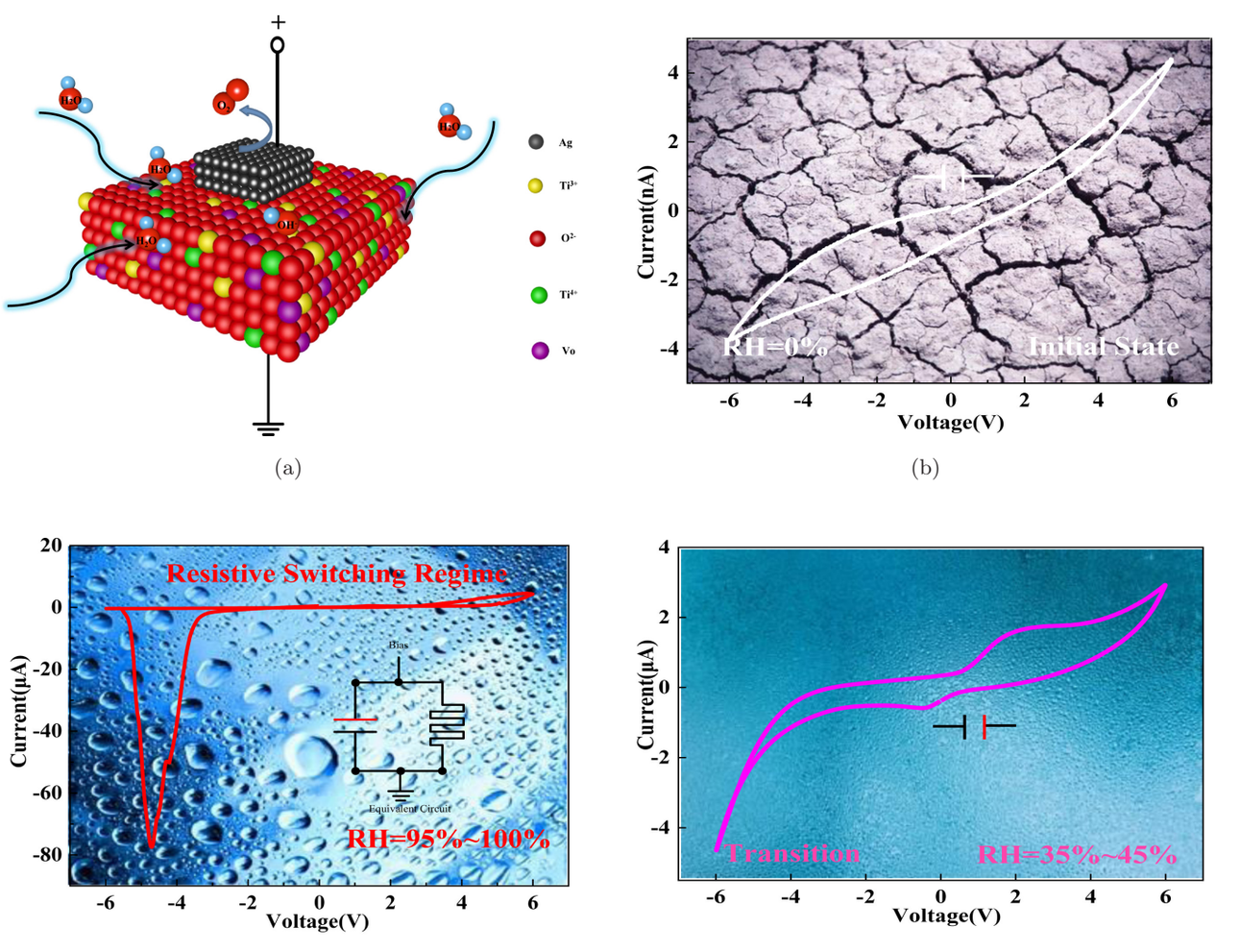


Fig. 1. (a) Schematic diagram of water molecules reaction in air with oxygen vacancies on the surface and interface of the functional layer of Ag/TiO_x nanobel/Ti devices. (b) I–V characteristic curve at 0% relative humidity. (c) I–V characteristic curve at 35%–45% relative humidity. (d) I–V characteristic curve at air relative humidity of 95%–100%. The background is an exaggerated representation of relative humidity.

0 V → −6 V → 0 V → 6 V → 0 V were measured under three RH levels (RH = 0%, 35%–45%, 95%–100%). The NFC is expectedly observed in the RH level of 0%, as shown in Fig. 1(b). Then, oxidized and reduced peaks appeared when the RH level was increased from 0% to 35%–45% (i.e. BLC state), and the high current feature is observed as well [as shown in Fig. 1(c)]. The device under the RH of 95%–100% exhibits the resistive switching (RS) memory due to the fact that the *I*–*V* curves are pinched [as shown in Fig. 1(d)]. The results suggest that the resistance switching behavior and evolution of Ag/TiO_x nanobelt/Ti memristors can be realized by changing the ambient humidity.

According to [Zhou *et al.*, 2020], an energy band-based physical model for explaining the evolution process of memristor under different moisture levels is exhibited in Fig. 2. The physical dynamic processes can be constructed for the NFC, BLC and RS states. The physical processes can be divided into four phases:

(1) For dry environment (RH = 0%), the restriction for both ion migration and surface-based reaction results in the TiO_x nanobelt device showing NFC behaviors [Fig. 2(a)];
(2) As the air humidity increases, the NFC is enhanced when the surface of the TiO_x nanobelt absorbs H_2O [Fig. 2(b)];
(3) As the air humidity continues to increase, a series of redox reactions are triggered by the adsorbed H2O and the active surface oxygen vacancy V_o. Then, the electron transferred from the H_2O to the surface/subsurface of the TiO_x nanobelts makes the device convert to the BLC [Fig. 2(c)];
(4) The coupling between the ions and electrons becomes very strong (migration, diffusion, and electron transfer) at higher moisture levels (RH = 95%–100%), driving the device into RS state [Fig. 2(d)].

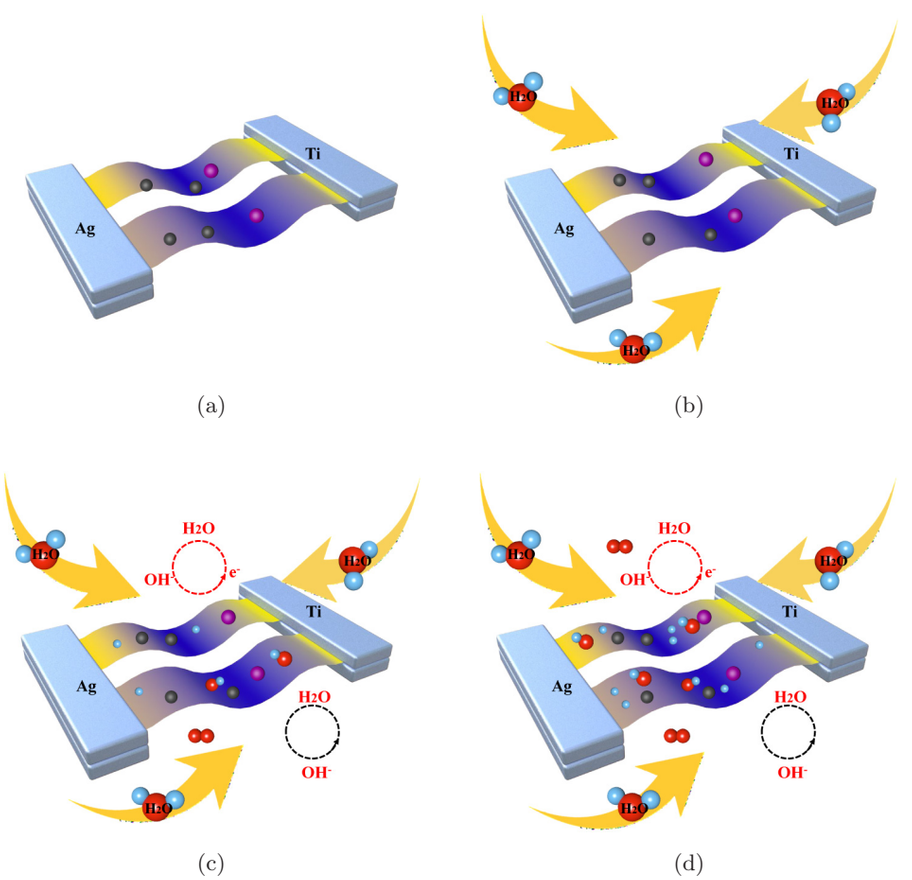


Fig. 2. Ag/TiO_x nanobelt/Ti memristor with triangular-wave voltage of 1 v/s applied at both ends. (a) NFC fitting, (b) BLC fitting and (c) RS fitting.

3. Memristor Modeling

3.1. *Demonstration of PSPICE analysis*

Generally, a voltage/current-controlled memristive system can be represented by [Panda *et al.*, 2018]:

$$\frac{dx}{dt} = F(x(t), v(t)), \tag{1}$$

$$i(t) = G(x(t), v(t)) \cdot v(t), \tag{2}$$

where $x(t)$ is the internal state variable, $v(t)$ is the applied voltage, $i(t)$ means the current passing through the memristive device, and $G(x(t), v(t))$ denotes the memconductance. From (2), it can be observed that the memconductance varies depending on the internal state variable and the current voltage.

An available memristor model should reflect and predict the behaviors of devices under a given stimulus. Based on the analysis in Sec. 2.2, it can be seen that the charged mobile ions (e.g. oxygen ions in TiO_x) would drift under the influence of the electric field and different moisture levels, leading to variations of the inner state variable. For TiO_x based devices, a Schottky barrier is always formed between the TiO_x nanobelts and Ti metal substrates, while an electron tunneling layer always develops when different stimulus is applied to the Ag electrode. The relationship between electric field intensity and ion migration speed is not linear, but always exponential. In addition, due to the high mobility of V_o, diffusion effects of the charged mobile ions should be considered as well.

In this section, a memristor model can be analyzed in two behavioral parts as shown in Fig. 3. The current source G_m in Fig. 3(a) holds the I–V relationship for the device. The terminals TE and BE represent the top and bottom electrodes of the memristor, where the model would be connected in a circuit schematic.

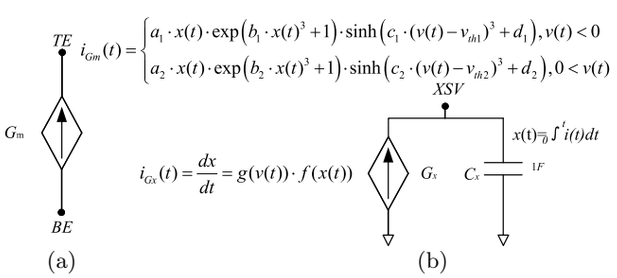


Fig. 3. PSPICE structure of the memristor.

From Fig. 3, the current and voltage relationship can be described by:

$$i_{Gm}(t) = \begin{cases} a_1 \cdot x(t) \cdot \exp(b_1 \cdot x(t)^3 + 1) \\ \quad \cdot \sinh(c_1 \cdot (v(t) - v_{\text{th1}})^3 + d_1), \\ \qquad\qquad v(t) < 0, \\ a_2 \cdot x(t) \cdot \exp(b_2 \cdot x(t)^3 + 1) \\ \quad \cdot \sinh(c_2 \cdot (v(t) - v_{\text{th2}})^3 + d_2), \\ \qquad\qquad 0 < v(t), \end{cases} \tag{3}$$

where $a_1, a_2, b_1, b_2, c_1, c_2, d_1$ and d_2 are all the fitting parameters of the model. Notably, these fitting parameters can be used to adjust the I–V response curve of the model to approximate the actual physical model under different moisture levels. In particular, the conductivity ability of the device is related to the values of the fitting parameters a_1, a_2, c_1 and c_2.

Figure 3(b) shows how the value of the state variable is determined using another current source and a capacitor. As can be seen, as the derivative of state variable $x(t), G_x$ is used to model the state variable motion in each of the memristor devices. The capacitor C_x is used to integrate the current generated by G_x to produce the value of the state variable. This technique has been proved effective in several memristor SPICE models [Yakopcic *et al.*, 2013; Kvatinsky *et al.*, 2012; Wang *et al.*, 2015; Dong *et al.*, 2018a]. Notably, the port XSV is created to provide a convenient method for representing the internal state variable.

The change of the state variable depending on two different functions $g(v(t))$ and $f(x(t))$ can be mathematically expressed as:

$$i_{Gx}(t) = \frac{dx}{dt} = g(v(t)) \cdot f(x(t)), \tag{4}$$

where $g(v(t))$ is a piecewise function, and its expression can be written as:

$$g(v(t)) = \begin{cases} k_L \cdot (v(t) - v_{\text{th1}})^{\alpha_L}, & v(t) < v_{\text{th1}} < 0 \\ 0, & v_{\text{th1}} \le v(t) \le v_{\text{th2}} \\ k_H \cdot (v(t) - v_{\text{th2}})^{\alpha_H}, & 0 < v_{\text{th2}} < v(t) \end{cases} \tag{5}$$

where k_H, k_L, α_H and α_L are the model fitting parameters. In general, parameter k_H is a positive constant, while k_L is a negative constant. v_{th1} and v_{th2} denote the threshold voltages, and $v(t)$ is the voltage applied to the memristor. It is noted that the state variable is constant if the applied voltage satisfies $v(t) \in [v_{\text{th1}}, v_{\text{th2}}]$; for other cases, the state variable will change in different ways.

Meanwhile, $f(x(t))$ composed of $f_H(x)$ and $f_L(x)$ behave as window function [Biolek *et al.*, 2009; Dong *et al.*, 2018b], which are utilized to constrain the state variable $x(t)$ within the range of $[x_{\min}, x_{\max}]$. R_L and R_H are the corresponding boundary resistances of the device when the state variables are $x_{\min}$ and $x_{\max}$ respectively. The window function assumes the following form:

$$f(x(t)) = \begin{cases} f_L(x) = \exp\left(-\exp\left(\dfrac{a_L - x}{w_c}\right)\right), \\ f_H(x) = \exp\left(-\exp\left(\dfrac{x - a_H}{w_c}\right)\right), \end{cases} \tag{6}$$

where w_c, a_L, and a_H represent fitting parameters.

The memristor model is implemented into the library of a circuit simulator (PSPICE), and the subcircuit description is provided in Table 1.

3.2. *Memristive devices fitting*

Ideally, a memristive model should reflect experimental data. To evaluate the accuracy of the proposed model, we fit these models to measured data by adjusting to minimize the error function. To perform the fitting, we use Gradient Descent [Mandt *et al.*, 2017] to minimize the relative error function value. The error function is selected as relative root mean squared error (RMSE):

$$E_{\text{rms}} = \sqrt{\frac{1}{N} \cdot \left(\frac{\sum_{n=1}^{N} (V_{\text{pro},n} - V_{\text{ref},n})^2}{V_{\text{ref}}^2} + \frac{\sum_{i=1}^{N} (I_{\text{pro},n} - I_{\text{ref},n})^2}{I_{\text{ref}}^2} \right)}, \tag{7}$$

where N is the total number of samples, $V_{\text{pro},n}$ and $I_{\text{pro},n}$ are the characteristics of the nth sample of the model under examination, $V_{\text{ref},n}$ and $I_{\text{ref},n}$ are the characteristics of the nth sample of reference data, and V_{ref} and I_{ref} are the Euclidean norms of their respective reference data.

Table 1. Subcircuit description of the TSSM model.

*TSSM model
Connection
TE-top electrode
BE-bottom electrode
XSV-External connection to plot state variable that is not used otherwise
.SUBCKT Memristor mode TE BE XSV:
.params a1 = 0.008 a2 = −500 b1 = −0.308 b2 = 8.15 c1 = 0.0066 c2 = 2E−8 d1 = 9.96E−5 d2 = 1.0
+Vth1 = 0 Vth2 = 0 kL = −5.66 AlphaL = 1.0 aL = 0.096 kH = 2.9E−5 AlphaH = 4.0 aH = 0.041 wc = −0.047
*****Multiplication functions to ensure zero state*****
**********Function dx/dt=F(x(t),v(t))**********
.func F(x, v, kL, kH, AlphaL, AlphaH, aL, aH, wc) = {If(v < Vth1, f1(x, v, kL, Vth1, AlphaL, aL, wc),
+If(v > Vth2, f2(x, v, kH, Vth2, AlphaH, aH, wc), 0))}
.func f1(x, v, kL, Vth1, AlphaL, aL, wc) = kL*(v − Vth1)^AlphaL ∗ exp(−exp((aL − x)/wc))
.func f2(x, v, kH, Vth2, AlphaH, aH, wc) = kH*(v − Vth2)^AlphaH ∗ exp(−exp((x − aH)/wc))
IV Response Hyperbolic sine due to MIN structure
.func IVRel(V) = {If(v < 0, a1 ∗ x ∗ exp(b1 ∗ x^3 + 1) ∗ sinh(c1 ∗ (V − Vth1) + d1)),
If(v > 0, a2 ∗ x ∗ exp(b2 ∗ x^3 + 1) ∗ sinh(c2 ∗ (V − Vth2) + d2))}
********Circuit to determine state variable********
Cx XSV 0 {1}
.ic V(XSV) = x0
Gx 0 XSV
*****Current source for memristor IV response*****
Gm TE BE value = {IVRel(V(TE, BE), V(XSV, 0))}
.ENDS TSSM model

During the fitting procedure, related parameters are iterated and adjusted to minimize the error function (7). The fitting results to measured data for the proposed model can reflect the three different states (i.e. NFC, BLC, and RS) of the physical memristor, as shown in Fig. 4. The corresponding parameters are listed in Table 2. Notably, the fitting parameters for the three states of the memristor are different and switchable.

From the simulations in Fig. 4(a), the model can describe the NFC state in dry environment (i.e. RH = 0%), where the model was able to match the measured data points with the RMSE values of 0.12%. Migration and interplay between ions and electrons are effectively restricted for the NFC observed in dry ambient conditions. The device with less Vo usually has a lower current drawn that may lead to higher switching threshold ($-v_{\mathrm{th1}} = v_{\mathrm{th2}} = 2\,\mathrm{V}$). Those parameters that are the lowest compared to the other two states include the conductivity parameters a_1, a_2, c_1, and c_2, and the initial position of the state variable x_0, corresponding to the output current of the nanoampere level.

The simulated I–V characteristic was matched to the measured data provided in the BLC state under moisture environment (RH = 35%–45%) with the RMSE values of 0.08%, as shown in Fig. 4(b). After exposing to the moisture atmosphere (RH = 35%–45%), the surface Vo becomes more sensitive to the H_2O molecules, where the H_2O splitting, migration and interplay between ions and electrons have occurred. Experimentally, we saw that the proposed model switched ON at about $+1\,\mathrm{V}$ and OFF at about $-1\,\mathrm{V}$, with the corresponding switching current up to the μA level. Those parameters that are increased include the conductivity parameters a_1, a_2, c_1, and c_2, and the initial position of the state variable x_0.

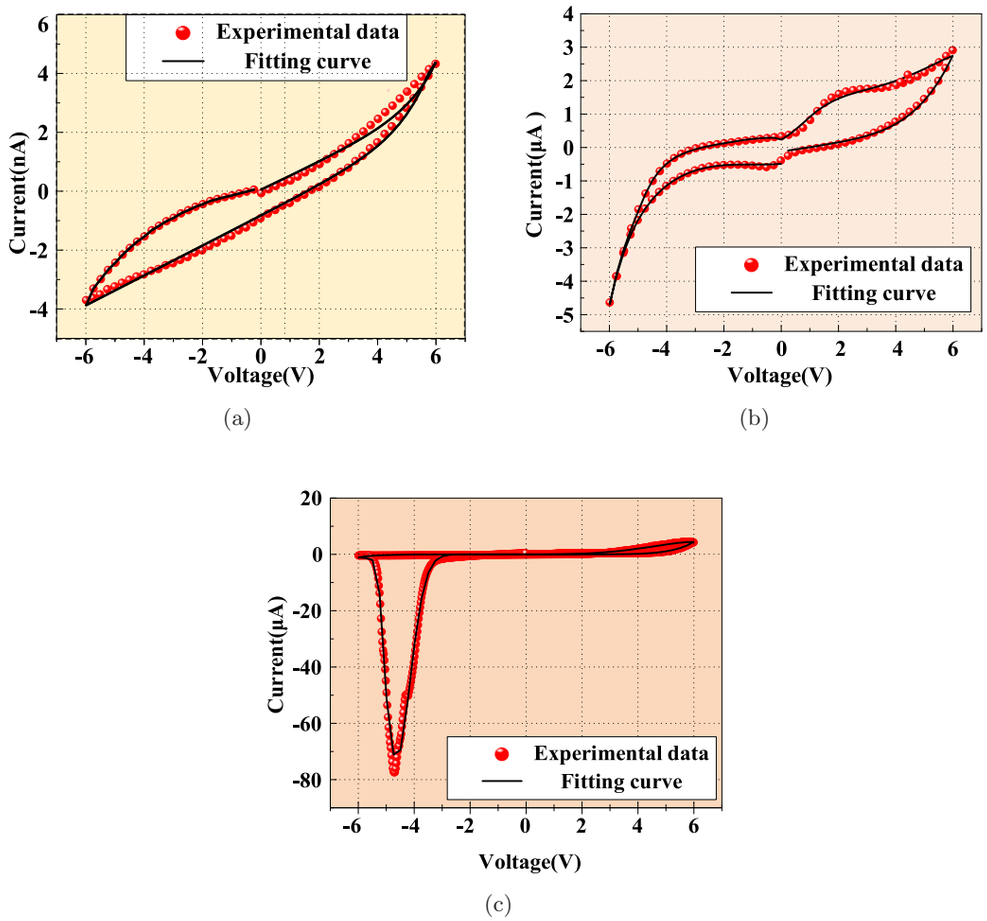


Fig. 4. Ag/TiO_x nanobelt/Ti memristor with triangular-wave voltage of 1 v/s applied at both ends. (a) NFC fitting, (b) BLC fitting and (c) RS fitting.

Figure 4(c) shows the result when matching the measured data provided in the RS state under a humid environment (RH = 95%–100%) with the RMSE values of 0.03%. When the moisture level is increased to the RH of 95%–100%, strong interplay with ions, electron transfer and migration of OH^- ions push the device into the RS state. The voltage threshold of RS state is the same as BLC state ($-v_{th1} = v_{th2} = 1\,V$). The fitting parameters a_1, a_2, c_1, and c_2 representing the conductivity increase sharply, and the corresponding output current is increased nearly ten times compared with the BLC state.

4. Characteristic Analysis of Memristors

The SPICE model from Sec. 3 was used for the simulation of experiments described in [Zhou *et al.*, 2020]. The corresponding results are shown in Figs. 5–8, and the corresponding parameters are listed in Table 2. In each case, the memristor is driven by a voltage source.

From Fig. 5, the external stimulus is a triangular-wave voltage with the amplitude of 6 V and frequency of 1 Hz. The black and red curves respectively represent the applied voltage and the current flowing across the TSSM model, as shown in Figs. 5(a), 5(d) and 5(g). The *I–V* relationship are shown in Figs. 5(b), 5(e) and 5(h). The memconductance curve are shown in Figs. 5(c), 5(f) and 5(i). The NFC state can be described by four stages. In the first stage (0 V–6 V), the current slowly increases to the highest value at 6 V. Here, we define the current value at 6 V as the positive maximum ($I_{max}+$). In the second stage (6 V–0 V), the current gradually decreases, but larger than the first stage at the same voltage point. Namely, two different resistance states exist for the two stages. In the third stage (0 V–−6 V), the current value gradually increases to the highest value at −6 V. Here, we define the current value at −6 V as the negative maximum ($I_{max}-$). In the fourth stage (−6 V–0 V), the current slowly decreases. The simulations of the NFC state indicate negative incremental resistance. It is worth noticing that the redox peaks are observed in the *I–V* curves in BLC state. The $I_{max}+$ and $I_{max}-$ are set to −3.5 nA and 4.0 nA for the NFC state, but they sharply increase to $-4.0\,\mu$A and $2.5\,\mu$A when entering into the BLC state. The Imax increases near three orders after exposing into the atmosphere with RH of 35%–45% ambient. Therefore, the NFC as a former state of the BLC is observed in the proposed TSSM model. The RS state can be described in four stages. In the first stage (0 V–6 V), the model is in the OFF state, namely, the high resistance state (HRS). With a forward bias voltage between 0 V and 1 V, a negligible current is generated. As the applied voltage increases over 1 V, the current value sharply increases, and the value reaches a maximum value at 6 V. In the second stage (6 V–0 V), the model

Table 2. Collection of memristor fitting parameters.

Parameter	Nonstandard Faradic Capacitance (NFC)	Battery-Like Capacitance (BLC)	Resistive Switching State (RS)
a_1	2.682e−6	2.998e−4	0.011
a_2	1.166e−7	5.004e−6	0.059
b_1	−3.199e+3	−2.195e+3	−0.308
b_2	−1.176e+3	208.688	5.781
c_1	1.162e−4	7.875e−4	6.600e−3
c_2	1.700e−3	0.011	7.998
d_1	0.011	0.050	9.956e−5
d_2	−0.164	−0.256	4.881e−7
k_L	−0.310	−1.641	−6.379
k_H	0.251	1.162	2.860
α_L	2.673e−4	−0.021	1.000
α_H	1.8746e−4	−2.159e−5	2.822
a_L	1.167e−3	0.093	30.332
a_H	0.7132	8.358	14.913
w_c	−0.034	−0.084	−0.497
x_0	0.001	0.011	0.011
RMSE	0.12%	0.08%	0.03%

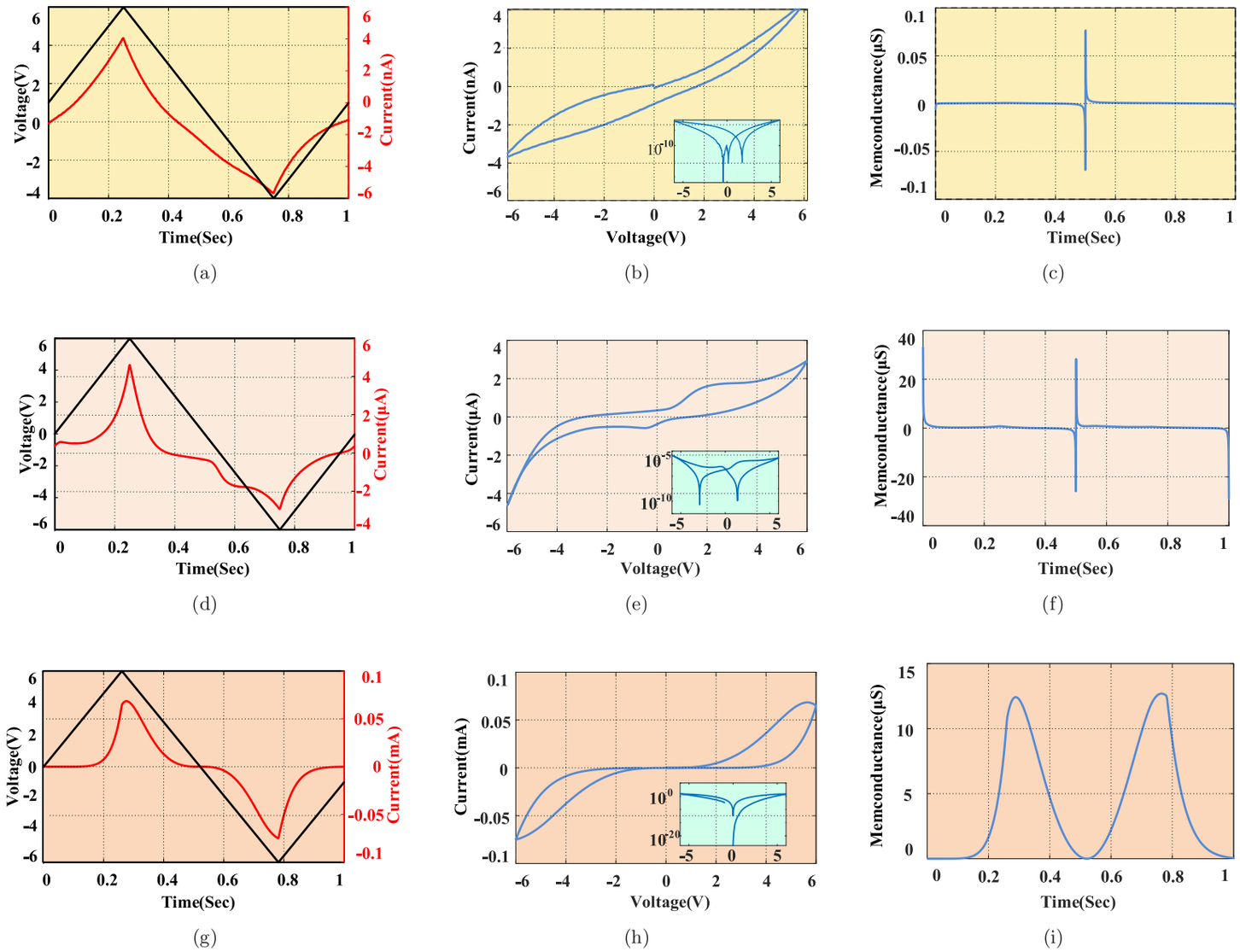


Fig. 5. Numerical simulation results of memristor model under triangular-wave voltage. (a)–(c) V & I–t, I–V, and M–t curves of NFC model. (d)–(f) V & I–t, I–V, and M–t curves of BLC model. (g)–(i) V & I–t, I–V, and M–t curves of RS model.

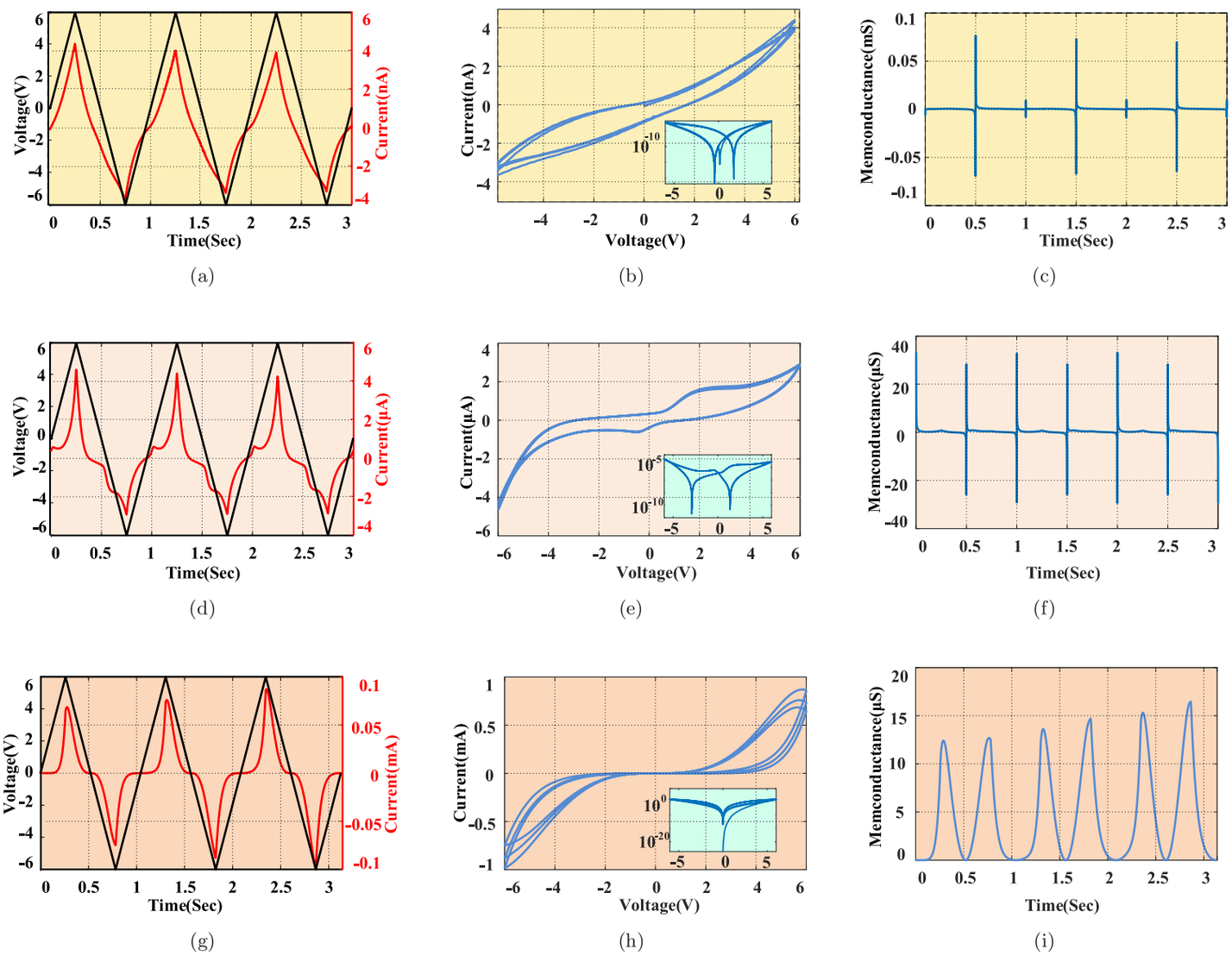


Fig. 6. Numerical simulation results of memristor model under triangular-wave voltage. (a)–(c) V & I–t, I–V, and M–t curves of NFC model. (d)–(f) V & I–t, I–V, and M–t curves of BLC model. (g)–(i) V & I–t, I–V, and M–t curves of RS model.

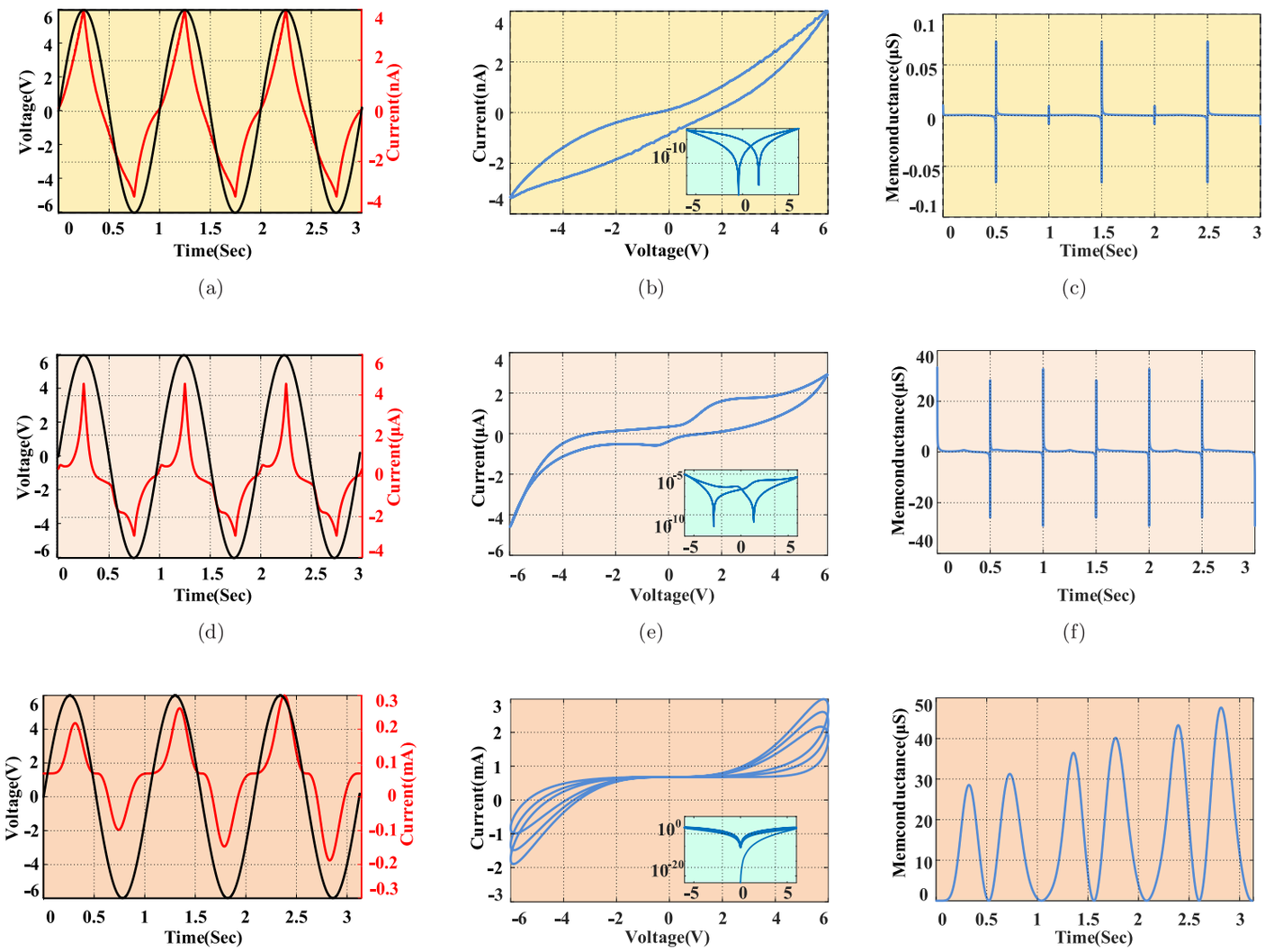


Fig. 7. Numerical simulation results of memristor model under sinusoidal voltage $v(t) = 6\sin(2\pi t), t = [0, 3]$. (a)–(c) V & I–t, I–V, and M–t curves of NFC model. (d)–(f) V & I–t, I–V, and M–t curves of BLC model. (g)–(i) V & I–t, I–V, and M–t curves of RS model.

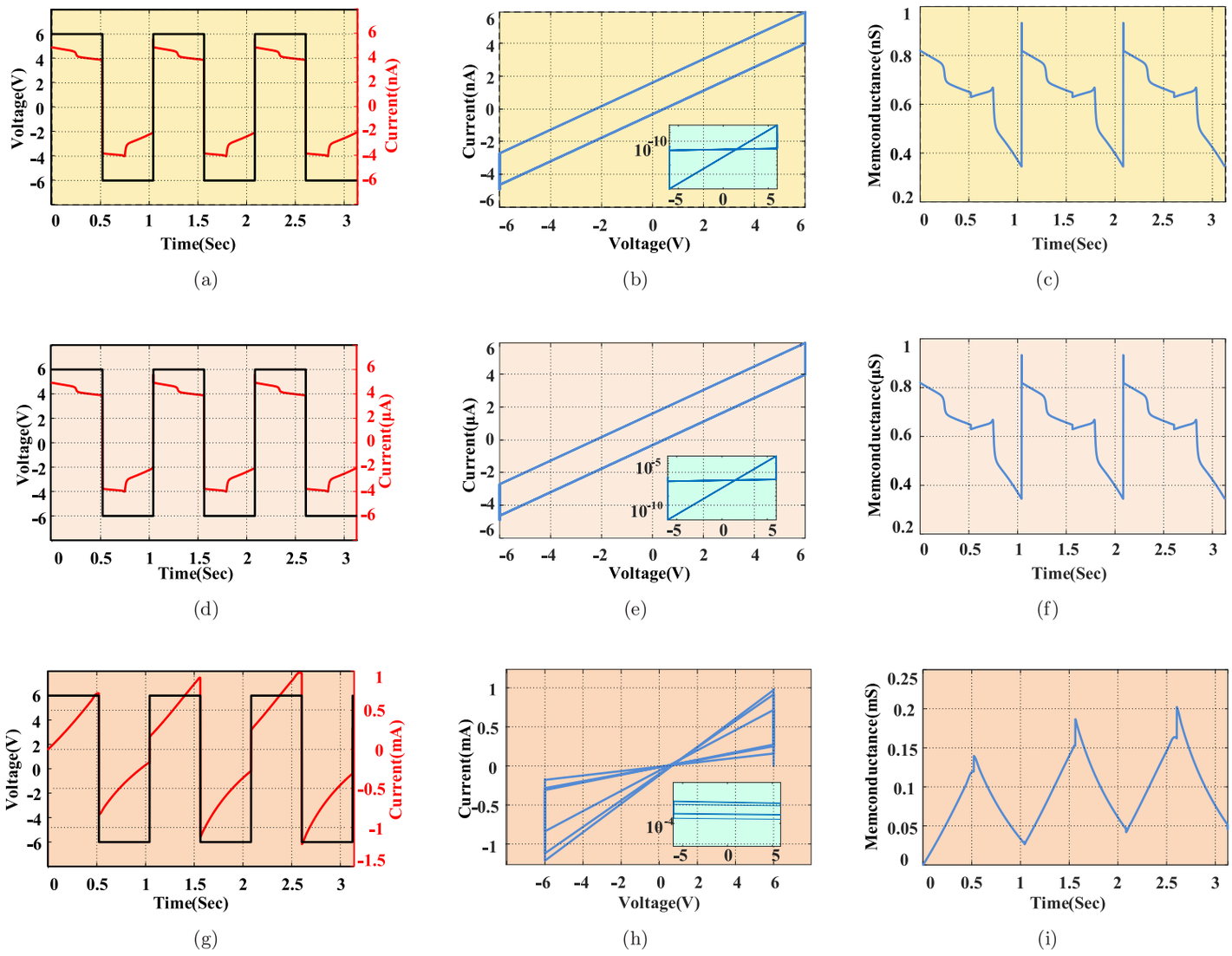


Fig. 8. Numerical simulation results of memristor model under rectangle-wave voltage. (a)–(c) V & I–t, I–V, and M–t curves of NFC model. (d)–(f) V & I–t, I–V, and M–t curves of BLC model. (g)–(i) V & I–t, I–V, and M–t curves of RS model.

switches to the ON state, namely, the low resistance state (LRS). Similarly, the third (0 V–−6 V) and fourth stages (−6 V–0 V) correspond to LRS and HRS, respectively.

From Fig. 6, when the same triangular-wave voltage is applied to the TSSM model within the time interval $[0, 3]$, it can be seen that there is no significant change in the shape of the curve and the maximum current is as compared to the memristor response curves in Fig. 5. The asymmetrical shape of the hysteresis I–V curves is well maintained in the RS model, but the maximum current increased slightly from 0.16 mA to 0.28 mA, as illustrated in Figs. 6(g)–6(i). Combined with the physical mechanism of the actual operation of memristors, the device exposure to the air allows the absorption of H_2O by the TiO_x nanobelt. The OH^- produced by the decomposition of H_2O move in an electric field, contributing to the current of the device.

Figure 7 shows the memristor response curves of the TSSM model (i.e. NFC, BLC, and RS) under a sinusoidal voltage $v(t) = 6\sin(2\pi t), t = [0, 3]$. Compared with the memristor response curves in Fig. 6, the coincidence degree of the I–V curve between the NFC and BLC models under sinusoidal voltage is clearly higher than that under triangular-wave voltage. The I–V curve of the RS model drifts [as shown in Fig. 7(h)], indicating that the conduction performance of the model under sinusoidal voltage continues to increase to a higher range. The maximum current value is nearly three times higher than that of the triangular-wave excitation.

Figure 8 displays the memristor response curves of the TSSM model under a rectangle-wave voltage with the amplitude of 6 V and frequency of 1 Hz. It can be found that the I–V characteristics exhibit significant hysteresis with an obvious capacitive effect in NFC model and BLC model in which a "Set" process is shown in the positive voltage region and the "Reset" process is exhibited in the negative voltage region. The RS model has remarkable switching characteristics in which 6V makes the model jump from the HRS to the LRS, and the opposite direction of the jump occurs in the symmetrical −6 V. The memconductance of the RS model increases continuously in the process of positive polarity repetitive programming. On the contrary, the I–V curve of the model exhibits a downward drift under the negative voltage, that is, the model conductance decreases continuously during the negative polarity repetitive programming. The experimental results indicate that the state of the memristor of the RS model can be adjusted continuously through a specific range of a continuous programming process.

5. Verification and Analysis

According to [Dong *et al.*, 2018b; Zhao *et al.*, 2019a], the logic implementation has emerged as an important branch of intelligent computing. As a result, the presented TSSM model is introduced into a classical logic implementation [Dong *et al.*, 2018b; Zhao *et al.*, 2019b] for verification purpose. The specific experiment description is provided in the following section.

From Fig. 9, the memristor-only logic circuit is composed of two memristors connected in anti-series. According to [Dong *et al.*, 2018b], the logic circuit is able to realize some double-input and even multiple-input basic Boolean logic operations (e.g. *AND* gate and *OR* gate). Specifically, M_1 and M_2 connected in the input region (labeled by the blue dashed box) are two identical memristors (TSSM model under resistive switching state), whose boundary resistances are denoted by R_L and R_H respectively, i.e. $R_1, R_2 \in [R_L, R_H]$. A and B are two input ports of the circuit, and F is the

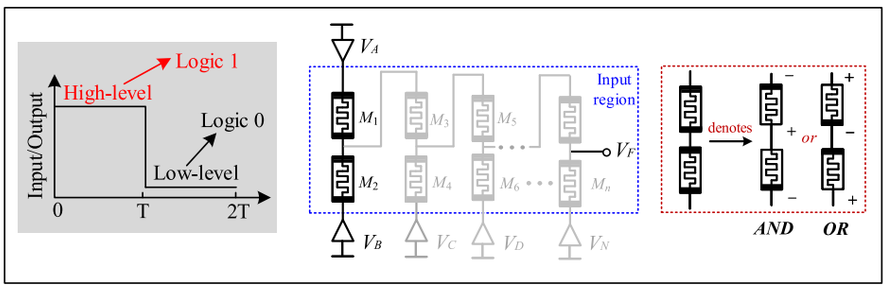


Fig. 9. The memristor-only logic circuit [Dong *et al.*, 2018b]. Notably, the TSSM model in specific logic implementation is under resistive switching state (RS).

Table 3. Overall information of *AND* and *OR* gate operations.

Functions	Truth Table	Input States		Memristances		Output States
		V_A	V_B	R_1	R_2	V_F
AND	$1 \quad 1 \to 1$	V_H	V_H	R_{01}	R_{02}	$V_H \to$ logic "1"
	$1 \quad 0 \to 0$	V_H	V_L	R_H	R_L	$V_L \to$ logic "0"
	$0 \quad 1 \to 0$	V_L	V_H	R_L	R_H	$V_L \to$ logic "0"
	$0 \quad 0 \to 0$	V_L	V_L	R_{01}	R_{02}	$V_L \to$ logic "0"
OR	$1 \quad 1 \to 1$	V_H	V_H	R_{01}	R_{02}	$V_H \to$ logic"1"
	$1 \quad 0 \to 1$	V_H	V_L	R_L	R_H	$V_H \to$ logic "1"
	$0 \quad 1 \to 1$	V_L	V_H	R_H	R_L	$V_H \to$ logic "1"
	$0 \quad 0 \to 0$	V_L	V_L	R_{01}	R_{02}	$V_L \to$ logic "0"

Note: R_{01} and R_{02} are the initial states of the memristors M_1 and M_2 respectively. They are determined by the initial state variable x_0.

corresponding output port. We assume that the voltages applied to ports A, B, and F are V_A, V_B, and V_F respectively. Commonly, the high-level voltage V_H designates the logic "1", while the low-level voltage V_L designates the logic "0". Following voltage divider rule, the output voltage V_F always satisfies:

$$V_F = \frac{R_2}{R_1 + R_2} \cdot V_A + \frac{R_1}{R_1 + R_2} \cdot V_B. \tag{8}$$

Then, taking the binary *AND* operation for example, the specific implementation procedure can be divided into three special cases.

Case a. When $V_A = V_B = V_H$ (high-level voltage V_H means logic "1"), there is no current passing through the logic circuit and the resistances of M_1 and M_2 remain in their initial states. From (8), the output voltage $V_F = V_H$ (representing logic "1").

Case b. When $V_A = V_B = V_L$ (low-level voltage V_L means logic "0"), there is no current passing through the logic circuit and the resistances of M_1 and M_2 remain in their initial states. From (8), the output voltage $V_F = V_L$ (representing logic "0").

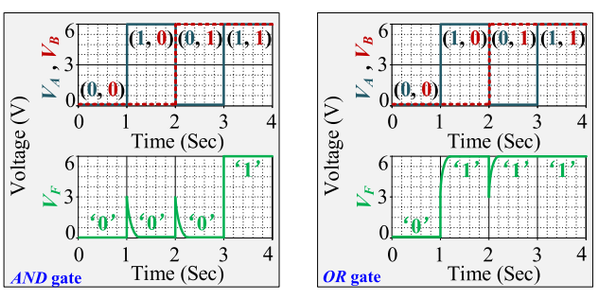
Case c. when $V_A = V_H$ and $V_B = V_L$ (or $V_A = V_L$ and $V_B = V_H$), from (8), the output voltage V_F can be given by:

$$V_F = \begin{cases} \dfrac{R_2}{R_1 + R_2} \cdot V_{\mathrm{H}}, & \text{when } V_A = V_{\mathrm{H}} \\ \dfrac{R_1}{R_1 + R_2} \cdot V_{\mathrm{H}}, & \text{when } V_B = V_{\mathrm{H}} \end{cases} \tag{9}$$

According to the memristance variation rule, the memristance under the high-level voltage will sharply increase to R_H, while the memristance under the low-level voltage will decrease to R_L within a very short time. Then the resulting output voltage can be computed by $V_F \approx R_L \cdot V_H/(R_L + R_H) \approx 0$ which denotes the logic "0".

Similarly, the basic *OR* gate can also be implemented effectively. The overall information of *AND* and *OR* gate operations is collected in Table 3. Furthermore, the corresponding circuit simulation results (conducted in SPICE platform) are exhibited in Fig. 10. Notably, the specific parameter setting (mainly the memristor fitting parameters) is provided in Table 2. Meanwhile, the high-level voltage and low-level voltage are set to $V_H = 6\,\mathrm{V}$ and $V_L = 0\,\mathrm{V}$, respectively.

From Fig. 10, the cyan solid line and the brown dashed line denote the two input voltages V_A and V_B, and the green solid line represents the resulting output voltage V_F. It is clear that the obtained input–output relationship is consistent with the corresponding truth table, which demonstrates the validity and effectiveness of the entire



(a) (b)

Fig. 10. The simulation results for these two basic logic gates: (a) Double-input *AND* gate and (b) double-input *OR* gate.

scheme. Compared with the physical Ag/TiO_x nanobelt/Ti device, the proposed TSSM model can be applied into the memristor-based logic implementation directly, irrespective of strict laboratory conditions, which provides a potential path connecting material science and electronic engineering.

6. Conclusions

This work mainly focuses on the investigation of three-state switchable memristor model (TSSM) based on the Ag/TiO_x nanobelt/Ti configuration, which considers the moisture effect on the resistive switching behaviors and the evolutionary process of memristor. The sufficient accuracy of the TSSM model as compared with the experimental data is achieved by tuning the fitting parameters, exhibiting a root mean squared error of under 0.12%. This model is suitable for Ag/TiO_x nanobelt/Ti device-based circuit design and has been implemented in SPICE simulations. The experimental results demonstrate that the constructed circuit is able to realize basic Boolean logic operations with fast response speed and high efficiency. Further work is needed to incorporate a more physically descriptive model that is humidity-related, and to extend the range of applications of the TSSM model to design a memristor-based network.

Acknowledgments

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