PSPICE Modeling of a Build-in Feedback Automatic –Reactive Power Compensation

M. A. Radi, M. F. Arman, M. K. Darwish, C. C. Marouchos

Abstract – *Over the last few years, the sudden increase of the use of non-linear loads such as personal computers and TV sets created a Power Factor (PF) problem. Although such loads consume relatively small amount of power, however the large number of these loads resulted on huge distortion in the power quality. This paper proposes an automatic reactive power compensation circuit which can generate a leading as well as lagging reactive current. The proposed circuit consists of a build-in feedback system which automatically controls the amount and the type (leading or lagging) of the reactive power required. The compensator is modeled on PSPICE at the component level to illustrate both the transient and the steady state responses.*

Keywords: *Power Factor, Reactive power compensation, Power Factor Correction*

I. Introduction

Since the last decade, reactive power compensation issue has been growing. This is due to the increase in the customer's reactive power electricity bill. In the mean time, fossil fuel prices is growing day by day, which enforces the consumers to minimize energy consumption. To optimize the use of the available apparent power (VA), the flow of reactive power should be eliminated or minimized. Another important term to quantify this problem is the power factor (PF). Its definition is correlated with the phase difference between the voltage and the current in AC circuits. In such circuits, they are supplied by sinusoidal voltage. The PF is represented for linear loads by (cos Φ), where Φ is the angle between the supplied voltage and the line current [1].

Generally, PF is considered as the measurement of how the power is optimized in inductive/capacitive loads. In other words, if the apparent power (VA) available to a customer equals to the real power (W) consumed then the PF will equal to unity (current and voltage are in phase). The main reason for poor PF is that electric circuits accumulate certain energy. This scenario is clearly well known in both linear and non-linear loads. In linear loads the PF is mainly a function of the reactive and resistive components of the load. Such PF can be adjusted/ corrected by introducing appropriate amount of leading or lagging reactive currents. Of course as the load changes the required amount of the reactive currents should also change automatically to maintain a unity or near unity PF. This automatic generation of the reactive current is covered fully in this paper with focus on the

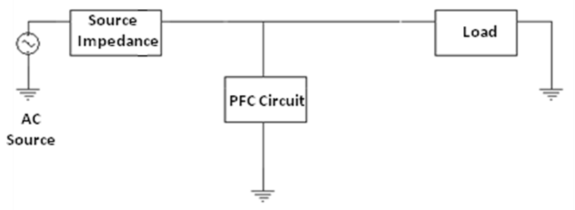

Fig.1. Overview schematic of reactive power compensation

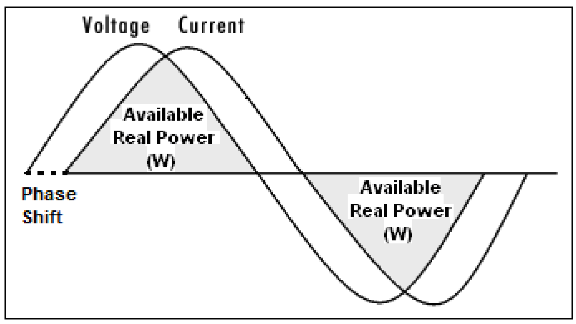

Fig.2. Voltage and current waveform representation

build-in feedback controller. In non-linear loads, the PF is not just a function of the reactive and resistive components but also a function of the non-linearity of the load (diodes; switches; etc.). In such loads PF cannot be just corrected by passive reactive compensators but it also needs active compensators which is outside the scope of this paper and will be discussed in future publication. Fig. 1 illustrates an overview schematic of reactive power compensation. As shown, the power factor correction (PFC) circuit is placed in parallel with the load in order to compensate the reactive power so that the line current is in phase with the supplied voltage. Fig. 2 shows voltage and current waveform representation showing the period for which real power is available (shaded area). It is obvious from this figure that as the current and voltage waveforms shifted away from each other the real power available becomes smaller. Next section (II) illustrates the theory of traditional and automatic reactive power compensators. The PSPICE modeling of both compensators is presented in section III. Sections IV and V contains the discussion and the concluding remarks, respectively.

II. Reactive power Compensation

The difference between apparent (S) and real power (P) is expressed by the “Reactive Power” (Q). The reactive power can be represented as a vector in the power factor triangle as shown in Fig. 3.Q represents the vector length which produces the angle between the apparent and the real power. The difference represents the phase shift between the supplied voltage and the line current [2]. Fig. 3 illustrates the power factor triangle, and the relation between S, Q, and P [3].

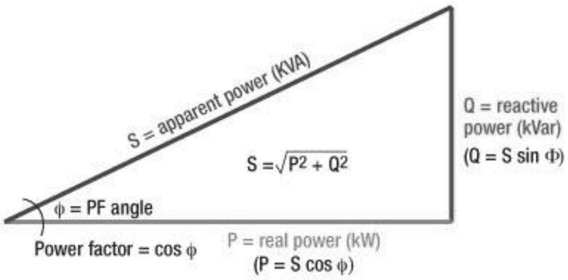

Fig.3. Power Factor Triangle

II.1. Traditional Compensation

The most well known method to handle the problem of the presence of reactive power is based on power capacitors. These compensating passive elements are attractive because of economical reasons, relatively cheap, and simple in operation compared to other compensation means such as active filters [4].

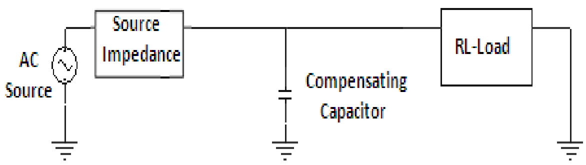

Fig.4. Overview Schematic of fixed PFC for linear load

Traditional PFC is sometimes called fixed PFC in literature [3]. In practice, this method is implemented by connecting power capacitor in parallel with the source system and directly to terminals of a load that has to be compensated as shown in Fig. 4. This connection has the merit of reducing electric grid load, since reactive power is generated at the consumer’s load terminals.

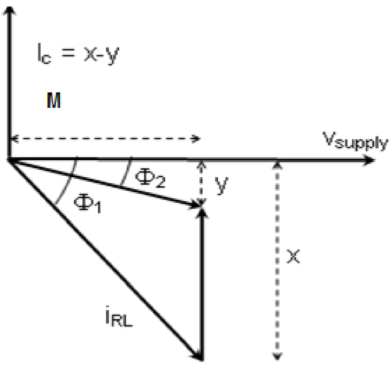

Fig.5. Vector representation for compensated capacitor calculation

In order to find out the value of capacitance to improve the PF to unity, a series of calculation steps is required. An inductive load in series with a resistor (R) is assumed. A proposed algorithm for linear loads is presented as follows [5]:

1- The load inductive reactance (X_L) to be determined, where f is the source system operating frequency in hertz (Hz), and L is the inductance in henries (H).

$$X_L = 2\pi f L \qquad (1)$$

2- Calculate the load’s total impedance (Z).

$$Z = \sqrt{R^2 + X_L^2} \qquad (2)$$

3- The load’s inductive current is computed, where I_{RL} is the current flowing through the load, and V is the supplied voltage.

$$I_{RL} = \frac{V}{Z} \qquad (3)$$

4- Determine the angle (Φ_1) between X_L and R.

$$\phi_1 = \tan^{-1}\left[X_L / R \right] \qquad (4)$$

5- Since the aim is improving the PF to unity, Φ_2 is zero. Inconsequence, the desired capacitive current can be calculated as follow:

$$Sin[\phi_1 - \phi_2] = \frac{I_c}{I_{RL}} \qquad (5)$$

$$I_c = Sin[\phi_1] \times I_{RL} \qquad (6)$$

6- Finally, the compensated capacitance can be determined as follows:

$$X_c = \frac{V}{I_c} \quad (7)$$

$$C = \frac{1}{2\pi f X_c} \quad (8)$$

Where X_c represents the capacitive reactance. Fig.5. shows a vector representation for compensated capacitor calculation [5].

II.2. Proposed Automatic Compensation Circuit

The proposed compensator is constructed from two fast semiconductor switches, and either one or two capacitors. This compensator depends on variable capacitance circuits called Switched Capacitor Circuits (SCC). There is a family of these circuits [6] and two SCC compensators have been investigated in [7].

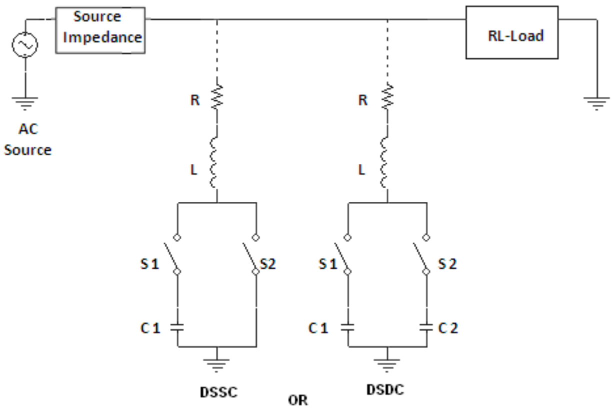

Fig.6. Overview Schematic of the proposed compensators

These are the Single capacitor Double switch (DSSC), and Double capacitor Double switch (DSDC) (Fig.6). DSSC compensator consists of a semiconductor switch (S_1) connected in series with a fixed capacitor (C_1), and another switch (S_2) connected in parallel with the S_1 and C_1.On the Other hand, DSDC compensator consists of two switches (S_1 and S_2) and two capacitors (C_1 and C_2). Each switch is connected in series with a capacitor. S_1 and S_2 are connected in series with C_1 and C_2, respectively. The semiconductor switches can switch on or off at any time and allow the current to flow in any direction as well as it can operate at relatively high switching frequency (10 Khz). High switching frequency is preferred to enhance the spectral performance of the SCCs output. S_1 and S_2 operate in anti-parallel manner so that when S_1 is closed, S_2 is open and vice versa. The operation of the switches is described by a switching function [7] as demonstrated in (Fig. 7).

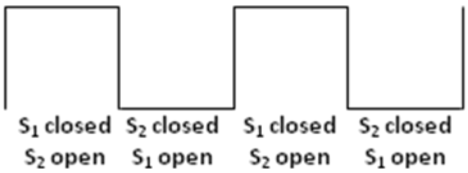

Fig.7. SCC switching operation

The two branches are connected in parallel and the whole combination is connected in series with an inductor (L) as shown in Fig. 6. The resistor shown in the figure represents the internal resistance of the inductor, switches, capacitors, and the wires [6,8,9]. The critical quantity which controls the impedance of the circuit [6] is the duty cycle of S_1 and S_2 in both SCCs. (T_{on}) or (T_{off}) is the time of the pulse during its on or off period, respectively. The duty-cycle (D) can be defined as follows [6,10]:

$$D = \frac{T_{on}}{Pulse\,Period} \quad (9)$$

D is the ratio of the on period to the pulse period where it can vary from 0 (always off) to 1 (always on). In these circuits the inductance remains unaffected and it is the capacitance (C_{eff}) which varies in accordance to the duty-cycle of the switch. In order to determine the effective capacitance for the compensator, the exact calculation algorithm mentioned in the previous section must be followed. After calculating the desired capacitance, the duty-cycle of S_1 and S_2 can be determined to get the C_{eff} using the derived equations for both DSDC, and DSSC. For the DSSC circuit:

$$C_{eff} = \frac{C_1}{D^2} \quad (10)$$

Where C_1 is the fixed capacitor in DSSC compensator. And for the DSDC:

$$C_{eff} = \frac{C_1}{D^2 + \gamma[1-D]^2} \quad (11)$$

$$\gamma = \frac{C_1}{C_2} \quad (12)$$

Where C_1 and C_2 represent the fixed capacitors in DSDC compensator, and γ is the ratio between C_1 and C_2.

II.3. Control method for the proposed Compensator

A control circuit has been designed in order to sense the change in the load and act simultaneously to correct the PF. This is achieved by controlling the duty-cycle of the SCC (Fig.8). The main operation of the feedback loop is to change the duty-cycle of the switches according to any change in the load. Every load's impedance generates its own reactive power and this change in the reactive power requires a range of compensating capacitors values. The fundamentals of the control method depend on the following facts [5]:

1- Any change in the load's impedance will either draw more or less current (I_{RL}) into it.
2- This I_{RL} is in the form of an AC signal. This waveform is to be rectified into a DC signal as shown in Fig.9.
3- An OpAmp comparator is used to find the intersection between the rectified I_{RL} and a saw-tooth signal.
4- The result will be a train of pulses where its duty cycle depends on the value of the input I_{RL}. These pulses are fed into the compensator's switches.

Fig. 10 shows the inversely proportional relationship between the rectified I_{RL} and the duty-cycles of the switches. This is due to the nature of the saw-tooth triangles shape. The higher the duty cycle the lower the C_{eff} , as seen in (10) and (11) for both DSSC, and DSDC compensators, respectively.

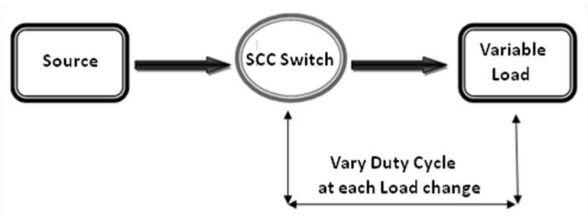

Fig.8. Chart flow of the proposed control method for SCC compensator

III. Simulation Results

In order to verify the proposed compensator and its control method, the circuits are simulated using Orcad PSPICE 16.3. Both traditional and automatic compensators are simulated in order to validate the proposed system.

III.1. Traditional Compensator results

An inductive linear load has been simulated for traditional reactive power compensation. The load consists of an inductor (30mH), and a resistor (25 Ω). Fig. 11 shows the result of the simulated inductive circuit.

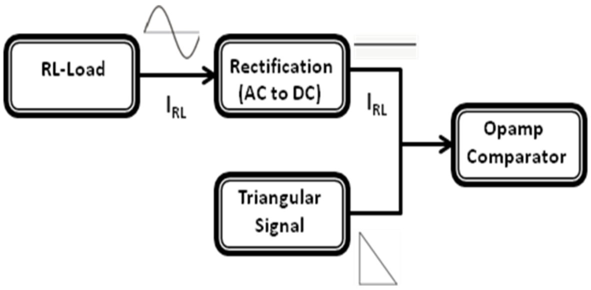

Fig.9. Detailed chart flow of the proposed control method

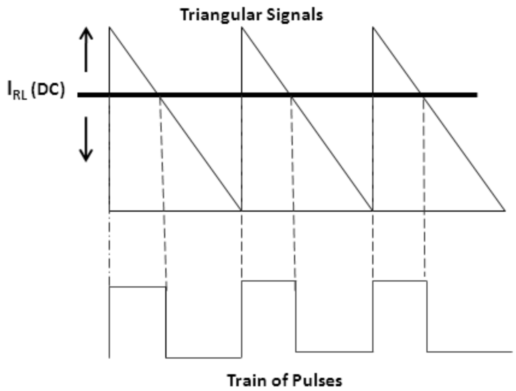

Fig.10. The comparator intended function in the control Process

The phase shift is seen clearly between the current and the supplied voltage. The current is lagging the voltage by 45 degrees. Fig. 12 illustrates the reactive power compensation using a fixed capacitor. The current and the voltage are in phase where the PF is nearly unity. The calculated value of the compensating capacitor is 42.55 microfarads (μF).

III.2. Automatic Compensator results

The same inductive load values are used in the proposed compensator simulation. By controlling the duty-cycle of the SCC compensator, the desired C_{eff} is set automatically. For the DSSC compensator, the calculated D is 0.5 for S_1 and inconsequence it is 0.5 for S_2 (anti-parallel switches). In other words, S_1 will be turned on for half of the cycle's period and S_2 will be turned off for the rest of the period. A fixed capacitor (C_1) of 10uF is being used for DSSC circuit. Fig. 13 shows the simulated results for the DSSC compensator. On the other hand, the calculated D for DSDC compensator is 0.7 and 0.3 for S_1 and S_2, respectively. S_1 will be turned on for 70% of the cycle while S_2 will be turned off for the rest 30% of the cycle. Two capacitors of 20μF and 100μF are used in series with S_1 and S_2, respectively. An inductor of 10mH is inserted to act as current limiter for both SCC

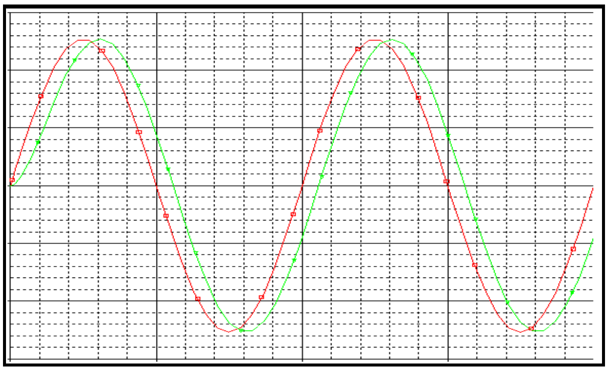

Fig.11. The current is lagging the voltage by 45 degrees.

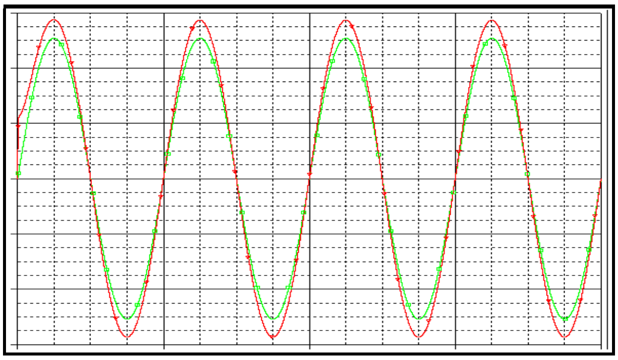

Fig.12. The current and the voltage are in phase after adding a compensated fixed capacitor.

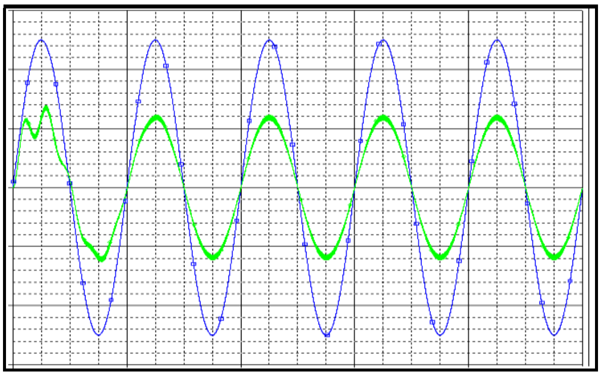

Fig.13. Reactive power compensation using SCDS compensator

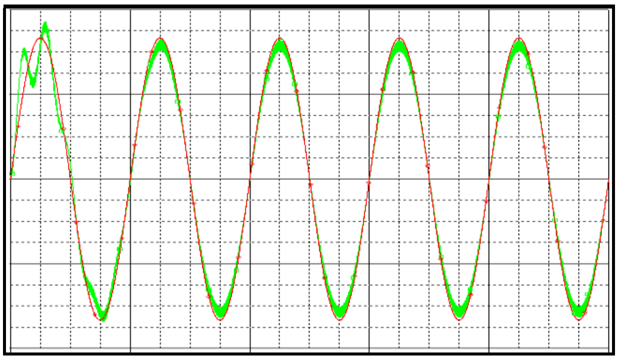

Fig.14. Reactive power compensation using DCDS compensator

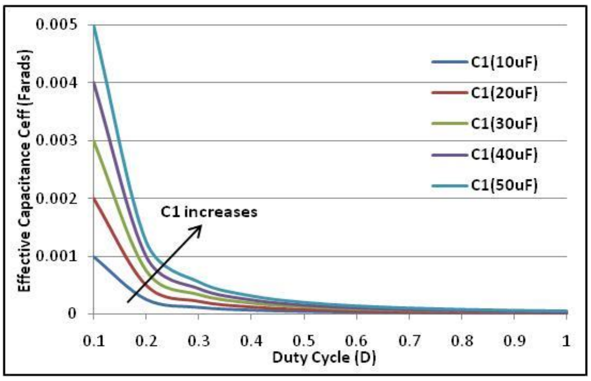

Fig.15. Relation between D and C_{eff} for SCDS compensator

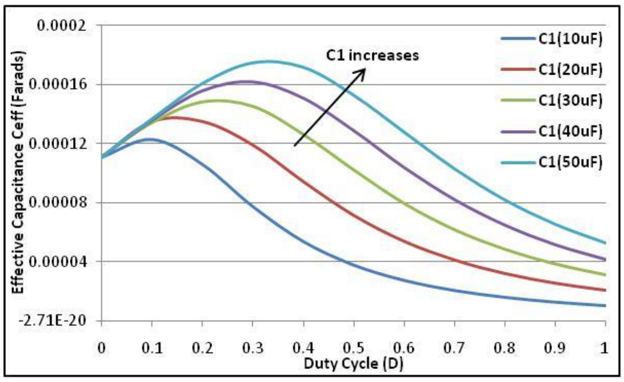

Fig.16. Relation between D and C_{eff} for DCDS compensator

compensators. Fig. 14 illustrates the nearly zero phase angle between the current and the supplied voltage in DSDC compensator. Fig. 15 and 16, display the relation between D and C_{eff} for the two compensators.

III.3. Automatic Compensator Control results

A control method for SCC compensators is simulated using PSPICE software package. The results show a good agreement of duty-cycles to compensate any reactive power within any change in the load. This control method is implemented on DSDC compensator. The duty-cycles are automatically calculated for three different RL-load impedances. Fig. 17 illustrates the result for correcting the PF for a load with R=13Ω, and L=42mH. This phase angle is corrected from 45 degrees to nearly zero. The same results is shown in Fig. 18 but for a load with R=63 Ω, and L=200mH. The correction is applied for the same phase shift.

IV. Discussions

Automatic SCC reactive power compensators are proposed with their control technique. The traditional and

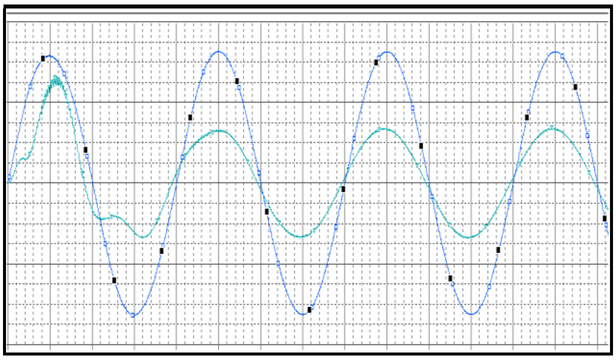

Fig.17. DCDS compensation for RL-load, R=13.4ohms, L=42mH

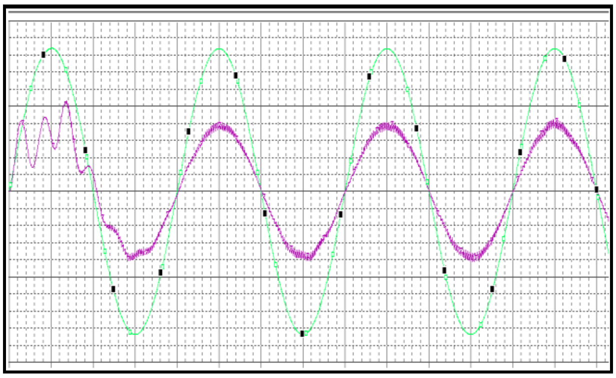

Fig.18. DCDS compensation for RL-load, R=63.04 ohms, L=0.2 H

automatic compensators are simulated and showed a clear agreement on correcting the PF effectively. The traditional (Fixed C) has the advantages of low number of components, easy of connection and simple operation. At the same time the fact that a single capacitor with a fixed value is used, under-compensation or overcompensation might occur. The problem is partly solved by the use of a number of capacitors where their combination gives smooth control of the available PF correction where this adds to complexity. The proposed method superiority is clearly shown in its automatic capability, ability of producing both leading and lagging current behaviors, and its ability to be used as an active filter. The proposed design may suffer from high number of components, and complexity in operation compared to the traditional method. But exact PF correction is possible at wide range of load variation. Both DSSC and DSDC compensators are able to provide the desired PF correction.

V. Conclusions

Automatic power factor compensation is developed which can be used in linear and non-linear loads. The proposed compensator can be used in shunt in conjunction with all types of loads. The compensator uses relatively fast semiconductor switches and the voltage and current ratings for such devices is still limited to low power applications. The reactive power compensators are simulated and compared with the traditional techniques. SCC compensators generate the required reactive power which is needed to improve the power factor for inductive loads. The main advantage of the system is its ability to generate smoothly variable leading as well as lagging reactive power using only one or two capacitors and two switches. This is achieved through controlling the duty-cycle of the semiconductor switches. A control method is proposed to provide a practical application of the SCC compensators. Future work will include an investigation in non-linear load applications, resonance phenomena, distortion and practical implementation.

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