The Teaching of Switched Mode Power Supplies – Design, Simulation and Practical Implementation for Undergraduate and Postgraduate Students

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***Abstract*— The teaching of switched mode power supplies can be very challenging. For example, do we just teach the operation of the power supplies? Is teaching a topology enough to produce a graduate capable of designing power supplies for the highest specifications? Should we consider other details like EMI, thermal effects and packaging in the design? What will happen if we ignore them? Should these details be considered at the simulation stage, or only when it comes to manufacturing phase? This paper covers all the steps required for the design procedure of switched mode power supplies. The paper can be used in developing practical/simulation courses in power electronics for teaching the design of switched mode power supplies.**

Keywords—Teaching power electronics; switched mode power supplies

I. INTRODUCTION

Power electronics is a multi-discipline branch and it deals with variety of interrelated topics like power distribution, protection, FACTS, HVDC systems, Electric Vehicles, energy storage systems, etc. In the heart of all these interrelated topics lies on a semiconductor switch (Thyristor, MOSFET, IGBT, etc.). When it comes to the simulation of power electronic circuits some people just consider the semiconductor switch as an ideal switch with zero resistance when ON ($R_{on} = 0$) and infinite resistance when OFF ($R_{off} = \infty$). Some others assume small value for R_{on} and large value for R_{off} to emulate the conduction and off losses in the semiconductor switch. Of course, there are also many simulation packages where a particular semiconductor switch can be picked up from the library with characteristics very close to the real semiconductor switch. When teaching power electronics, which level do we go for? Do we assume 'ideal' switch, 'semi-ideal' switch, or a library model for the exact switch characteristics? How important the switching losses and conduction losses when simulating general power electronic circuits? In this paper, switched mode power supplies are selected as examples for simulating power electronic circuits. The switched-mode power supplies are excellent examples to demonstrate the effect of all types of losses on power electronic circuits. First, a general review of switching and conduction losses is presented and then the effect of each one is tested on a boost converter with a single MOSFET switch controlling the power to a load. The load could be inductive or purely resistive load; it does not make much difference as the FWD will conduct during the turn off time of the switch. These losses are analysed for a MOSFET switch at different operating conditions.

II. LOSSES IN SEMICONDUCTOR SWITCHES

Losses in semiconductor switches can be divided into four main categories:

1) Switching loss.

2) Loss during forward conduction.

3) Loss associated with leakage current.

4) Loss occurring in the gate circuit.

The switching loss can be divided further into switching 'on' loss and switching 'off' loss. The value of this loss depends on the turn-on and turn-off times of the switch but most importantly, it depends on the switching frequency. The switching loss in MOSFETS for example is much lower than the switching loss in BJT and this is due to the smaller turn-on and turn-off times in MOSFETS.

The forward conduction loss is mainly due to the voltage drop across the switch multiplied by the current through the switch during the 'on' time. It should be noted that in MOSFETs the internal (dynamic) resistance between drain and source during on state, $R_{DS(ON)}$, limits the power handling capability of MOSFETs. Hence, MOSFETs have high 'on' losses especially for high voltage device due to $R_{DS(ON)}$.

Smaller semiconductors have thinner insulating layers, causing more leakage current. This leakage current multiplied by the voltage across the switch generates loss which is associated with leakage current.

The 4th type of loss is the loss occurring in the gate circuit of semiconductor switches. Gate charge loss is a power loss ascribed to MOSFET gate charging. This is usually very small in comparison with the other three types of losses.

Fig. 1 illustrates the loci diagram of 'v' against 'i' at equal and unequal turn-on and turn-off times. In the following section, the switching losses in a single MOSFET switch are studied in more details.

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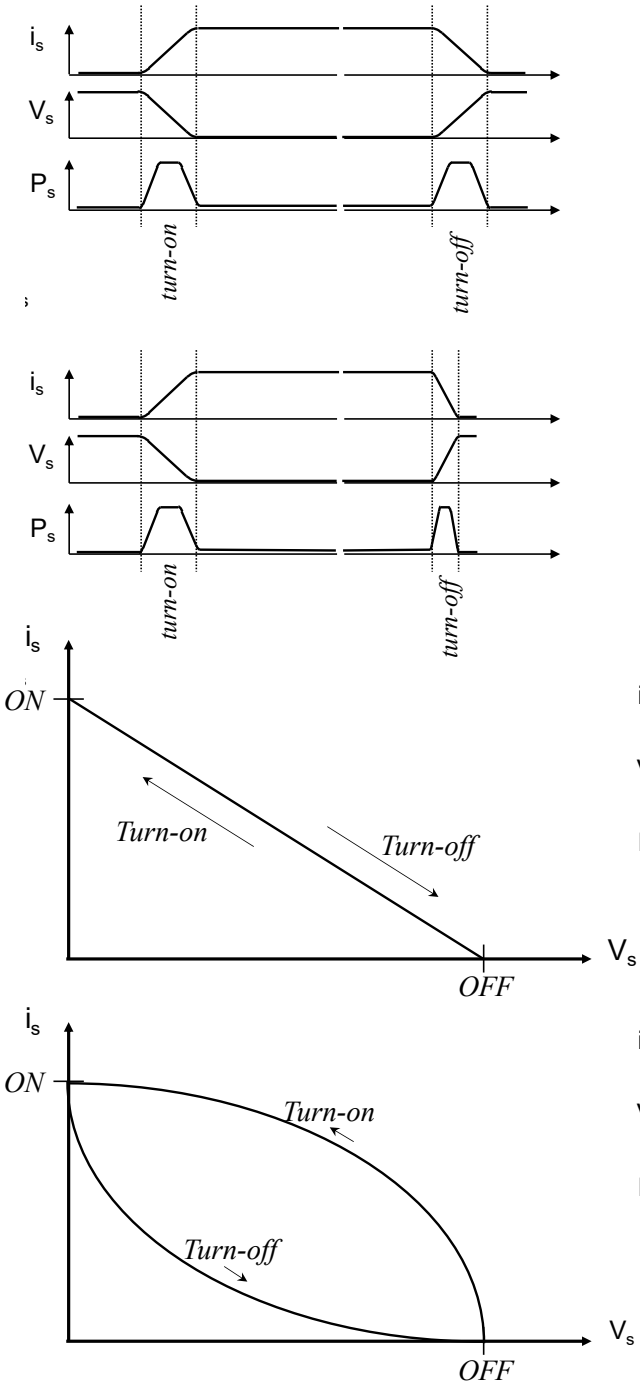

Fig.1: loci diagram of 'v' against 'i' at equal and unequal turn-on and turn-off times

III. SWITCHING LOSSES IN A SINGLE MOSFET SWITCH

Fig. 2 shows a boost converter with a MOSFET switch IRFZ34. The switch is rated at the following values;

V_{DS} = 60V, I_D = 30A, $R_{DS\ (on)}$ = 0.028 Ω. This is a relatively low voltage high current MOSFET and will be used in the rest of this paper. Other semiconductor devices can be equally used to for the same purpose; however, the same switch should be used in all case studies.

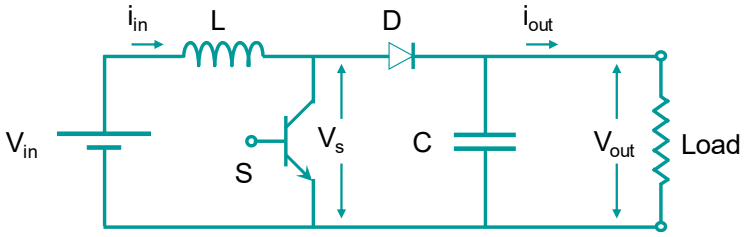

Fig.2: The boost converter topology under study

The boost converter is tested for different switching frequencies (10 kHz, 20 kHz, 40 kHz, and 80 kHz). The value of the inductor and capacitor are evaluated for each switching frequency in order to minimise the value of the inductor current using the usual boost equations:

$$L_{\min} = \frac{D(1-D)^2 R}{2f} \quad and \quad C = \frac{D}{R f \left(\frac{\Delta V_{out}}{V_{out}}\right)}$$

Where R is the load, D is the duty cycle, f is the switching frequency and $\Delta V_{out}/V_{out}$ is the output ripple voltage. The minimum value of the inductor is increased by 25% to ensure continuous mode of operation.

Where. Fig. 3 shows the overall losses of the switch (conduction and on-losses). However, since the switch duty cycle is kept the same (50%), the conduction losses is the same for all cases of different switching frequencies, and Fig. 3 can then present the relative switching losses at different switching frequencies. It is obvious from Fig. 3 how the switching frequency contributes largely to the switching losses. In fact, teaching power electronics with an ideal switch could be very misleading unless the emphasis is on the principles of operation of the circuit.

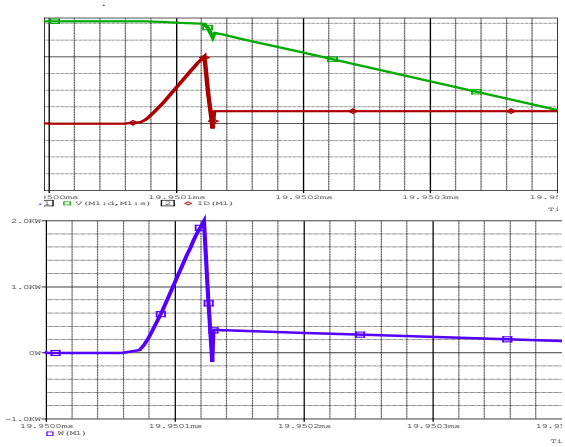

Fig.3: Current and voltage (top) and power (bottom) during turn-on time

Fig. 4 illustrates the losses vs the switching frequencies. The duty cycle is kept at 50%. The switching frequency is varied on OrCAD using the 'PARAM' from 5 kHz to 1 MHz. It can be shown in that figure that the switching losses becomes almost constant above 500 kHz. The relationship between the switching losses and the switching frequency is not a linear relationship. The selection of the operating switching frequency in a switched mode power supplies may reduce the size of the magnetics (inductors, transformers), but it increases the switching losses. Students at final year and MSc should be able to find out the optimum switching frequency for a specific application.

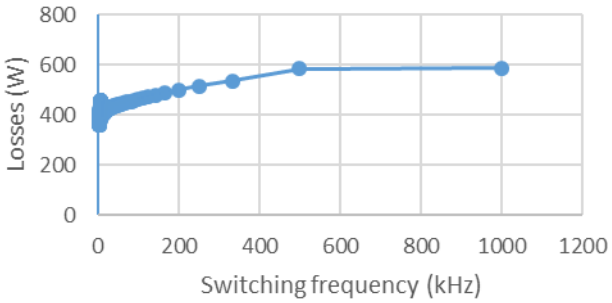

Fig.4: Losses vs switching frequencies

IV. Conduction Losses in a Single MOSFET Switch

The conduction losses are evaluated for the same switch in the same boost converter. The switching frequency stayed the same but the switch duty cycle is varied. The idea here is to look at the conduction losses while keeping the switching losses at constant value. Fig. 5 shows the circuit used in simulating the conduction losses. The PARAM was used here to control the switch duty cycle from 0 to 0.8. Above this value the internal resistor of the inductor in the boost converter limits the operation of the circuit and hence the choice of 0.8 duty cycle as a maximum value. Fig. 6 shows the conduction losses vs the duty cycle at different switching frequencies. It can be seen that the conduction losses almost increases linearly with the duty cycle. There is a jump in the overall losses between 20 kHz and 100 kHz as expected.

After covering the losses in semiconductor switches, the question now is what do we do with these losses?

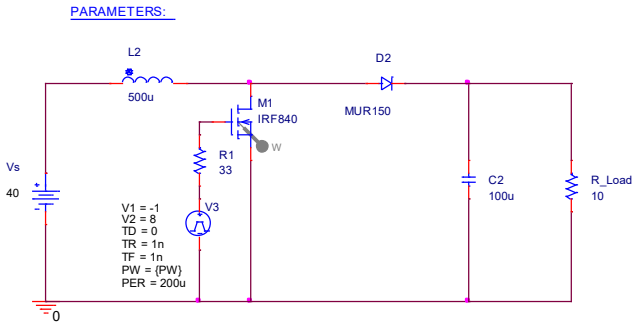

Fig.5: Circuit to evaluate losses at different duty cycles

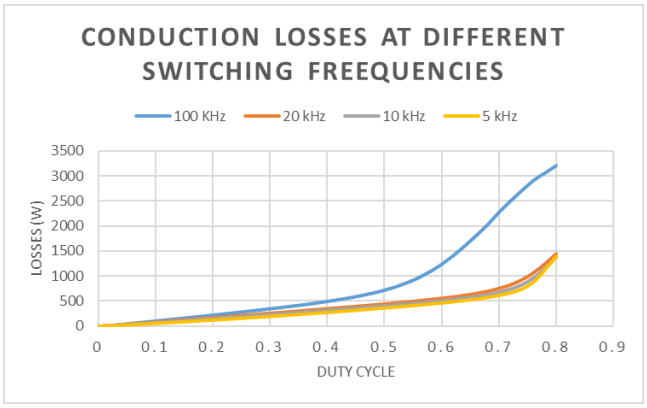

Fig.6: Conduction losses vs the duty cycle at different switching frequencies

V. Protection of the Switches

The switching losses could be diverted and dissipated in external resistance and hence removing the stress from the switch. That can be done by using turn-on and turn-off dissipative snubber circuits. This could be taught at final year of undergraduate programme. The switching energy can also be feedback to the supply instead of wasted in external resistor by using energy-efficient snubber circuit. This could be taught at postgraduate level. There are many types of dissipative snubber circuits and the main principles is to develop voltage across a series inductor during the turn-on time equal to the input voltage and hence leaving the switch with almost zero voltage across it. During the turn-off a parallel capacitor is used to divert the current during the turn-off time. In both during the turn-on and turn-off times the energy stored as a current in the inductor or stored as a voltage across the capacitor should be dissipated quickly before the next cycle of the turn-on or turn-off times. An external resistor with an appropriate value is used to dissipate this energy. Fig. 7 shows a combined turn-on / turn-off snubber circuit which can be used in such applications.

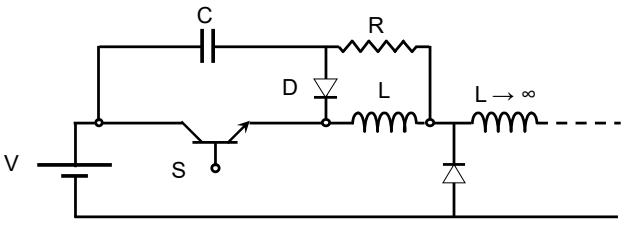

Fig.7: A combined turn-on / turn-off snubber circuit

The values of the snubber inductor and snubber capacitor can be calculated as follows:

- Initially no current flows in 'S' and the small snubber inductance 'L'. As the current through 'S' rises during the rising time (t_r) a voltage V_L=L di_s / dt is developed across L.
- Assuming that is increases linearly with t, we find that V_L=L I / t_r .
- If we choose L so that V_L=V there will be zero voltage developed across S during t_r , giving zero turn-on loss in the switching device.
- Energy of ½LI^2 is stored in L and must be removed (during t_{off}) so that the snubber is reset by the start of the next cycle. Resistor and a diode are used to dissipate the energy as heat.
- The value of 'R' is not critical, but two factors restrict it:
  - The time-constant L/R must be short enough that the current can decay sufficiently during t_{off}.
  - Immediately after 'S' has opened it sees a voltage 'V+IR' across it. The voltage rating of 'S' must therefore be increased withstand such voltage.
- The power dissipated in 'S' during ton is ideally zero. The power dissipated in 'R' is simply the stored energy multiplied by the switching frequency (1/T).
- P_R = LI^2 / (2T) (Note that P_R is independent of 'R')
- If 'L' is smaller than its optimum value, some power will be dissipated in 'S' but correspondingly less will be dissipated in 'R'.
- The total loss $P_{s(on)}$ + P_R remains the same.
- If 'L' is larger than its optimum value, the power dissipated in 'S' stays at zero while the dissipation in 'R' increases. This is illustrated in Fig. 8.

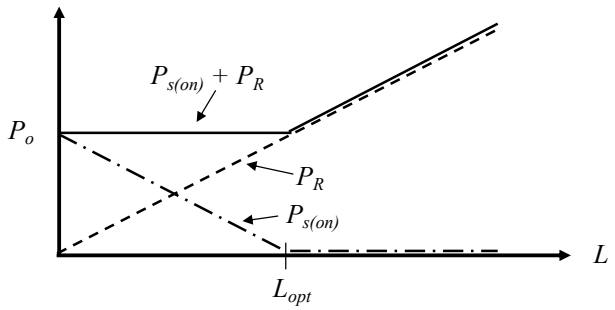

Fig.8: Optimum value of snubber inductor

For the turn-off snubber, energy of (½ CV^2) is stored in C and must be removed (during ton). The simplest way to do this is to add diode and resistor to the snubber. The same turn-on snubber resistor can be used. The voltage across C decays exponentially when the switch is closed. Again, the value of R is not critical, but two factors restrict it:

- The time constant CR must be short enough that V_c can decay to a negligible value during ton . (3 time-constants will be sufficient)
- Immediately after the switch closes, it passes a current of (I+V/R) greater than the snubbed current, I. The current rating of S must therefore be increased relative to the un-snubbed case.
- Choose $C_{opt(1)}$ to minimise the total turn-off loss.
- $C_{opt(1)}$ = 0.22 I t_f /V
- Choose $C_{opt(2)}$ to minimise the loss in the switch without increasing the total loss above P_0 .
- $C_{opt(2)}$ = 0.91 I t_f /V. This is illustrated in Fig. 9.

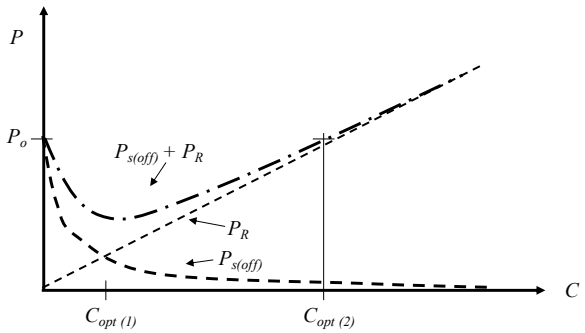

Fig.9: Optimum value of snubber capacitor

For postgraduate students energy efficient snubber circuits can be introduced. The aim of energy-efficient snubbing is to improve the overall efficiency of the converter. For the turn-on an energy recovery winding is added to the snubber inductor to demagnetise it and feed energy back to the supply. In the case of turn-off snubber circuit, a small auxiliary DC-DC converter is used in place of the discharge resistor to feed the energy stored in the snubber capacitor back to the supply. This could be a bit complicated as students should be very familiar with the transient response during the turn-on and turn-off times. Turn-on energy efficient snubber circuits is shown in Fig.10. The student at this stage should be familiar with the energy recovery mechanism in order to appreciate how the energy stored in the snubber inductor can be fed back to the DC sourse with minimum losses.

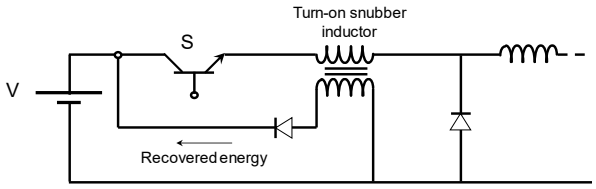

Fig.10: Energy recovery turn-on configuration

Turn-off energy efficient snubber circuits is shown in Fig.11. In fact an auxiliary DC/DC converter can be used to recover the energy stored in the snubber capacitor and feed this energy back to the DC source again with minimum losses. The rating of auxiliary DC/DC converter is much smaller than the main boost converter.

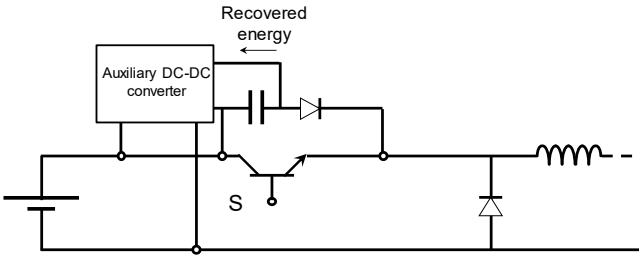

Fig.11: Energy recovery turn-off configuration

VI. Design Parameters in Switched Mode Power Supplies

An important factor in teaching switched mode power supplies is the effect of either over calculating or under calculating the inductor value. Another important factor is the choice of the switching frequency. Through simulation, the student should discover how under calculating the inductor value could lead to the discontinuous inductor current. Also what is the effect of the switching frequency on the continuity of the inductor current? What is the effect of the load? Figs12-14 illustrates the effect of all three factors.

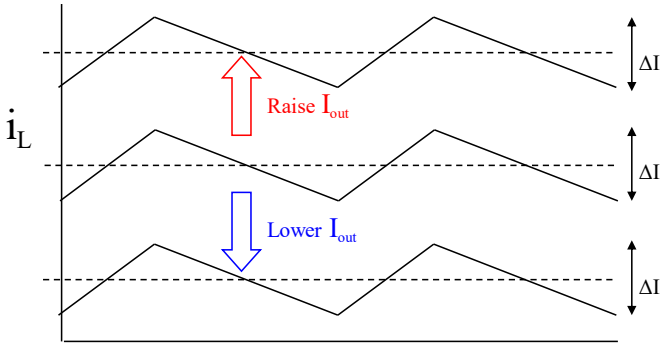

Fig.12: Effect of raising and lowering I_{out} while holding V_{in}, V_{out}, f, and L constant

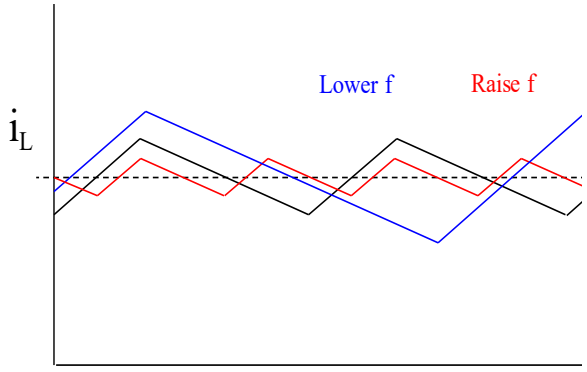

Fig.13: Effect of raising and lowering f while holding V_{in}, V_{out}, I_{out}, and L constant

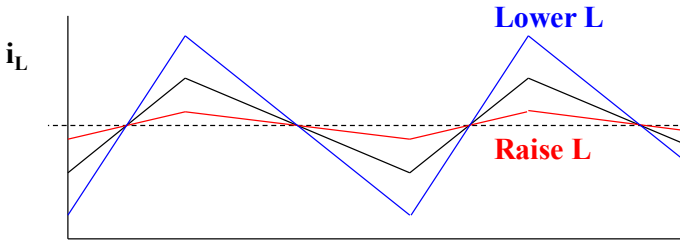

Fig.14: Effect of raising and lowering L while holding V_{in}, V_{out}, I_{out} and f constant

Table 1 shows how different points can be covered in which level when teaching switching mode power supplies.

Table 1: Teaching switched mode power supplies

	Level 1	Levels 2&3	MSc
Semiconductor switch	It can be taught as very low or very high resistor	A library model can be introduced	A library model with temperature characteristics
Dissipative snubber circuits	A simple RC snubber can be introduced	How to design a snubber circuit can be introduced	Optimisation of snubber values can be introduced
Energy efficient snubber circuits	-	-	Can be an interesting assignment topic
Considering internal resistance of inductance	-	The students should be aware of it.	Can be an interesting assignment topic

VII. CONCLUSIONS

Teaching switched mode power supplies could be very challenging. This paper focuses on the effort to teach students the design of power electronics converters at different levels. In this paper, different aspects of switching losses and switch protection are covered together with the design parameters in teaching power supplies for undergraduate and postgraduate levels. It is important to use the simulation tools to show the effect of changing different variables.

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