Development of Alternative Pulse Width Modulation Methods for Conventional and Multilevel Voltage Source Inverters

A thesis submitted for the degree of

Doctor of Philosophy

by

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Abstract

Multilevel inverters have attracted wide interest in both the academic community and the industry for the past decades. Therefore, the investigation and development of modulation strategies in multilevel inverters emerges as a necessity for the industry and researchers.

In this doctoral thesis, alternative modulation methods suitable for three-level conventional single-phase inverters and especially for cascade H-bridge multilevel inverters are discussed and proposed. The theory of Equal Areas is reformed and presented and its modifications are proposed. These modifications are compared with other well-known modulation schemes, such as carrier-based modulation schemes and programmed pulse width modulation techniques.

The advantage of the modified Equal Areas Pulse Width Modulation (EAPWM) is its algorithmic simplicity due to simple algebraic relationships, which results in less computational effort. A fully mathematical formulation for the Equal Areas modulation is proposed for both conventional and multilevel inverters. The EAPWM is shown to produce well-formed switched output voltages that have low total harmonic distortion at even low switching frequencies. The importance of this thesis is complimented by the results, produced after the implementation of EAPWM in multilevel inverters, which can be used as a more accurate reference when compared with other modulation strategies. Moreover, this direct modulation strategy has been extended to work on higher

amplitude modulation ratios, in a linear manner, while entering the over modulation region. In this context, modified algorithms have been developed using different criteria for the calculation of the pulses' width and their placement inside the time interval. The equal areas method, implemented in conventional single-phase inverters, uses odd pulse numbers per half cycle, holding integer frequency ratios in contrast to its implementation in multilevel inverters, where non-integer frequency ratios occur due to the level-by-level application.

The application of the method is verified by simulations together with experimental work using a full-scale prototype inverter.

Acknowledgements

First, I would like to express my deepest appreciation to my Supervisor Professor Dr. Mohamed Darwish whose continuous support, professionalism and ethos have helped me greatly in successfully completing my dissertation. Additionally, I would like to thank my Professor at Technical Educational Institute of Athens (T.E.I of Athens) Dr. Drosos Nafpaktitis, whose useful advice and guidance has assisted in completing my theoretical and experimental work.

Even though I cannot list here all the people with whom I had the pleasure to work, and discuss around the coffee table, I dare to mention a few exceptional colleagues. Especially, I should express my gratitude to Dr. Gregory Koulouras, Dr. George Hloupis and Mr. Dimitris Lorentzos. Your active support is deeply appreciated.

Here, I would like to give a big thank you to all of my friends for their psychological support during this long journey of this thesis. Especially Kostis Grimanis who helped me, putting words in the right order, and enabled me to make the text readable and bring my thoughts and ideas into hopefully, an understandable format.

Last but not least, I deeply thank my beloved family, my mother, father and brother and notably my uncle Filimon who passed away during this journey. Their unconditional love and warmth played a huge part in what I have become today.

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Nomenclature

A_p	Number of pulses-intervals in half-period
A_{p1}	Number of pulses-intervals in 1st level in MLI
A_{pe}	Number of pulses-intervals in the *e* level of a MLI
$b_{(n)}$	Amplitude of the nth harmonic
C	Capacitance
d	Duration of the time interval
d_e	Duration of the time interval in the e level of a MLI
D_e	Duration of the *e* level of a MLI during the 1st quarter of f_0
E	Number of sources in MLI
f_0	Fundamental frequency
$f_s=f_{sw}$	Switching frequency
f_p	Phase-leg switching frequency
J	Number of interval
L	Inductance
m	Number of levels of a MLI
m_a=DF	Amplitude modulation ratio/ Duty Factor
$m_f=fs/f_0$	Frequency modulation ratio
n	Number of harmonic
T	Fundamental Period

t_δ	Inactive time interval between PWM pulses
t_P	Active time of a PWM pulse
t_{pJ}	Pulse active time in J interval
$t_{\varepsilon J}$	Firing time for the pulse of J interval
t_k	Firing and closing time of a PWM pulse
t'_e	fundamental firing time for the switched e level
$U_{max}=U_{sin}=V_{max}$	Amplitude of the sinus reference waveform
$U_{pmax}=U_{pulse}$	Amplitude of the PWM pulse
U_{pmm}	Marginal amplitude of the PWM pulse
$U_{dc}=V_{dc}$	DC link voltage
U_{grid}	Amplitude of the target voltage
U_{rms}	Rms voltage of the PWM voltage output
$U_{(n)}$	Amplitude(rms) of the n^{th} voltage harmonic
$V_{1,rms}$	Amplitude of the fundamental rms voltage
THDn	Total Harmonic Distortion until the n^{th} harmonic
THDrms	Total Harmonic Distortion calculated using rms values
EAPWM	Equal Areas Pulse Width Modulation
EMI	Electro Magnetic Interference
APOD	Alternative Phase Opposition Disposition
POD	Phase Opposition Disposition
PD	Phase Disposition
MLI	Multilevel Inverter

CHAPTER 1

Introduction

1.1 Scope

The scope of this thesis is to present the results obtained in the PhD project "Development of *Alternative Pulse Width Modulation for Conventional and Multilevel Voltage Source Inverters*" performed by the author during the period September 2011 to June 2016. Most of the scientific results obtained have been already published in journal papers. The published papers are included at the end of this thesis. The outcome of this research is the proposition of a new PWM method that has been implemented in two different level (3-level and 7-level) prototype inverters, along with their simulation and practical results.

The objective of this thesis is to contribute in the existing field of PWM methods in power inverters. More specifically, it addresses and analyses the advantages and disadvantages along with the problems and limitations that may occur in carrier-based and programmed PWM methods. Furthermore, an alternative PWM method is proposed in the direction of limiting drawbacks of the existing solutions. In addition, the proposed method, can be applied both to conventional and multilevel inverters.

1.2 Background and Motivation

In the past years plenty of topologies of DC/AC inverters have been created. The need to produce voltage control for adjustable frequency loads along with the concept of regulating the switched state of power electronic devices to achieve this control unfortunately can only be accompanied by undesirable harmonics, as a result of the inherent switched nature of modern power electronic equipment [1].

The development and evolution of DC/AC power converters in energy systems, along with the rising penetration of the Multilevel inverters technology in the industrial applications, renewable energy systems and generally in high-power medium-voltage energy control, indicates the need for improvement of the converter performances. These improvements may include the optimization of power quality, the rising of the nominal power of the converters, the control simplification and the performance of different algorithms in order to improve the Total Harmonic Distortion (THD) of the output signals. Nowadays it is noted that, more and more researchers are focused on the harmonic elimination using pre-calculated switching functions to improve the harmonic content of the output as demonstrated by the THD factor and therefore the power quality. Given these facts it is obvious that the background and motivation of this work arises from the emerging need for optimizing and re-approaching the PWM methods regarding the harmonic content, the minimizing of computational effort needed and other factors such as switching power losses and filter sizing of the output.

1.2.1. Harmonics in Electrical Systems

One of the most considerable problems in power quality aspects is the harmonic contents in an electrical system. Electrical systems are designed to operate at a fundamental frequency of 50 or 60Hz. However, certain types of

load such as resistive load, capacitive load or inductive load, produce currents and voltages that are integer multiples of the fundamental frequency. These higher frequencies can be considered as a form of electrical pollution and are known as power system harmonics [2].

Generally, harmonics can be divided into two types: 1) voltage harmonics, and 2) current harmonics. Voltage and current harmonics imply power losses, Electromagnetic Interference (EMI) and pulsating torque in AC motor drives. Both types of harmonics can be generated by either the source or by the load side. Current harmonics are usually produced by harmonics contained in voltage source supplies and depend on the type of load. Nowadays, the most common sources of harmonics are generated by power electronic loads such as adjustable-speed drives (ASDs) and switch mode power supplies. In the case of ASDs, the DC is then converted to variable-frequency AC to control motor speed. These power electronic loads generate harmonics due to nonlinear operation of diodes, silicone-controlled rectifiers (SCRs), power transistors, and other electronic switches which are used to chop waveforms to control power or to convert 50/60 Hz AC to DC [3]. On the other hand, these loads offer tremendous advantages in efficiency and controllability due to which they can be found from low voltage appliances to high voltage converters. It is obvious, that these undesired power systems harmonics are an important problem that has to be addressed. In this thesis, the harmonics problem will be addressed on the converters and voltage source inverters (VSIs) aspect.

1.2.2 Harmonic Distortion Factor

In order to consider the degree to which the undesirable harmonics are created during the process of voltage control, basic performance indices have been developed which quantify the harmonic distortion. Various converter modulation algorithms appeared over the years. One way to compare the effectiveness of one method over another is to compare the unwanted components, i.e. the distortion in the output voltage or current waveform

relative to that of an ideal sine wave [1]. Given that the output voltage of a converter *v(t)* is a periodic function with period *T* the root-mean-square (RMS) value of the function is:

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T v(t)^2 dt} \qquad (1.1)$$

Since *v(t)* is periodic, then it can be represented by Fourier series

$$v(t) = V_0 + V_1 \cos \omega_1 t + V_2 \cos 2\omega_1 t + V_3 \cos 3\omega_1 t + ... \quad (1.2)$$

Whereupon

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T \sum_{n=0}^{\infty}\sum_{k=0}^{\infty} V_n V_k \cos n\omega_1 t \cos k\omega_1 t dt} \quad (1.3)$$

Upon expanding, the integration of terms in which $n \neq k$ become zero and the double- frequency term integrates to zero over a complete period so that finally,

$$V_{rms} = \sqrt{V_0^{\,2} + \sum_{n=1}^{\infty} \frac{V_n^{\,2}}{2}} \quad (1.4)$$

Or in terms of RMS values of the individual harmonics

$$V_{rms} = \sqrt{V_0^{\,2} + \sum_{n=1}^{\infty} V_{n,rms}^2} \quad (1.5)$$

If the fundamental component is the desired output the reminder of this expression is then considered as the distortion. Factoring out this desired component gives

$$V_{rms} = V_{1,rms}\sqrt{1 + \left(\frac{V_0}{V_{1,rms}}\right)^2 + \sum_{n=2}^{\infty}\left(\frac{V_{n,rms}}{V_{1,rms}}\right)^2} \quad (1.6)$$

One can conclude to an expression of the total harmonic distortion factor (THD) of the voltage, which is defined in terms of the amplitudes of the harmonics V_n.

$$THD = \sqrt{\left(\frac{V_0}{V_{1,rms}}\right)^2 + \sum_{n=2,3,\ldots}^{\infty}\left(\frac{V_{n,rms}}{V_{1,rms}}\right)^2} \qquad (1.7)$$

And the RMS voltage becomes

$$V_{rms} = V_{1,rms}\sqrt{1+THD^2} \qquad (1.8)$$

It easily noted that the RMS value of the waveform is equal to the fundamental RMS if THD is equal to zero. Solving the last equation eq.(1.8) for the THD an alternative mean of calculating this quantity is provided.

$$THD = \sqrt{\left(\frac{V_{n,rms}}{V_{1,rms}}\right)^2 - 1} \qquad (1.9)$$

This definition of THD is eligible only if the desired output voltage is the fundamental otherwise the definition of THD has to be modified accordingly. If this equation is applied to a full bridge inverter Figure 1.1 it can be assumed that by proper control, the positive and negative portions of the output wave are symmetrical meaning no DC or even harmonics, the voltage THD factor reduces to

$$THD = \sqrt{\sum_{n=3,5,7,\ldots}^{\infty}\left(\frac{V_n}{V_1}\right)^2} \qquad (1.10)$$

Or

$$THD = \sqrt{\sum_{n=3,5,7,\ldots}^{\infty}\left(\frac{V_{n,rms}}{V_{rms}}\right)^2} \qquad (1.11)$$

where, V_{rms} denotes the RMS value of the overall waveform. This expression is used mainly in Europe and has the advantage of always being between zero and one [1].

1.2.3. Fundamental Concepts of PWM Methods

One of the most widely utilized strategies for controlling the AC output of power electronic converters is the technique known as pulse width modulation (PWM) which varies the duty cycle of the converter switches at a high switching frequency to achieve a target average low frequency output voltage or current [4]. For over three decades, modulation theory has occupied a great part of the research being carrying out in the area of power electronics and still continues to attract substantial attention and interest [1]. This is justifiable, since power electronics penetration in many aspects of everyday life has been increased more and more. Power converters have been present to nearly all appliances and industrial devices and particularly modulation is at the heart of almost every modern power electronic converter. On the other hand, the significant increasingly amount of papers published about this topic, makes it hard for the user to identify the basic modulation principles of the methods or which is the most suitable for implementing in particular applications. One can easily notice that many published researches has been presented as “new”, “novel” or “improved” PWM techniques which are often only a variation of previous approaches. This sometimes can be difficult to detect and understand how they are actually related. However, a number of clear trends in the research and development of PWM strategies has been carrying out since the 70’s [5], [6] clearly addressing the main objectives of reducing harmonics or increasing the magnitude of the output for a given switching frequency along with the development of suitable converter topologies for different applications.

At their origin all modulation schemes aim to create switched pulse trains which have the same fundamental volt/second average, (the integral of the voltage waveform over time), as a target reference waveform at any moment. The drawback of these modulation strategies is that these trains of switched pulses contain unwanted harmonic content which shouldn't be present and must be minimized. Thus, for all PWMs after satisfying the primary objective, which is to calculate and determine the desirable switching scheme to create the wanted target output voltage or current, the second objective is to determine the most effective way of arranging the switching process to minimize unwanted harmonic distortion, switching losses, or meet any other specified performance criterion.

Performance characteristics of power converters largely depend on the choice of PWM strategy implemented. In present-day available PWM techniques can be broadly classified as carrier-modulated sine PWM and pre-calculated programmed PWM schemes [7]. The actual process of carrier based PWM schemes is usually a simple comparison between a reference waveform and a sawtooth or a triangular carrier waveform. If the switching losses in a power converter are not a concern, meaning that switching ranges of few kHz, then carrier PWM methods are acceptable and very effective for controlling. Since the generated harmonics are beyond the bandwidth of the system being implemented, therefore these harmonics do not dissipate power [8]. On the other hand, for systems where high efficiency is very important and switching must be kept at low frequencies the approach of programmed PWM strategies is needed [9]. Programmed PWM techniques such as Optimized Space Vector modulation, Harmonic elimination PWM, Optimum PWM and Minimum-Loss PWM [1] are able to optimize a particular objective function such as to obtain minimum switching losses, reduce torque pulsations (i.e. motor drive), selective harmonic elimination and therefore are more suitable to obtain high-performance results [7]. The difficult task of computing specific PWM switching times to optimize a particular objective has the result of much considerable

computational effort and that becomes one of the main drawbacks of programmed schemes.

Regarding the approaches of the renewable sources, the power converters are designed in medium-high power rating. In these applications, the implementation of high frequency PWM for two-level inverters is limited due to voltage levels, current ratings of switching devices, switching losses, and electromagnetic interferences caused by high dv/dt.[10] Thus, to overcome these limitations, multilevel inverters have been proposed as a promising solution. In the next steps, different circuit topologies, control algorithms, and the applications for multilevel inverters are described.

1.2.4. Multilevel Inverters

While conventional PWM inverters have been used in industrial applications widely, they have many drawbacks:

- The carrier frequency must be very high. At Mohan's book [8] a m_f>21 is proposed which means an average switching frequency f_s>1 kHz if the output waveform frequency is at 50Hz. This leads to an f_s at 2-20 kHz in order to keep the THD small [8].
- The pulse height is significantly high. The output voltage of a PWM inverter has a large jumping span. For example, if the DC linkage voltage is at 400V all the pulses have to reach the peak value of 400V causing large dv/dt and significant EMI.
- In case of a desirable low voltage output the pulse width would be much narrowed. For example if the voltage output is a10 V and the DC linkage voltage is at 400V the pulse width must be at 2.5% of the pulse period at 50Hz.
- The last two terms cause two more problems. Plenty of harmonics are produced resulting in poor THD along with the very rigorous switching conditions that are needed causing the switching devices to experience large power losses.

- Finally the inverter control unit has to be very complex and devices become costly.

Furthermore, it is hard to connect a single power semiconductor switch to the medium-voltage grids where voltages are from 2.3, 3.3, 4.16 or even 6.9 kV.

For the above reasons, as a solution for working with higher voltage levels, the new family of multilevel inverters has emerged [11, 13]. Multilevel inverters have been recently applied in high-power medium-voltage applications. Firstly, the idea was published by Nabae A. in 1980 in an IEEE international conference, IEEE APEC'80 [14], where a different approach for inverters was introduced with multilevel inverters technology. Instead of chopping vertically a reference waveform to achieve the similar sinus output waveform, the multilevel technique horizontally accumulates levels to achieve the output waveform.

This technique overcomes the above drawbacks of the conventional PWM inverters in a manner which:

- The switching frequency of the switching devices is very low. Close to the output signal frequency (only a small multiple).
- The pulse heights are quite small depending on the levels (layers) chosen. This normally causes low dv/dt and low EMI.
- The pulse widths of the all layer pulses are comparable to the output signal.
- Now the last two terms cannot cause plenty of harmonics and the THD is much lower. They offer also low switching power losses.
- Finally the inverter control unit is relatively simple and the inverter devices become economical.

Two are the major drawbacks of multilevel inverters. First is that they contain a serious amount of power switches, capacitors and diodes. The second is that they require isolated voltage sources or a bank of series capacitors for voltage balancing. Multilevel inverters include an array of power semiconductor and

capacitors voltage sources. Their voltage output generates the stepped waveform for the inverter. The commutation of the switches is taking place in such a manner that the capacitor voltages are being added reaching high voltages at the output, while the semiconductors withstand only lower voltages.

In Figure 1.1 a schematic diagram of one phase leg of inverters with different numbers of levels is shown. The action of the power switches is represented by an ideal switch with several positions. A two level inverter Figure 1.1a generates an output voltage of two levels with respect to the negative terminal of the capacitor. In Figure 1.1b a three-level inverter is shown and in Figure1.1c an m-level is shown generating an m-level voltage output.

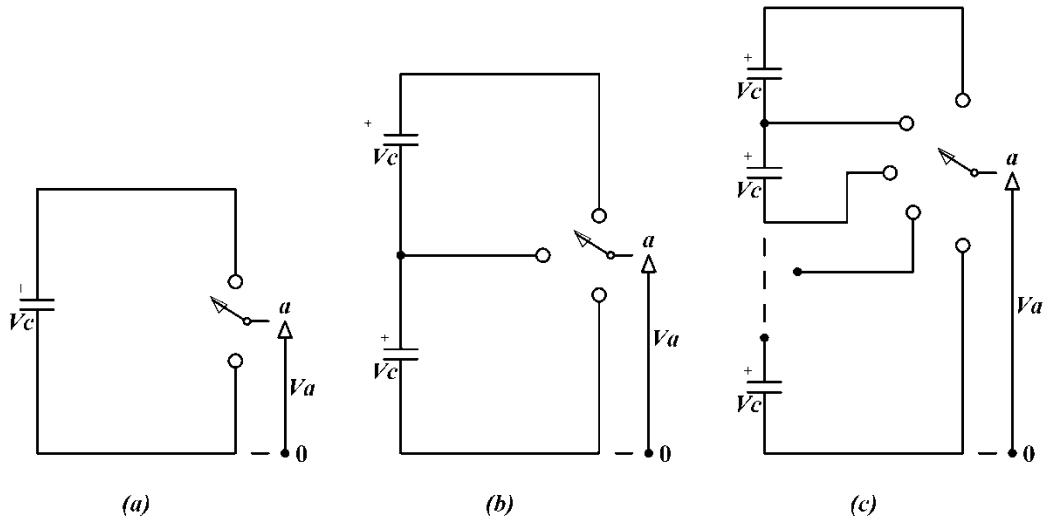

Figure 1.1 One phase leg of an inverter: (a) two levels, (b) three-levels, (c) m-levels.

Hence the output of multilevel inverters has multiple voltage levels reaching high voltage output levels, while the semiconductors withstand only lower voltages.

Various kinds of multilevel inverter topologies have been proposed, tested and installed [3] such as:

- Diode clamped
- Capacitor clamped

- Cascade multilevel inverters with separate DC sources
- H-bridge multilevel inverters
- Generalized multilevel inverters
- Mixed-level inverters
- Multilevel inverters by the connection of three-phase two-level inverters
- Soft-switched multilevel inverters
- Laddered inverters

As the number of levels (DC sources) that synthesize the output voltage increases, the quality of the voltage is improved and the effort of output filters can be decreased. The transformers can be eliminated due to the reduced voltage. Life of the switches is increased, since they operate in much lower frequency. Furthermore, since multilevel inverters are cost effective solutions, their usage is extended to medium and low power applications such as photovoltaic systems, vehicle propulsion systems, active power filters, voltage sag compensators, uninterrupted power systems (UPS) and distributed power systems.

The technology involved for the creation of different topologies is not new. Various topologies, over the past three decades have been investigated and developed. The diode clamped topology inverter (NPC) that was firstly presented in 1980 from Nabae can effectively double the voltage output of the device without requiring precise voltage matching. The capacitor clamped (also called flying capacitor) topology was introduced in the 90's. The cascade multilevel inverter topology, even if it was invented earlier it became widespread after the mid of 90's. In our times, cascade topology has drawn great interest due to the significant demand on medium-voltage high-power applications.

Multilevel inverters have been applied also to a wide variety of high-power applications such as, railway traction applications, motor drives, high voltage

DC transmissions (HVDC), unified power flow controllers (UPFC), static VAR compensators (SVCs), and static synchronous compensators (STATCOMs).

Multilevel inverters are able to offer an alternative approach of the compromises between switching frequency and optimization of the harmonic content of the output of a power converter.

Finally, a concentrated diagram of all multilevel inverter topologies is given in Figure 1.2. The family of multilevel inverter has brought a great solution to high-power medium-voltage energy control.

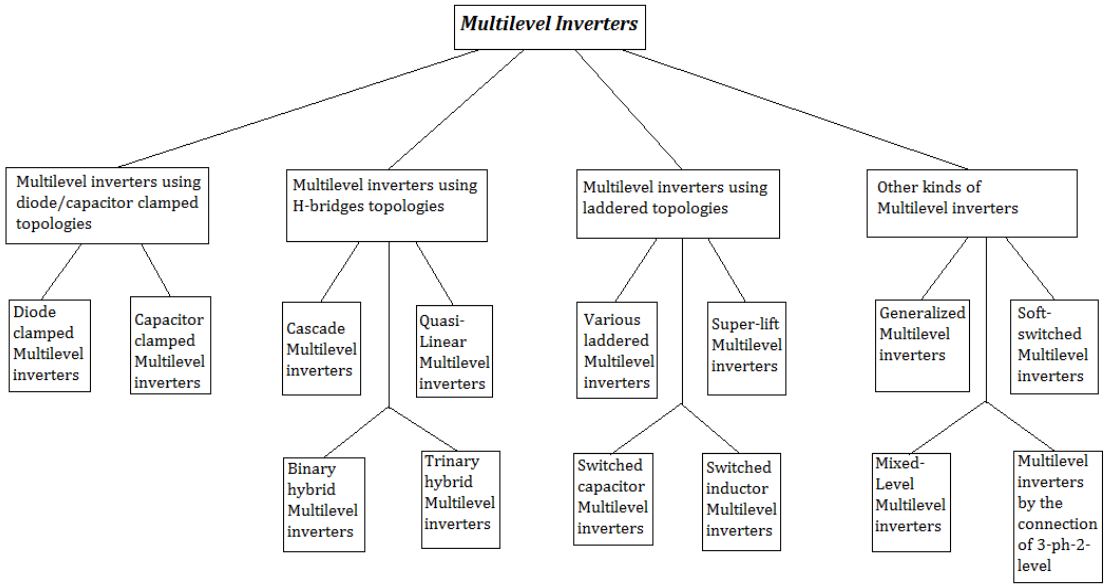

Figure 1.2 Multilevel inverter topologies family-tree.

The cascaded H-bridge multilevel inverter topology is used for the implementation of the proposed EAPWM and thus will be explained further in this thesis, since this modular topology is more widely used in numerous high-voltage medium power applications.

1.2.5 Multilevel inverters using H-Bridge Converters

Their basic structure is based on the connection of identical H-bridges (HBs). In Figure 1.3 the power circuit of one phase leg of a multilevel inverter with three HBs is shown. Each HB is powered by a separate DC source. The output voltage

is synthesized by the addition of the voltages that is being generated by the HBs. If the DC sources of each HB are equal then the inverter is called cascade multilevel inverter, if the DC sources are not equal then the inverter can be called hybrid multilevel inverter. In Figure 1.4 the waveforms of cascade multilevel inverters is shown. Since the DC link voltages of the identical HBs are equal

$$V_{dc1} = V_{dc2} = V_{dc3} = E$$

where, E is the source voltage. Each HB generates three voltages at the output: *+E, 0, -E*. The resulting AC output voltage ranges from -3E to 3E with seven levels as shown in Figure 1.4.

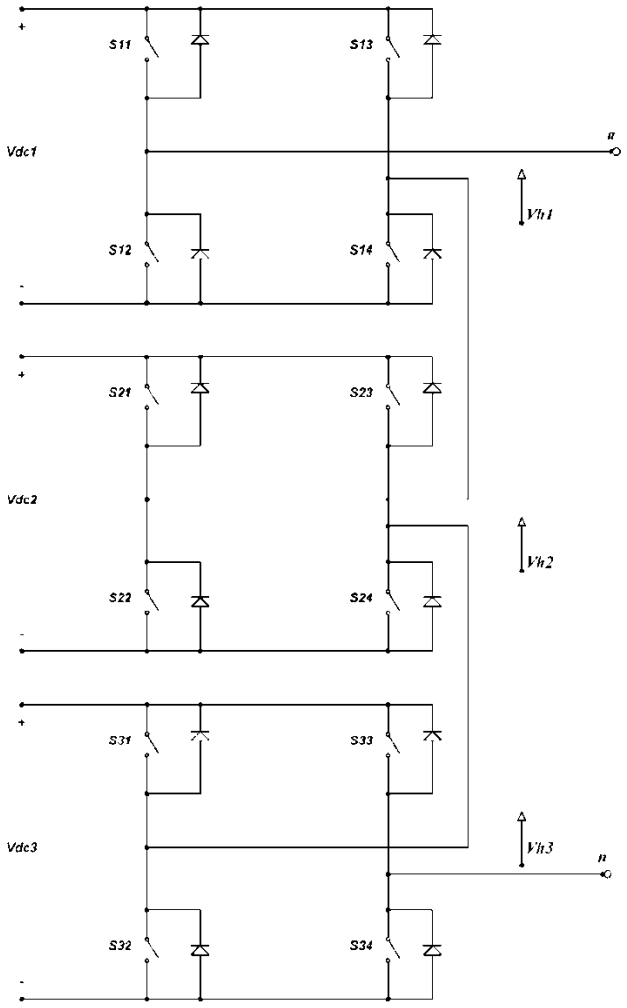

Figure 1.3 Power circuit of a cascade multilevel inverter with three HBs.

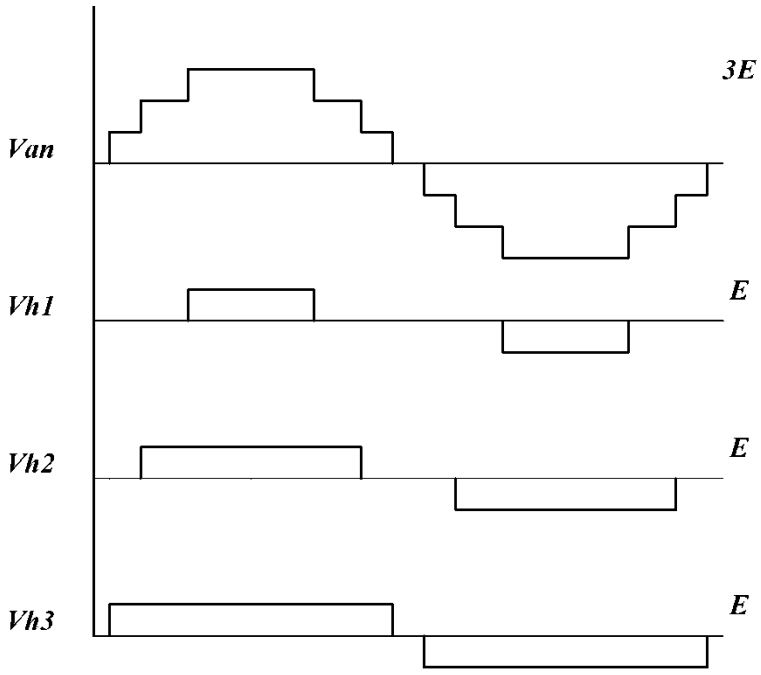

Figure 1.4 Waveforms of cascaded multilevel inverters with 7-levels.

Modulation in multilevel inverters is possible and has beneficial results. Significant reduce in THD values can be achieved with multilevel block modulation. That means that when the DC source voltage levels and switching instants are optimized the THD factor can be reduced even without necessarily resorting to pulse width modulation. This aspect of modulation can be enough when the output voltage target range is relatively small (i.e. in UPS). When the output voltage target is wide and the slew rate is relatively rapid (i.e. in AC motor drive) pulse width modulation of multilevel inverters becomes almost a necessity.

1.3 Aim and Objectives

The project aims to identify and investigate all up to date pulse width modulation (PWM) methods that are present for conventional and multilevel inverters. The primary objective of this project is to introduce a new approach in pulse width modulation and propose a microcontroller-based PWM method suitable for implementation in both conventional and multilevel inverters. The proposed algebraic method produced an algorithm to calculate the desired PWM pulse train. The results produced by the equal areas theory were then used for software simulation and evaluation of the experimental results. The software used for theoretical and simulation results were MATLAB 2012a and Proteus ISIS 7 Professional. A prototype full-bridge single-phase inverter was built to validate the theoretical results. A prototype inverter using the cascade topology was also built to produce the practical results and confirm the simulation outcome for the multilevel implementation of the proposed PWM.

The literature review carried out from this research also aims to identify and analyze the variable distinguishing factors existing for comparing the different PWM techniques. Since, the research regarding the topic of pulse width modulation has been contiguous over the last decades and gradually increasing over the last years with the introduction of multilevel inverters age, it is critical to identify in literature the basic concepts that are present behind any 'new' , 'novel' and 'unique' PWM methods. The latest fundamental PWM methods will be discussed regarding their advantages and drawbacks as well as limitations in implementation for particular applications.

The main contribution of this research is to develop an alternative PWM method to determine the switching angles in a direct way, using a consistent mathematical framework, requiring less computational effort for digital online implementation on a microprocessor-based system. In addition, investigation to the over-modulation region will be carried out in order to expand the linear operation of the power converter.

1.4 Project Plan

A flow chart is shown in Figure 1.5 illustrating the work carried out in this project. The flow chart shows also how the papers were produced over the carried out work.

The project took place in the lab of Power Electronics of the Electronics Engineering Department of the Technical Educational Institute of Athens (T.E.I of Athens), under the invaluable supervision of Dr. Drosos Nafpaktitis. Professor Dr. Mohamed Darwish of Brunel University had the overall supervision of the research. Based on the theoretical frame of the equal areas criteria for the conventional inverters, research and development formulated the proposed PWM method for multilevel inverters.

After defining the project aims and objectives, a literature review of the existing PWM methods was performed in order to achieve a critical understanding of the advantages and disadvantages of most commonly used methods. The up-to-date methods were also identified for conventional and multilevel inverters. A deep understanding of the variable PWM fundamental concepts and techniques was necessary to adequately distinguish, compare, and recognize their drawbacks regarding their applications, limitations and implementations.

Then the theoretical background of the proposed method was formulated in order to derive the basic algebraic equations. In parallel, the designing of the prototypes took place by choosing the suitable topologies. Designing procedures were quite fastidious in order to be able to extract the most reliable practical results from the implementation of the PWM method from the inverter prototypes. Driving the MOSFETS was quite a challenge using the driver IR2110 from International Rectifier.

Finally, after producing the simulation and practical results, comparison with other methods was performed. During the literature review, evaluation schemes were developed enabling a better choice of performance indicators.

PhD Overview

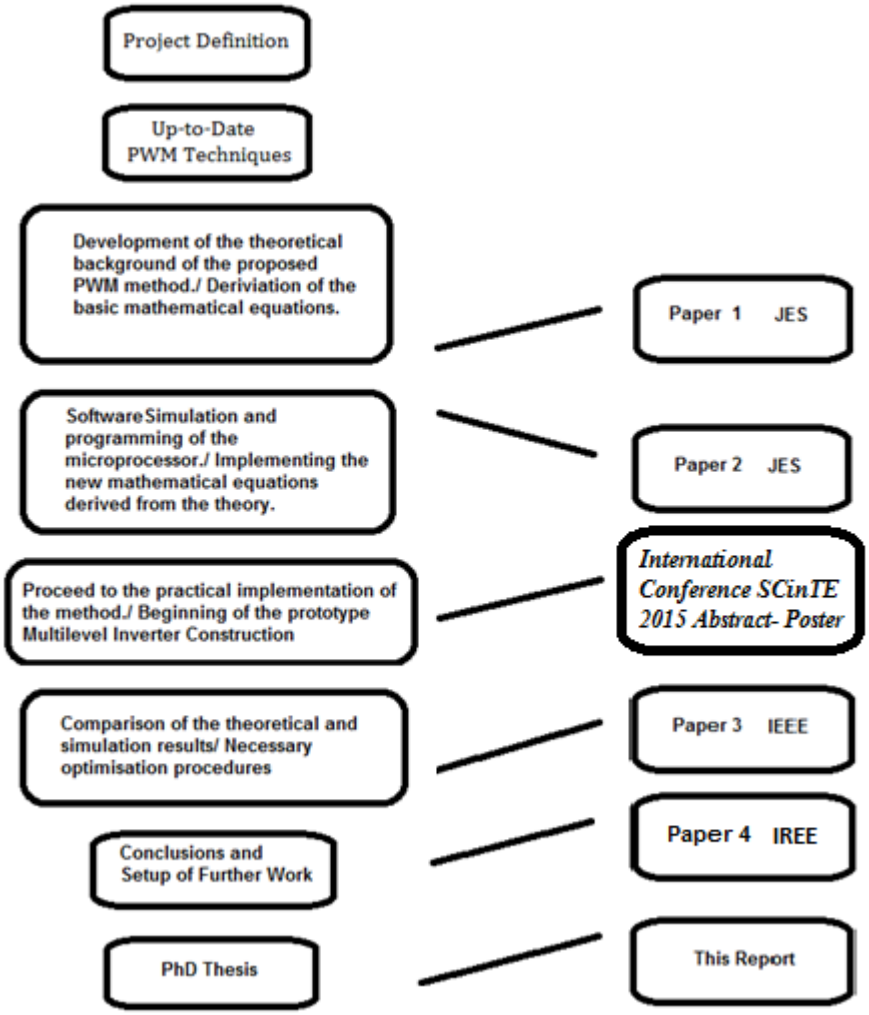

Figure 1.5 Flow Chart of PhD work plan

Paper 1. D. Nafpaktitis, G. Hloupis, I. Stavrakas, F. Paterakis, "An Alternative Approach for PWM Modelling in Power Electronics Systems," J. Electrical Systems 7-4 (2011): 438-447.

Paper 2. D. Nafpaktitis, F. Paterakis, M. Darwish, G. Hloupis, "The Equal Areas Pulse Width Modulation (EAPWM) Method: an alternative approach to programmed PWM schemes," J. Electrical Systems 12-1 (2016): 174-186.

Abstract-Poster, F. Paterakis, D. Nafpaktitis, G. Koulouras, M. Darwish, G. Hloupis, “Equal Areas Pulse Width Modulation for Voltage Source Inverters and Multilevel Inverters.” Poster in International Conference ‘Science InTechnology’ SCinTE 2015, 222-A02-141

Paper 3. F. Paterakis, D. Nafpaktitis, M. Darwish, G. Koulouras, ‘’A Modified Algorithm based on the Equal-Areas PWM for the Extend of Linear Operation of a Microprocessor-Controlled PWM Inverter’’ Institute of Electrical and Electronics Engineers (IEEE) under review.

Paper 4. Fotis Paterakis , Drosos Nafpaktitis, Mohamed Darwish, Grigorios Koulouras, Al Janbey, George Hloupis, ‘’ Implementation of Equal Areas-PWM in Multilevel Inverters’’, *International Review of Electrical Engineering (IREE)*, accepted paper ID number:9812, 2016

1.5 Thesis Structure and Content

The structure and content of this PhD thesis is illustrated in the flow chart presented in Figure 1.6.

The published papers include much of the work performed in this PhD thesis.

This thesis is therefore providing a coherent presentation of the overall work carried out on this project and its results. The thesis focuses mostly in the theoretical aspects of the project since experimental results are already included in the published papers. However, whenever it is needed, practical results are also mentioned in order to verify or illustrate the significance of the theory.

The structure of this thesis reflects the timetable of the work carried out following the projects plan organization i.e. background and motivation to define the objective/ Up-to-date (literature review)/ theory and derivation of

basic algebraic equations for the conventional inverter/ theory and derivation of basic algebraic equations for the multilevel inverter/ simulation and practical results/ conclusions. This thesis is organized to present the project results in a coherent and straightforward manner.

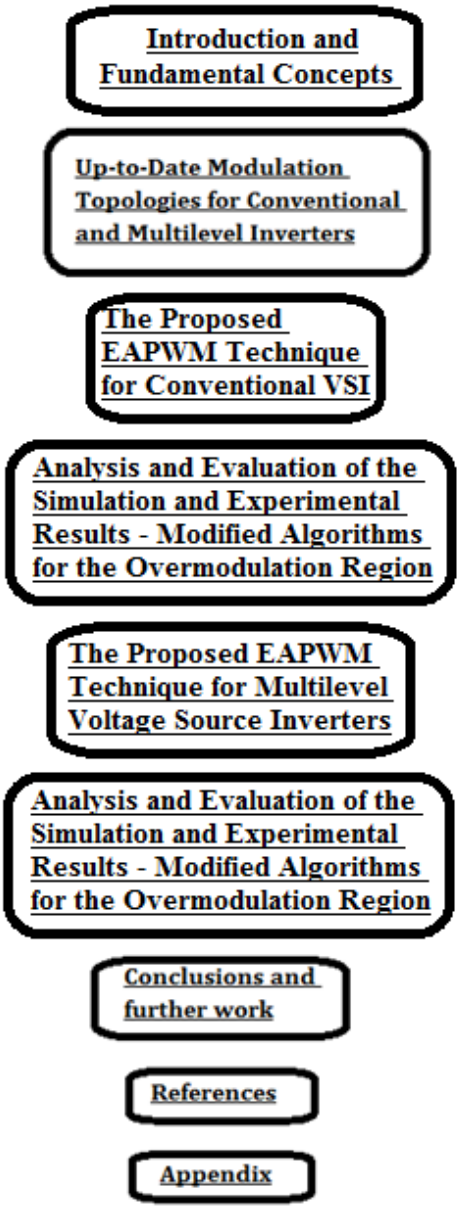

Figure 1.6 PhD Thesis structure.

CHAPTER 2

Up-to-Date Modulation Topologies for Conventional and Multilevel Inverters

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Introduction

In this chapter state of the art modulation topologies for conventional inverters and multilevel inverters will be discussed. The latest updates on pulse width modulation methods for conventional voltage source inverters (VSI) including carrier based and programmed based techniques will be briefly examined, focusing on single–phase VSI. Despite the fact that the topic of modulation in voltage source inverters has been carrying on for many decades, the researchers still are focusing on the optimization and development of the existing methods or even propose new and novel techniques so as to improve the voltage output of a voltage source inverter. At the same time, as multilevel inverters have been penetrated more and more in high-power medium-voltage energy systems, great interest has emerged on modulation to this converter technology as well. State of the art modulation regarding the optimization of the switching commutation and pulse width modulation will be being examined. In this thesis carrier based and programmed based techniques will be discussed and evaluated given the precedence to cascade multilevel inverters topology.

2.1 Modulation alternatives and performance criteria for Conventional VSIs

The main objective for all PWM methods is to calculate the inverter switching-on times in order to create a desired voltage output [1]. Despite the wealth of

papers that have been published over the years regarding PWM, there are only three major alternatives for determining the inverter switch on times for fixed-frequency modulation systems [2]. These alternatives are:

- Naturally sampled PWM - (Switching at the intersection of a target reference waveform (sinus) and a high-frequency carrier).
- Regular sampled PWM – (Switching at the intersection between a regularly sampled reference waveform and a high-frequency carrier)
- Direct PWM – (Switching so that the integrated area of the target reference waveform over the carrier interval is the same as the integrated area of the converter switched output).

Classical sine-modulation compares a sinusoidal reference modulation wave (naturally sampled) with a high frequency carrier to create gating pulses for the switches of the inverter. According to the carrier wave geometric form, there are two types of natural modulation methods: sawtooth (trailing edge) and triangle-carrier modulation (double-edge). For the saw-tooth carrier only the trailing edge of the pulse varies when the value of the modulation index changes, in opposition with the triangle carrier, when both sides of the switched output pulse from the phase leg are modulated, which considerably improves the harmonic performance of the PWM waveform (Figure 2.1).

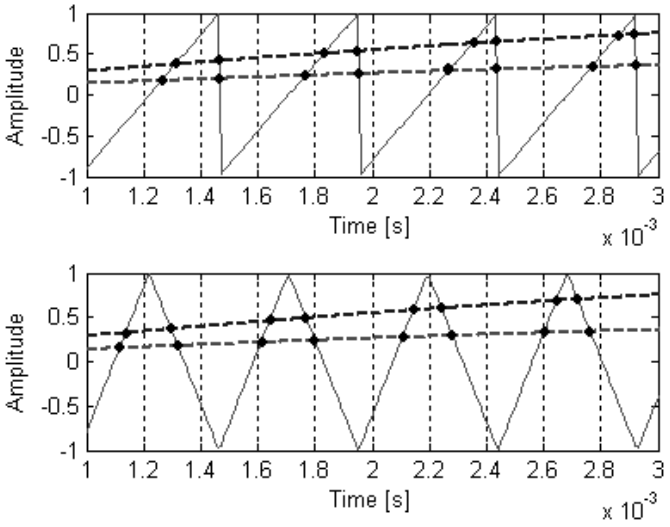


Figure 2.1 Naturally sampled modulation of sawtooth (trailing edge) and triangle-carrier modulation (double-edge), for different modulation ratios- dashed line.

One major disadvantage of naturally sampled PWM techniques is the fact that it is difficult to implement them in a digital modulation system, as the intersection between the reference and the carrier is defined by a transcendental equation and needs great computational effort to be calculated. The answer to that problem is the use of regular sampled PWM, where the reference waveform is sampled and then hold constant during each carrier interval. Then these stored values are compared against the carrier (saw or triangular) to produce the gating pulses for the switches of the inverter. Depending on the carrier used for a sawtooth the sampling occurs at the falling end of the sawtooth ramping period. On the other hand, if the carrier is a triangle two alternatives can exist. Sampling can be symmetrical where the sampling reference starts at the positive or negative pick of the triangle waveform or asymmetrical where the sampling occurs every half carrier interval at both the positive and negative carrier peak. Regular sampling alternatives are illustrated in Figures 2.2-2.3-2.4, where the dash lines illustrate the changing in the modulation ratio. However, a drawback of these methods is that they generate an increased harmonic spectrum due to the regular sampling process, which can be attenuated by using a higher ratio between the carrier-wave frequency and reference modulation wave frequency. The advantage of these regular sampling methods is that they are relatively easy to implement on digital structures and more important, when used for three-phase converters, some of the induced sideband harmonics (triple harmonics) are cancelled between phase legs.

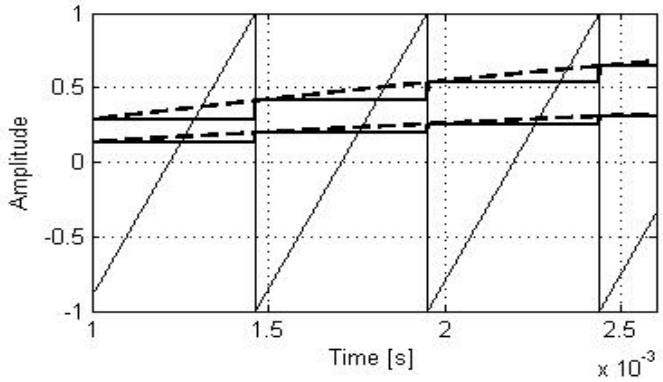


Figure 2.2 Regular sampling for sawtooth carrier.

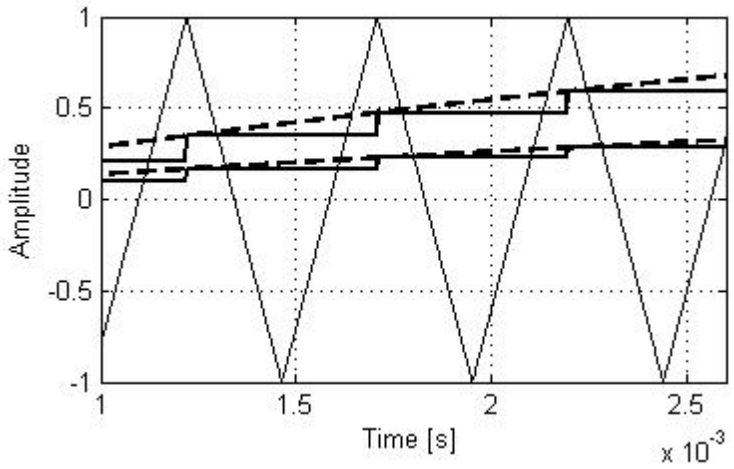


Figure 2.3 Regular sampling for triangle carrier (symmetrical).

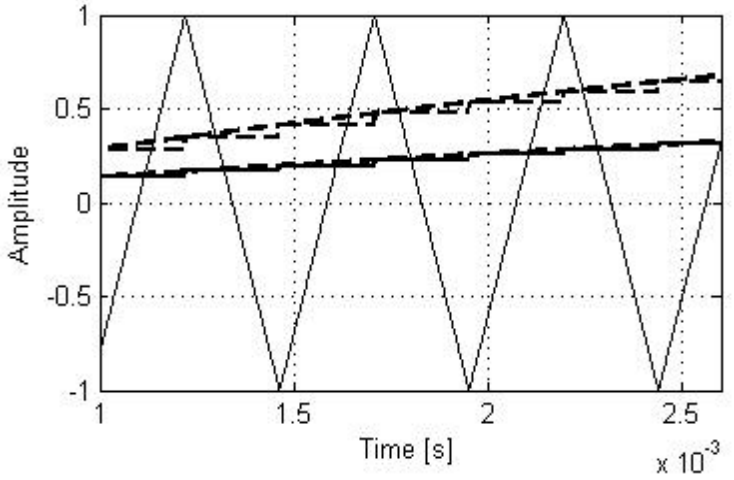


Figure 2.4 Regular sampling for triangle carrier (asymmetrical).

When examining the naturally and regular sampled PWM schemes it is useful to understand that these strategies require both phase-legs of the inverter to switch between the upper and lower DC voltage at the carrier frequency. That means that all devices switch continuously during the fundamental frequency and this approach is termed as continuous modulation. On the other hand, when only one phase-leg is modulated in the first half of the fundamental cycle, while the other is modulated in the second half (swapping as positive and negative polarity) of the fundamental cycle, this approach is termed

discontinuous modulation[3]. Figure 2.5 shows a single-phase leg and a full-bridge inverter.

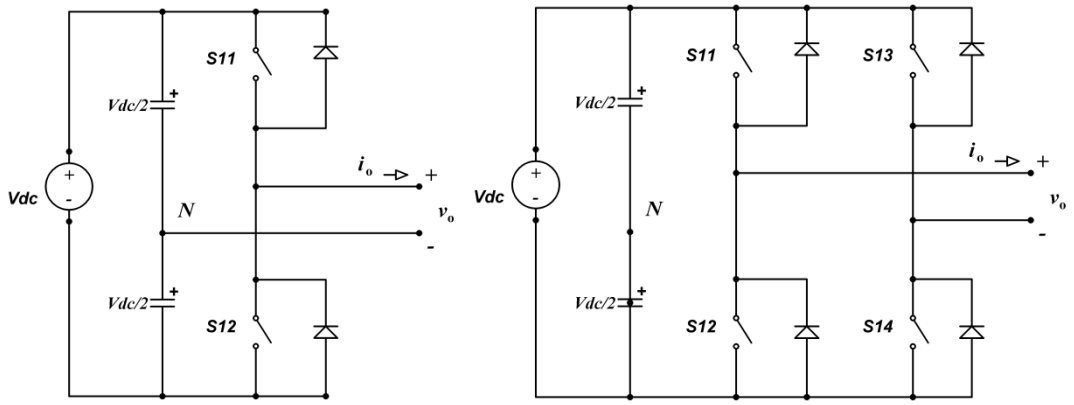


Figure 2.5 Single-phase leg half-bridge and a full-bridge VSI.

Variations of those alternatives have been published over the years in a great amount of researches, making sometimes difficult for someone to see their underlying commonality. Most of the PWM methods fall into these categories as for example the well-known space vector modulation strategy which is only a variation of regular sampled PWM which specifies the same switched pulse widths but places them a bit differently in each carrier interval [2]. Hence, it is useful to explain the fixed frequency open-loop PWM strategies in terms of:

- The determination of the switched pulse width.
- The position of the switched pulse within a carrier interval.
- The sequence of the switched pulse within and across carrier intervals.

Then, the harmonic performance of a particular PWM inverter can be explained as the effect of these three factors on the harmonic spectrum of the inverter output. Speaking on performance, over the years the subject of a common basis for evaluating the performance of various PWM strategies has gathered a considerable research work. There is an arguing between researchers on the basis of how beneficial really are, for comparison of PWM schemes over the other, the diminished harmonics [4]. Other researchers proposed other performance factors such as first or second-order filtered distortion

performance factors [5]. Others evaluate the RMS harmonic ripple current in a typical load such as the induction motor [6]. All of these perspectives that have been published are accompanied with particular arguments as to why the performance index proposed in preferable. In order to avoid the confusion that unfortunately is procured from this large amount of work Grahame Holmes and Tomas Lipo [1] propound an approach for comparing all PWM variations on exactly the same basis. The approach used is threefold:

- The existence and availability of analytic solutions for determining the magnitude of the various harmonic components.
- PWM to be examined at the same phase leg switching frequencies.
- The first-order weighted THD factor for a more rapid comparison of PWM alternatives.

The alternatives discussed so far can be called classical techniques and generally not optimized [7]. They involve the exact positioning of the pulses within a clock cycle obtained from the carrier frequency, so as to achieve a minimal distortion waveform. However, there are also modulation alternatives which can remove this constrain. These are the programmed modulation strategies.

2.2 Programmed modulation Strategies

All previous modulation methods can be considered as clocked modulations. Since the frequency of the basic modulation carrier (sawtooth-triangle) has been held fixed the modulation was clocked to this mark-space interval. This constrain can be removed so as the individual pulses can vary in width and position over a much wider interval. The removal of this particular constrain enables a new approach of determining the switching times. The switching times can now be calculated based on the minimization of a suitable objective function which in most cases represents the system losses in general. These modulation methods are called programmed modulation schemes as the

switching operation is programmed in order to optimize the overall performance of the power converter. The best optimization results are achieved with switching sequences having odd pulse numbers and quarter-wave symmetry [1].

The optimization procedure is done off-line on a personal or master computer. The results of the computational process which consist a set of switching angles (which are functions of modulation index M) are stored in the memory of a microcontroller or an EPROM in order to be accessed in real time. The harmonic spectrum of the PWM signal is free from sub-harmonic components since this set of angles has been produced in synchronization of the fundamental component. The computational effort needed for these calculations increases significantly as the number of the switching angles increases. The benefits of these methods are undeniable, but the excess in time, computational effort and resources can prevent their use in lower-cost applications. However, these optimized methods can be combined with classical techniques discussed earlier, to produce a more cost effective solution to a wider field of applications [8].

In literature, the classification of programmed off-line schemes can also be done either with respect of the optimization object and the PWM technique that the optimization is implemented or a general classification with two basic alternatives:

- Line-to-line (*l-l*) PWM waveforms consisting of three-level switching (between positive-zero-negative states)
- Line-to-neutral (*l-n*) PWM waveforms consisting of two-level switching (between positive and negative states)

These two basic categories stem into several other possible schemes based on single or three-phase inverter configurations [9].

In this report, a brief reference of the most dominant programmed PWM schemes for conventional inverters (single or three-phase) along with their up to date modifications will be addressed.

2.2.1 Space Vector PWM and Optimized Space Vector PWM

In this thesis only the fundamentals of Space Vector Modulation (SVM) and Optimum Space Vector modulation are presented. Since this project concerns are more weighted to single phase voltage source inverters this thesis will not expand to three phase voltage source and current source techniques.

Space vector modulation emerged in the mid-1980s proposing an alternative method of determining the switching pulse widths. It was claimed to offer significant advantages over natural and regular sampled PWM in terms of ease of implementation and performance [10, 11, 12]. The main alteration and eventually the major benefit of SVM is the explicit identification of pulse placement as an additional degree of freedom that can be used to achieve harmonic performance gains. The only difference of SVM with regular sampled PWM is the position of the zero (inactive) space vectors within each half carrier period. In regular sampled PWM these zero vectors have no opportunity for variation since they are prescribed by the algorithm definition that is given. In SVM these space vectors are left undefined giving the opportunity to manipulate them in benefit of the harmonics. The conventional SVM centers the active space vectors and splits the remaining zero (inactive) space vectors equally. Optimized Space Vector Modulation reallocate the position of inactive space vectors in a specific time interval optimizing the switching periods.

In literature generic algorithms have been used to optimize the harmonic content for power inverters under the SVM. The relationship between three-phase carrier based PWM and SVM has been analyzed by Keliang Zhou and Danwei Wang in [13]. All the relationships between the methods showed that a

universal platform can be provided not only to implement transformation between carrier-based PWM and space-vector modulation, but also to develop different performance PWM modulators. Jian Sun and Horst Grotstollen in [14] studied the relationship between Optimized SVM and regular sampled techniques showing that the apportioning of null-vector time between two null vectors (for SVM) and the zero-sequence components added to the modulation waves (in regular-sampled PWM) represent a significant degree of freedom that can be properly utilized to optimize the performance of each modulation method in terms of harmonic current distortion and/or switching losses. An analysis of naturally sampled SVM PWM in overmodulation region has been carried out in [15] proving that naturally sampled SVM PWM could be used not only in undermodulation but also in overmodulation region. In [16] researchers used generic algorithms for optimization of SVM aiming to minimize the filtering requirement by lowering most significant harmonics while conforming to the available standards for voltage waveform quality. The SVM in three-leg inverters topology cannot handle the neutral current, so a four-leg topology was proposed in 1993 [17] to solve this problem by adding a neutral leg. The 3-D SVPWM used in three-phase four-leg topology was proposed for the first time in 1997 [18].

2.2.2 Harmonic Elimination Techniques

One of the earliest schemes of PWM technique [19] which introduced programmed forms and algorithms to progressively eliminate the low order harmonics is the so called harmonic elimination PWM [20, 21]. Generally, each phase-leg of an inverter has a two-level output. The main objective is to obtain a sinusoidal AC output voltage waveform where the fundamental component can vary by adjusting arbitrarily (within a range) the switches of the two level output of each phase-leg as seen in Figure 2.6 and also selectively eliminate the unwanted harmonics. This is achieved by mathematically generating the exact instant of the turn-on and turn-off of the power switches. The AC output voltage

features odd half- and quarter-wave symmetry. Therefore, even harmonics are not present. Moreover, the per-phase-leg voltage waveform (Figure 2.6), should be chopped N times per half-cycle in order to adjust the fundamental and eliminate N-1 harmonics in the AC output voltage waveform.

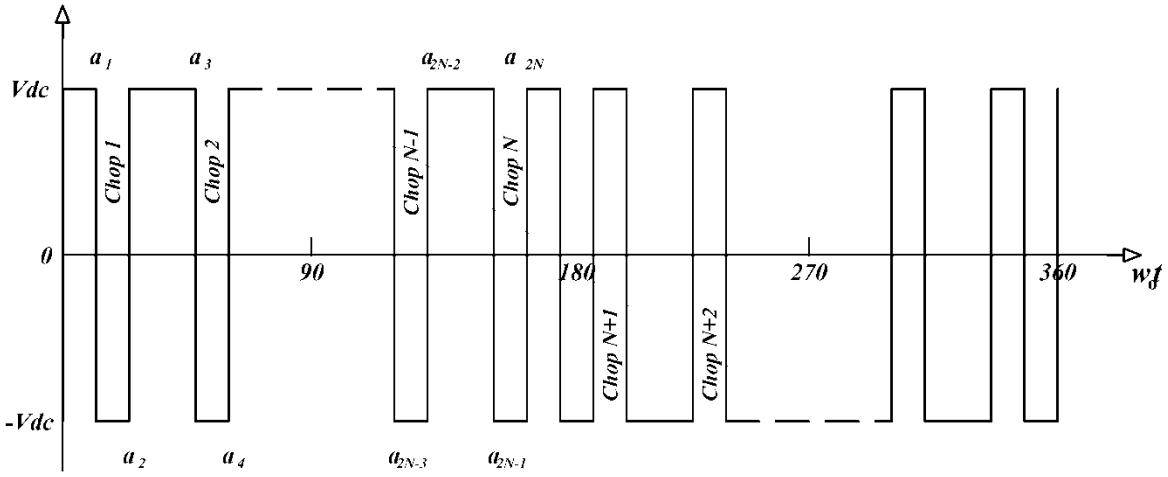


Figure 2.6 Generalized output waveform of half bridge inverter showing 2N notches per cycle.

For example, for N=6, in the squared waveform in Figure2.7, 6 chops are introduced to control the voltage magnitude of the fundamental component and the elimination of the fifth, and seventh harmonic. It is shown in Figure 2.7 that the output waveform has half-wave odd symmetry. Hence, only odd harmonics are present at the output. In a three phase inverter which consists of three identical phase-legs the triplen harmonics of the switched output are being eliminated to minimize the THD and thus there is no need to eliminate them.

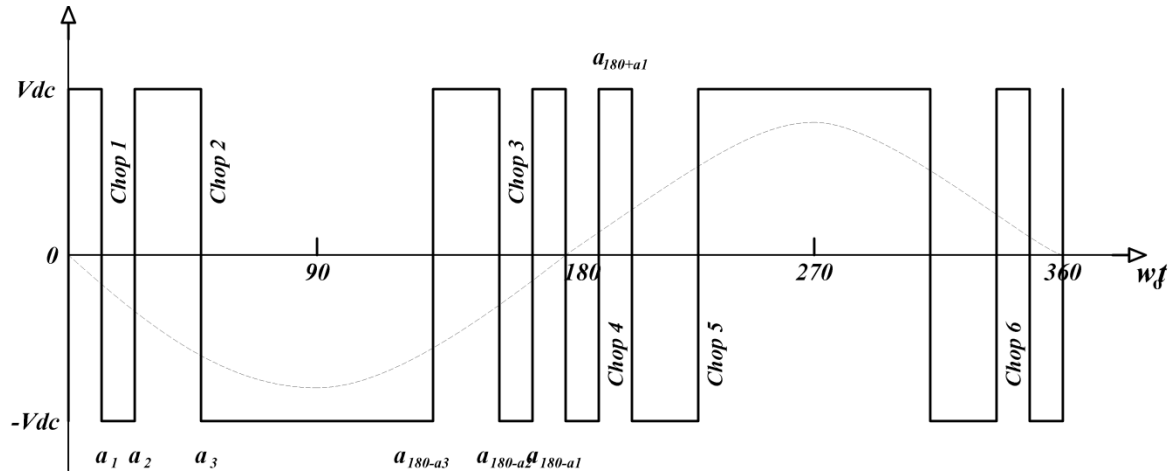


Figure 2.7 Programmed elimination of fifth and seventh harmonic component.

To define the angular positions of α_1, α_2,… α_{2N} the use of Fourier series considering also the odd quarter-wave symmetry concluded to the expression

$$a_n = \frac{4}{n\pi}\left[1+2\sum_{k=1}^{N}(-1)^k \cos n a_k\right] \qquad (2.1)$$

which showed that for a two-state waveform of the type shown in Figure 2.6, any N harmonics can be eliminated by solving the N equations obtained from setting equation (2.1) equal to zero. The waveform is chopped N times per half-cycle and is constrained to possess odd quarter-wave symmetry. This theory applied to full bridge inverters where it is shown that it is possible to eliminate as many harmonics as the number of pulses per half-cycle of the waveform by constraining the size and position of the pulses. One advantage of generating the waveform for full-bridge over that of single phase-leg inverter is the reduction in the number of commutations per cycle required to eliminate the same number of harmonics.

In literature, a significant amount of research work has been focused on finding the switching angles that produce the fundamental while not generating specifically chosen harmonics. In [22] S.R. Bowes introduces a new harmonic elimination strategy using regular sampling techniques enabling to calculate

the switching angles in real-time. The calculated times are very closely approximations of the exact switching angles produced off-line for the harmonic elimination PWM strategy. J.Chiasson and L.M Tolbert in [23] using the resultant theory were able to find all solutions, even solutions that were never found before in literature for both unipolar and bipolar switching patterns of harmonic elimination problem. Instead of using Newton Raphson iterative method they converted the transcendental equations that form the harmonic elimination problem into an equivalent set of polynomial equations enabling them to use the mathematical theory of resultants. Resultants are used to solve systems of polynomial equations to determine whether or not solutions exist or to reduce a given system to one with fewer variables and/or fewer equations. Genetic algorithms have also been used to solve the problem without the need of initial values which can be arbitrarily selected enabling to put forward these methods to be used in cases where the load can change [24]. Yuan Zhi-bao and Yang Ke-hu in [25] used Groebner bases theory to solve the selective harmonic elimination problem. Similarly, the equations have been transformed to polynomial equations but now using the multiple-angle formulas and variables substitution, the polynomial equations are converted to an equivalent triangular form by computing the reduced Groebner bases under the pure lexicographic monomial order. Finally, the triangular equations can be solved by a successive back-substitution manner just like the Gaussian elimination, which is used to solve the linear equations. This method gathered three advantages: no need to set initial values, all solution can be found and choose the optimal and it enables you to see whether the SHEPWM equations have a solution or not. Latest researches have been focusing on grid harmonics problem as the distributed networks technology expands. The extensive use of non-linear devices as well as power electronic devices causes grid harmonic problems. In [26] researchers investigate the effects of harmonic elimination and discuss the possible effective filtering in micro-grids as they expand.

2.2.3 Optimum PWM-Minimum Loss PWM

Forced commutated inverters are mostly used to supply variable speed AC drives. In these cases pulse width modulation is preferable in order to achieve the ultimate purpose of modulation: to create, to as high in accuracy as possible, a sinusoidal current flowing in the motor stator winding. To attain this outcome the various PWM techniques attempt to create a sinusoidal voltage while progressively eliminating harmonics. This is an indirect way of dealing with the problem. Another approach is to simply use the distortion in the current as a figure of merit and attempt to minimize this function [27, 28]. Of course, minimizing this factor demands much more difficult procedures since, the current waveform is not known *a priori* without current sensors or without the knowledge of the load. Nevertheless, considerable outcome can be obtained by adopting a few simple assumptions i.e. assuming constant motor parameters which in actuality vary with frequency. In addition, powerful micro-processors in embedded systems give the possibility in the near future for on-line optimization.

Now assuming the load under consideration to be an AC motor two critical assumptions can be made: the leakage inductance of the motor is not frequency dependent and the voltages applied to the motor are symmetric three-phase set with no DC component. As a result, the RMS current in one of the motor phases can be expressed as

$$I_{rms} = \sqrt{\frac{1}{2}\sum_{n=2}^{\infty}\left(\frac{V_n}{n\omega_o L_\sigma}\right)^2} \qquad (2.2)$$

where

I_{rms}=RMS value of the sum of the harmonic currents

V_n=peak value of the n harmonic of the output voltage

ω_o=fundamental angular voltage

L_σ= nominal sum of the motor stator and rotor, leakage inductance

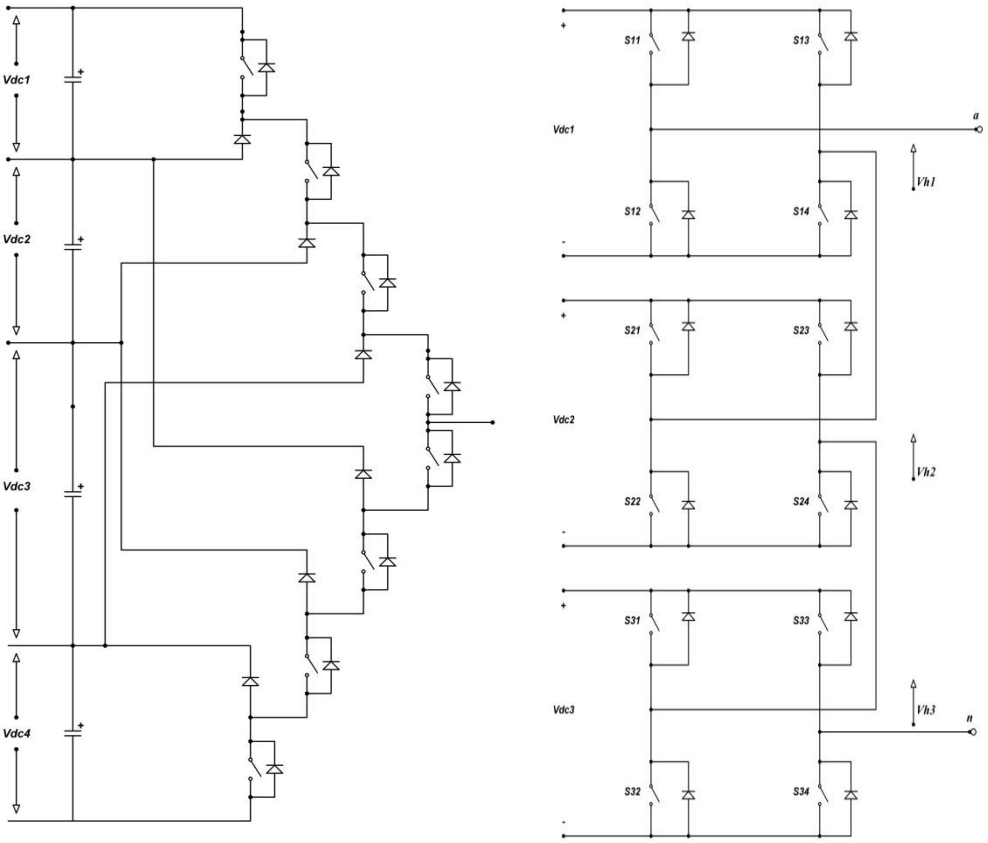
The last equation (2.2) can be used as the performance index against which various optimizing PWM methods can be compared [2].

While the concept of minimizing this performance index can be considered straightforward, the actual process is very difficult since the expression is in fact again a function of the switching angles. As the number of switching angles increases, the possible number of solution increases rapidly and the number of solutions becomes more difficult to predict than for harmonic elimination. Another approach, uses equation (2.2) to derive specific loss factors of loss components like copper losses or iron core losses in an inductive load or induction motor [29, 30]. Summarizing, the true optimum remains a difficult to find target, and will certainly be the interest of research for the next years.

2.3 Determining the Switching Angles for Multilevel Inverters

Multilevel inverters nowadays are offering an attractive alternative for mid and higher power applications. The problem that occurred with the semiconductor switch ratings that were limiting the application of power converters in the tens to hundreds of megawatts can now be overcome by the use of Multi Level Inverters (MLIs). Inverters operating at mid-range voltage (2 kV to 13.8 kV) are frequently making use of GTO thyristors that are able to handle these large power levels. The drawback of GTO thyristors is that their switching capability is limited to a carrier frequency of a few hundred hertz. On the other hand, IGBT switches are able to achieve higher switching speeds, but can withstand less voltage stress. To overcome these problems in that kind of power converters, IGBT switches were used in series to share the impressed DC link voltage, and to obtain higher switching speeds. However, the operation of the power converters became a concern since the series switches had to be carefully matched to turn on and off in concert with other series to prevent transient overvoltages, resulting in the implementation of sophisticated adaptive gate control algorithms. MLIs also use higher speed switching semiconductors but

can avoid the problems of using them in series by connecting single devices between multiple DC voltage levels. It has to be mentioned, that MLIs can be more complex to control and modulate because of the number of switches involved, but they provide the significant benefit of reduced harmonic content and THD in the switched output voltage. Two of the most common topologies of MLI are the diode-clamped inverter [31] and the cascade inverter [32]. The diode clamped topology uses one DC bus subdivided in to a number of voltage levels by a series of capacitors. The voltages across each of the switches are clamped by a diode at the voltage level of only one of the series capacitor. On the other hand, cascade topology is constructed by a series of single-phase-full-bridge inverters, each one fed by their own isolated DC bus. In Figure 2.8 the most common types of the two topologies are shown.



(a) (b)

Figure 2.8 (a) One pole of a five-level diode-clamped MLI, (b) a seven-level cascade MLI (three single-phase-full-bridge inverters in series)

In order to simply synthesize the output, the semiconductors of a MLI can be switched with fundamental switching frequency. By choosing appropriate-optimized switching angles, a significant small THD can be obtained for the synthesized voltage output. A switching diagram is shown in Figure 2.9. Furthermore, the DC levels that compose the voltage output of a MLI are not limited to be equal. There is no need for the DC levels to be identical, but can vary to each other and furthermore can be adjusted as desired in the particular application. That means that there are two possibilities for synthesizing the output of a MLI. One, where the DC voltages remain equal and only the switching angles have to be adjusted so as to adjust the fundamental component and minimize the THD [33], and the second, where both the DC voltages and the angles are adjusted to achieve the desired fundamental component and the minimum THD [34, 35]. In this thesis, programmed methods to determine the main switching angles are going to be investigated. Methods and optimization techniques discussed previously for conventional inverters can be also implemented to obtain the main switching angles for the MLIs.

Harmonic elimination or optimum PWM methods that have been mentioned before in this chapter can be pursued to optimize the switching angles. If harmonic elimination technique is used for a seven-level inverter, then either a maximum number of three harmonics can be eliminated determining also the value of M (modulation index) or if M is specified then one less harmonic can be eliminated.

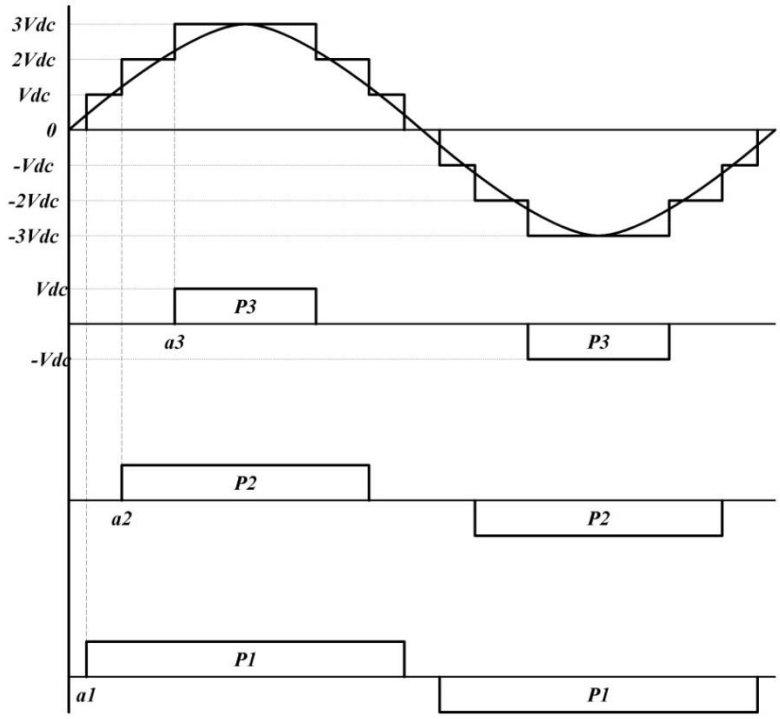


Figure 2.9 Switching diagram for a seven-level cascade inverter with equal DC sources.

From Figure 2.9 one can observe that the block modulation induces unequal losses in the semiconductors switches. For example, area P3 corresponds to an individual full-bridge cell that delivers only the P3 voltage for both positive and negative cycle over one period. Since P3 is less than P1 then the switches of full-bridge P3 will be stressed less than the switches of full-bridge that delivers P1. This problem can be critical if the DC link for every full-bridge were instead a battery pack. Thus, each battery pack would not be discharged at the same rate. This problem can be solved by appropriate techniques for equalization of voltage and current stresses. One technique is to program the pulses as shown in Figure 2.10, where the voltage and current stresses can be equalled by sequentially swapping every half cycle of the voltage pulses P1, P2, P3 identified in Figure 2.9 [36].

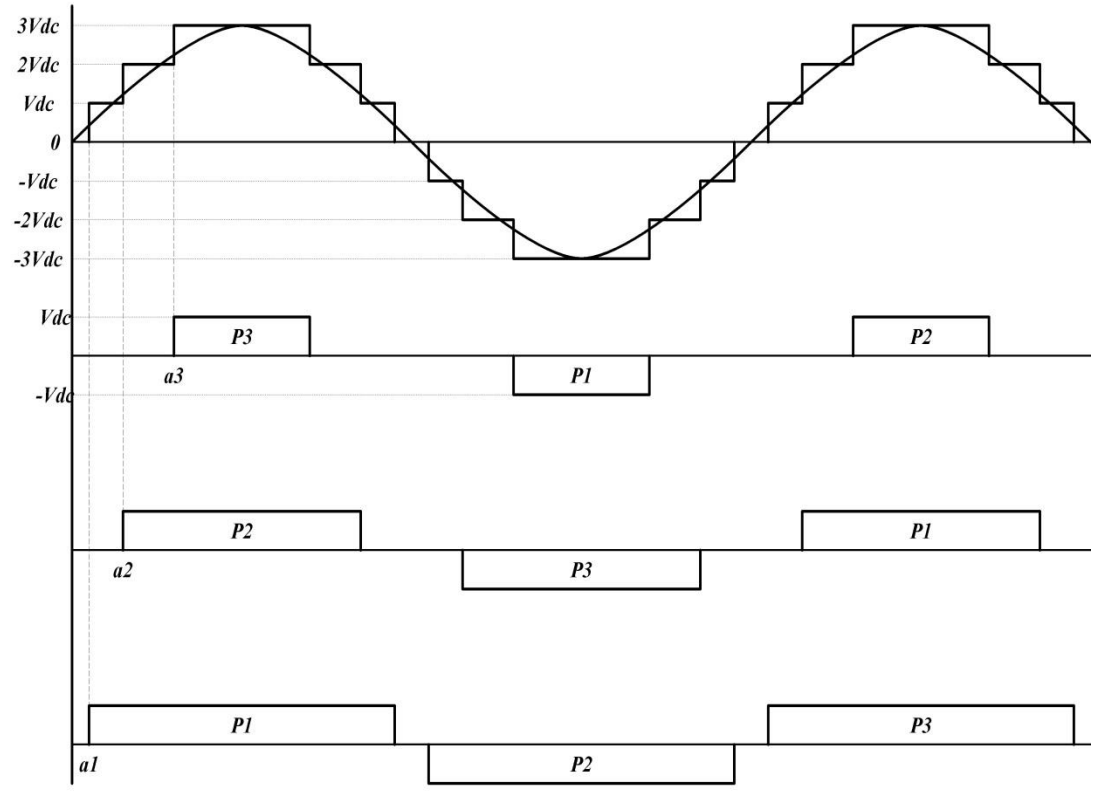


Figure 2.10 Balanced stresses among inverters by sequentially swapping of voltage pulses.

Another useful criterion to determine the switching angles of a MLI is the use of optimization algorithms to minimize the THD of the output, thus minimizing the losses in a motor load. In this case, if the DC voltage levels are assumed to be equal then the only variable will be the switching angles. Optimal solutions can be found also in cases where the DC voltage levels can be variables but in practice given a target fundamental voltage, the DC voltages must be held constant otherwise adjusting these voltage levels would imply costly adjustable DC supplies for each level.

In the cascade topology, each H-bridge inverter unit has a conducting angle. Since the conducting angles are the factors determining the amplitude of the harmonic components they are calculated to minimize the harmonic components. The harmonic elimination technique [20, 21] can be regarded as

the conventional method which reduces the predominant low-order harmonics and maximizes the fundamental wave of the output phase voltage. The drawback of the conventional method is that in order to determine the switching instants, iterative methods need to be used such as Newton-Raphson. These methods can be time demanding, may include errors since they depend on iteration and finally large computational effort is needed and cannot be used on-line. Kang [37] proposed a simple method of determining the switching angles. This method does not require solving the set of nonlinear transcendental equations, but calculates several trigonometric functions derived by area equalities. This difference can be considered as a benefit since the method can obtain the switching angles through an on-line operation, given the modulation index. Fang Lin Luo and Hong Ye [38], presented four new methods to solve the problem of the accurate determination of the best switching angles to obtain lowest total harmonic distortion (THD) in advanced multilevel inverters. All methods described in [38] do not need to solve transcendental equations and are based on simple ideas using average distributions of switching angles over the range of 0-π and trigonometric functions as to obtain an output waveform as close to sine wave as possible.

In general, given that in most applications the output voltage amplitude and the frequency remain constant, PWM is not a necessity in low power applications (e.g., UPS, grid tie converters), but when the output voltage demand is wide and di/dt is relatively rapid (e.g. in a motor drive) pulse width modulation becomes again a necessity.

2.4 Carrier-Based PWM Methods for Multilevel Inverters

Modulation control of any type of multilevel converters can be quite challenging, and much of the recent research is based on heuristic methods and investigations. A common thread for researchers is the carrier-based PWM methods that are usually implemented only to individual inverter structures. A major contribution to the categorization of different modulation strategies for multilevel inverters was firstly introduced in 1992 by Carrara [39]. Carrara [40] set the stage for the detailed evaluation of the modulation alternatives existing until 1992. Ten years later McGrath and Holmes [41] provided analytical solutions for the most common forms of PWM for each multilevel inverter topology to identify modulation commonalities between the converter topologies. Through this research, which was McGrath's Ph.D. thesis, they were also able to develop the harmonically superior modulation strategy for each converter topology. Given that this research is considered as a milestone in carrier-based PWM for multilevel inverters, analysis and theoretical conclusions will be used from this research in order to clearly identify the fundamental principles of each carrier-based PWM technique.

2.4.1 PWM strategies for Cascaded Single-Phase H-Bridges

Carrier-based PWM of multilevel converters can be categorized by the topology that is implemented. PWM of cascaded single-phase H-bridges topology is using the modulation process denoted as *Phase-Shifted Cascaded* PWM or PSCPWM [42]. The essential principle of PSCPWM is to phase shift the carriers of each bridge to achieve additional harmonic sideband cancellation around the even carrier multiple groups, by retaining at the same time sinusoidal reference waveforms for the two phase legs of each H-bridge inverter that are phase shifted 180^{o} . The optimum harmonic cancellation occurs by phase shifting each carrier by $(k\text{-}1)\pi/E$, where k is the k^{th} converter and E is the number of series connected single-phase inverters per phase leg. For example, in case of a 5-level inverter then two $(E=2)$ single-phase H-bridge inverters are needed and two

carriers. Each carrier, for optimum cancellation has to be shifted using the previous equation as: first carrier- *k=1, E=1* so zero degrees for the first carrier, for the second carrier- *k=2, E=2* so $\pi/2$ degrees for the second carrier. In figure 2.11, a case of a 5-level inverter with *M=0.8* and $f_c/f_o=5$ is illustrated. It is apparent that each single-phase inverter is controlled using three-level modulation (unipolar modulation).

For the case of a five-level inverter with carrier phase shifts of 90°, harmonic cancellation up to sidebands around multiples of $4f_c$ will be achieved. For a seven-level inverter with carrier phase shifts of 60°, harmonic cancellation up to $6f_c$ will be achieved, and so on. If two-level modulation (bipolar modulation) was used, the carrier phase shift equation becomes $2(k\text{-}1)\pi/E$ thus harmonic elimination that can be achieved by this modulation is less. More specifically, the bipolar modulation can achieve harmonic elimination up to $E^{th}f_c$ where the unipolar case can eliminate up to $2E^{th}f_c$. Hence, bipolar modulation is not preferable for cascade multilevel inverters.

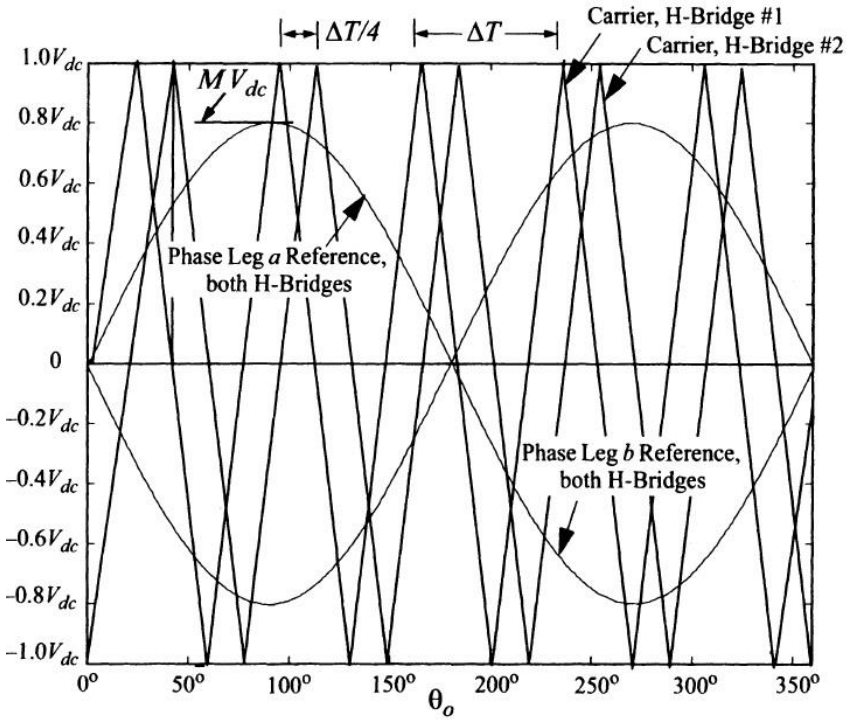


Figure 2.11 PSCPWM for five-level inverter with M=0.8 and $f_c/f_o=5$.

The unipolar technique can be considered as naturally sampled modulation and it is superior to symmetrical regular sampled modulation where cancellation will occur up to the E^{th} carrier multiple. On the other hand, asymmetrical regular sampled modulation can achieve the same results as naturally sampled up to the $2E^{th}$ carrier multiple. Obviously, the above are valid in linear region of the multilevel inverter 0<M<1. In Figure 2.12, the harmonic spectrum of the voltage output of PSCPWM is illustrated for a five level cascaded inverter.

Summarizing, among the carrier based pulse width modulation (PWM) techniques, PSCPWM technique is preferred for cascaded H-Bridge multilevel inverters. This technique distributes power evenly among the H-bridges and also ensures equal utilization of inverter switches within an H-bridge converter.

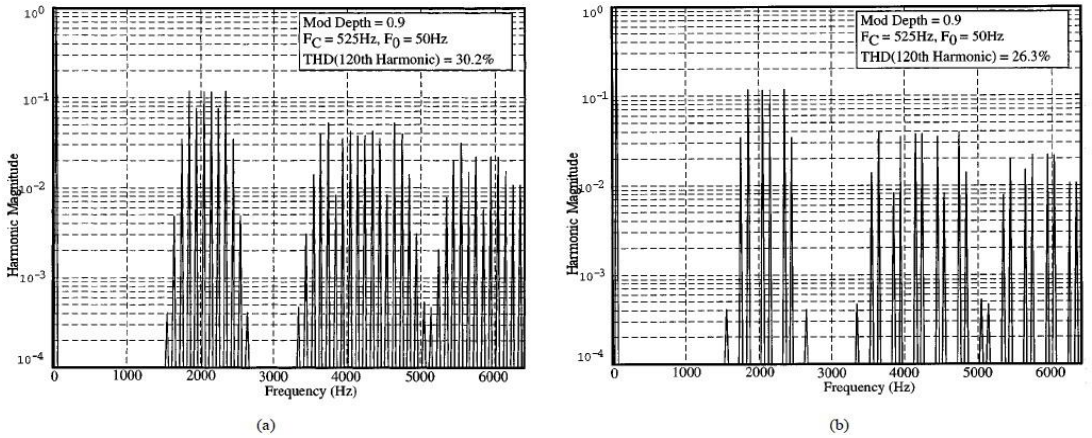


Figure 2.12 Five-level cascaded inverter, PSCPWM. (a) Phase leg voltage: analytical spectrum. (b) Line-to-line voltage: analytical spectrum

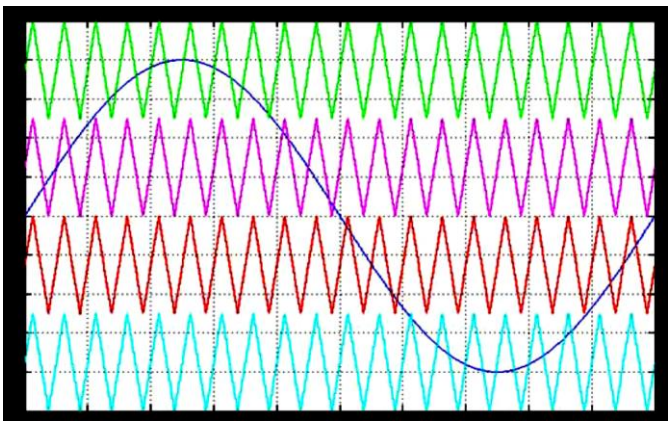
2.4.2 PWM strategies for Diode-Clamped Multilevel Inverters

The other major category of multilevel inverters is the diode-clamped circuits. Carrier-based strategies employed for conventional two-level modulation three-phase inverters can be extended to the multilevel diode-clamped circuit case. As mentioned before, since the benefits of harmonic cancellation are superior on the triangular (double edge) carrier modulation in a two-level modulation inverter, in a multilevel inverter only this approach will be

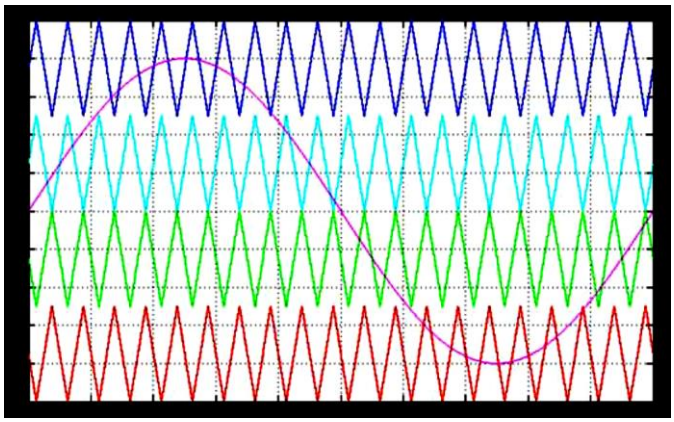
considered. By increasing the number of triangular carriers to *m-1,* where *m* is the number of voltage levels, double-edge modulation can be achieved. These carriers must be arranged in a manner that they fully occupy contiguous bands in the range of *–(m-1)Vdc/2* to *(m-1)Vdc/2* (for *m* odd). Then a single sinusoidal reference wave is needed to be compared with these carriers to determine the switching transitions of the inverter switches. Three alternative strategies can be produced by different phase relationships between the carriers. In the literature Carrara [29] clearly identified these alternatives.

- PD PWM: Phase Disposition, where all carriers are in phase across all bands.
- POD PWM: Phase Opposition Disposition, where the carriers above the reference zero point are out of phase with those below zero by 180^{o}.
- APOD PWM: Alternative Phase Opposition Disposition, where carriers in adjacent bands are phase shifted by 180^{o}.

Figure 2.13, illustrates these three alternative modulation strategies for a five level inverter. It is generally accepted that the PD method produces the lowest harmonic distortion in higher modulation ratios when compared with the other alternatives. This method is also applicable to cascade inverters [43]. POD and APOD methods are exactly the same for a three-level inverter.



(a)



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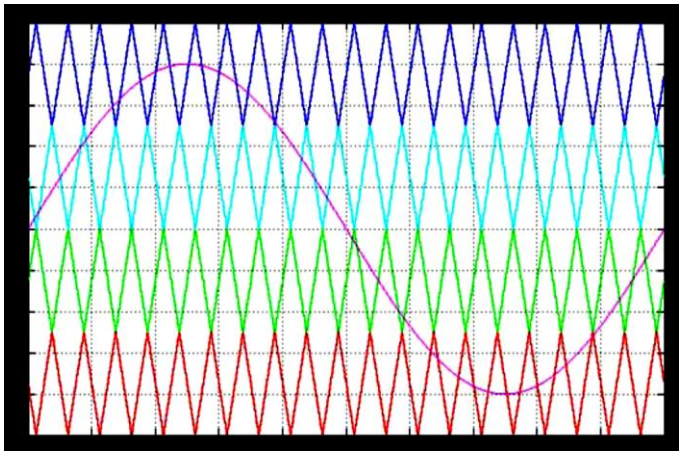

(c)

Figure 2.13 Diode-clamped PWM modulation alternatives for a five-level inverter: (a) PD, (b) POD, (c) APOD where $f_c/f_o=10$

On the other hand, POD has better harmonic results in lower modulation ratios. In this alternative, there is no harmonic on the carrier frequency and its multiples and the dispersion occurs around them. The third alternative -APOD, has similarities with the POD strategy and the major difference occurs on the amount of the third order harmonics that are greater on APOD. However, on a three-phase case, third order harmonics are cancelled in line voltages so the importance of that difference fades out resulting in a lower THD and becomes an advantage comparing it with POD. The harmonic spectrum for each alternative is illustrated in Figure 2.14 and 2.15, for a phase leg and line to line

voltage. The results for all voltage spectrums for each modulation alternatives are taken from McGrath and Holmes research and Ph.D thesis.

Comparing PD and APOD results, it can be concluded that line to line voltage THD for PD is close to one half of that for APOD. This shows the superiority of PD for line to line harmonic performance. This is because the phase leg spectrum of PD puts its most significant harmonic in the first carrier component, in contrast to APOD that only generates carrier sideband components. Thus, PD while placing significant harmonic content into the carrier components takes advantage of the common mode cancellation between the inverter phase legs to eliminate this carrier from the final line to line output.

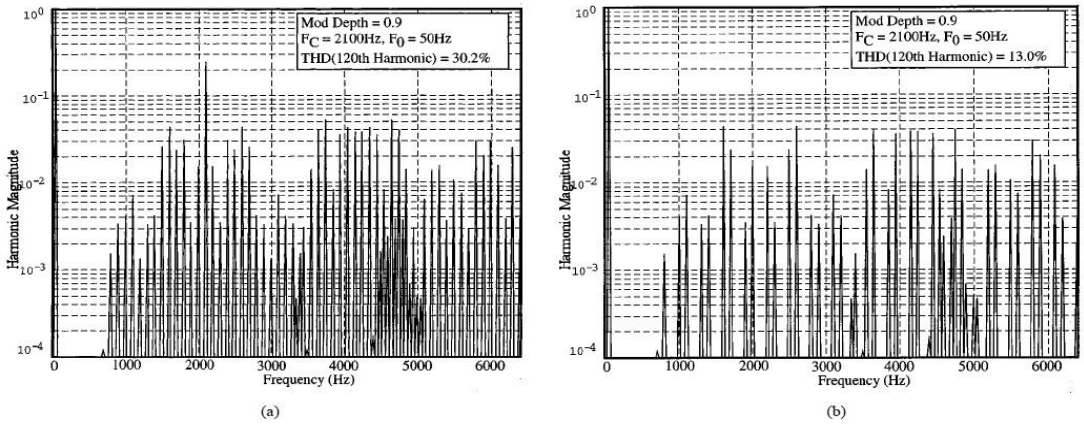

Figure 2.14 Five-level diode-clamped inverter, PD PWM. (a) Phase leg voltage: analytical spectrum. (b) Line-to-line voltage: analytical spectrum

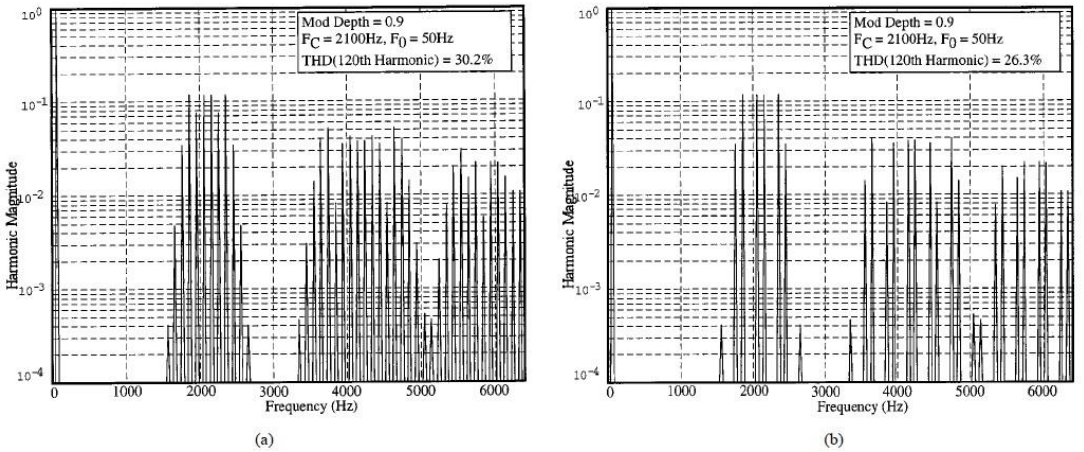

Figure 2.15 Five-level diode-clamped inverter, APOD PWM. (a) Phase leg voltage: analytical spectrum. (b) Line-to-line voltage: analytical spectrum

McGrath and Holmes in [41] also noted that PSCPWM has exactly the same harmonic magnitudes as for APOD PWM (for a 5-level inverter). The only difference is that the first group of sideband harmonics is centred around the carrier frequency for APOD, while in PSCPWM they are centred around the fourth multiple of the carrier frequency. However, since the total number of switching transitions for PSCPWM is exactly four times the number of switching transitions for APOD PWM, normalizing the switching frequencies the harmonic components become the same.

While POD and APOD do not introduce harmonic energy into the first carrier harmonic, in a three-phase case the APOD scheme is superior because it places more harmonic energy into the triplen sideband harmonics than POD. These triplen harmonics are then cancelled on a line to line basis, improving the performance of APOD strategy compared to POD.

As mentioned before, PD PWM can be implemented to cascaded inverters. Since this strategy is superior among the other alternatives, an equivalent PD for cascaded inverters has been developed from McGrath and Holmes [41]. Using discontinuous PWM with phase shifted carriers within each H-Bridge of each multilevel phase leg. The new modulation scheme gave similar improved harmonic performance as the PD modulation for diode-clamped inverter does.

2.4.3 PWM in Hybrid Multilevel inverter

While other topologies exist in the literature, like the flying-capacitor multilevel inverter, Hybrid MLI has been derived from the cascade structure [44, 45]. The hybrid inverter utilizes cascaded series inverters with different internal DC bus voltages and with different switching devices for the different DC levels. In the case of two series connected, single-phase converters with their DC bus voltages sized in the ratio of 2:1 (2 Vdc: Vdc) seven levels can be produced by this type of arrangement. This is very important in terms of reduced circuit complexity. While the two inverters are switched at different voltage levels

(high voltage level: 2 Vdc, low voltage level: Vdc) the high voltage cell will switch at fundamental frequency (using relatively slow switches like GTO's and IGCT's) and the low voltage cell will switch on a PWM scheme (using relatively fast switches like IGBT's). McGrath and Holmes also developed [45] an equivalent PD PWM for hybrid inverters.

2.4.4 Third-Harmonic Injection for Multilevel inverters

As with two-level inverters, third-harmonic injection can be implemented into the reference waveforms of a three-phase multilevel inverter as well. The switching frequency optimal PWM (SFOPWM) proposed by Steinke [46], which triples harmonic voltage, is added to each of the carrier waveforms. It actually takes the instantaneous average of the maximum and minimum of the three reference voltages and subtracts the value from each of the individual reference voltages to obtain the modulation waveforms.

$$V_{offset} = \frac{\max(V_a, V_b, V_c) + \min(V_a, V_b, V_c)}{2}$$
$$V_a = V_a - V_{offset}$$
$$V_b = V_b - V_{offset}$$
$$V_c = V_b - V_{offset}$$

This method could achieve a 15% increase on the modulation ratio range before overmodulation nonlinearities occur. In a three-phase case this simply occurs because of the reduced height of the three phase reference envelope that is achieved by third-harmonic injection. The effect of the third-harmonic injection is to transfer harmonic energy between sidebands, but not necessarily in an advantageous way. The main advantage remains the extension of the available linear modulation region, if this is required.

2.4.5 Overmodulation of Multilevel Inverters

It is possible to determine the behaviour of multilevel inverters in the overmodulation region for both naturally and asymmetric regularly sampled cases, using complex equations. While these equations are indeed quite complex after examination the complexity is mainly related with the magnitude of the harmonic components. Further, new harmonic components are created only in the baseband region with frequencies of $(2n-1)\omega_o t$. These harmonics produced by the overmodulation process can be identified as low-order odd harmonics since the effective reference waveform turns more to a square wave in a similar way as in two-level modulation. However, the advantage of harmonic cancellation of the sideband harmonics that occur in cascaded H-bridges is not affected by the overmodulation.

In three level inverters, overmodulation occurs when the commanded amplitude of the sinusoidal voltage exceeds the amplitude of the triangle wave carrier. Again, the behaviour of the multilevel inverter in a diode-clamped topology can be described by very complex equations as in the cascaded topology. However, the complexity is mainly related with the magnitude of the harmonic components and new harmonic components are created only in the baseband region with frequencies of $(2n-1)\omega_o t$. Similarly, these harmonics produced by the overmodulation process can be identified as low-order odd harmonics since the effective reference waveform turns more to a square wave in a way similar to two-level modulation. It is apparent that the only effect of overmodulation apart from the above is the magnitude of the switching harmonics and not their frequencies. Cancellation of the carrier harmonic and the triplen harmonics in the line to line voltage occurs again.

2.5 Summary

Summarizing, there are several techniques that can take advantage of special properties available in multilevel inverters. Control techniques for the determination of the switching angles in multilevel inverters can be classified into PWM, Selective Harmonic Elimination (SHEPWM), and Optimized Harmonics Stepped Waveform (OHSW) where further classification can be applied to open and closed loop as illustrated in Figure 2.16. This thesis is mainly focused in open loop PWM techniques. Techniques such as constant switching frequency, variable switching frequency, and phase shifted carrier pulse width modulation methods are used to minimize the total harmonic distortion and increase output voltage. In Figure 2.17, a comprehensive diagram is illustrating the variable control techniques used in multilevel inverters for determining the fundamental switching angles.

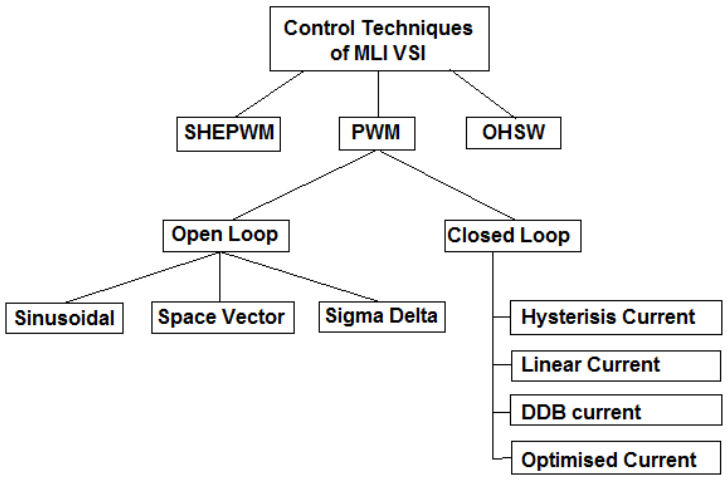

Figure 2.16 Control techniques for Multilevel Voltage Source Inverters

In literature, further classification can be seen by subdividing constant switching, variable switching and phase shifted pulse width modulations to Sub-harmonic PWM using only one modulation wave and Switching Frequency Optimal (SFO). Several researchers have been proposing new, novel, alternative PWM techniques based on the aforementioned multicarrier modulation

techniques. Radan and Shahirinia [32] suggested three new multicarrier techniques by simply re-arranging the carrier triangular signals over time and amplitude. Singh and Agarwal [35] considered a case of a three-phase five-level inverter, where Switching Frequency Optimal (SFO) is implemented in PD, POD and APOD PWM introducing new schemes by taking the instantaneous average of the maximum and minimum of the three reference voltages and subtracting the value from each of the individual reference voltage to obtain the modulation waveforms. This is actually a triplen harmonic added to each of the carrier waveforms. Variable Switching Frequency (VSF) pulse PWM has also been investigated by Palanivel and Dash [36] and Manasa, Parimala [37]. Super Imposed Carrier techniques are analysed by Kumar and Chinnaiyan, Jerome [38] where the carrier signal is super-imposed on the modulation signal. Fei, Zhang and Wu [39] have proposed a digital oriented SPWM for multilevel inverters and generalized for any levels and any topologies method. Using quarter wave symmetry and equality of areas three schemes where proposed claiming better harmonic results than level-shifted PWM schemes.

Space Vector (SV) method, can be readily extended to incorporate multilevel inverters. To avoid massive computational effort caused by the large number of states offered by a multilevel inverter, the SV method must be optimized. Optimized SV methods were introduced by Celanovic, & Boroyevich [41] and evolved by Gao and Fletcher [42] and Deng, Saeedifard and Harley [43]. McGrath and Holmes [44] identified a similar equivalence between PD carrier modulation and space-vector modulation, for diode-clamped, m-level cascaded and hybrid multilevel inverters. In this paper it is also shown how discontinuous modulation can be applied to multilevel inverters using zero sequence offset voltages derived from two-level inverter space vector concepts.

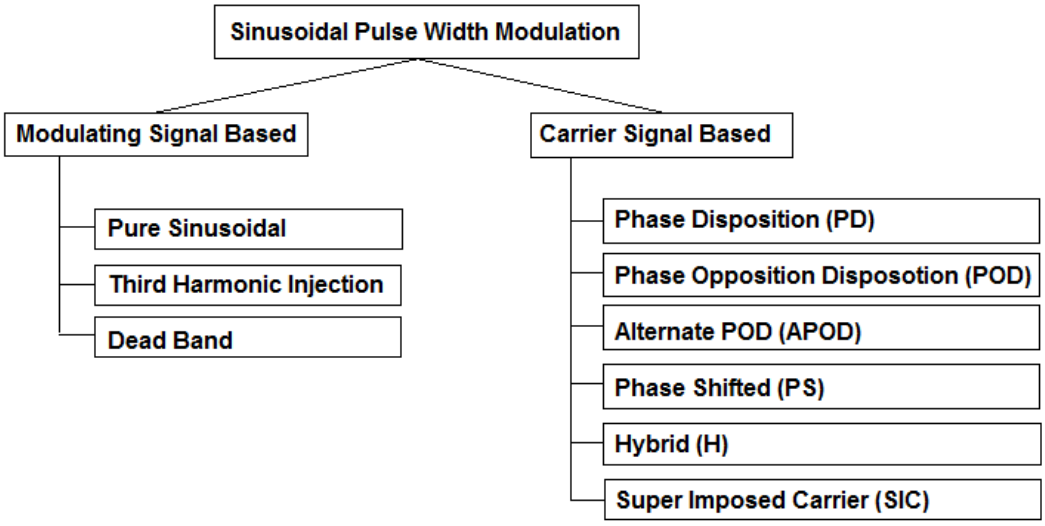

Figure 2.17. Classification of Sinusoidal PWM for Multilevel Inverters.

It is apparent from the literature review, that most of the research in our days is concentrated on the multicarrier modulation than the programmed digital oriented strategies. This is mainly because programmed PWM methods need large computational effort, and memory space adequate for storing large look-up tables to be used for the operation of the converter. These drawbacks limit the use of programmed PWM methods on an online system in a real time manner. The development of a programmed PWM technique that can be implemented in a real time manner taking in special consideration the ease of implementation and the concerns of computational effort is clearly needed in our days. Considering all of the above, in the following chapters, an alternative PWM method with a clear mathematical frame, simple trigonometric equations avoiding transcendental equations, and applying an algebraic theorem of equal areas has been used. In this thesis it is shown how this method has been evolved to be implemented in conventional and multilevel voltage source inverters.

CHAPTER 3

The Equal Areas PWM (EAPWM): An Alternative Approach to Pulse Width Modulation

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Introduction

In recent years several PWM techniques have been proposed for controlling the AC output of power electronic converters. The primary objective for all PWM schemes is to calculate the converter switching-on times in order to create the desired target output voltage [1]. The available schemes can be broadly classified as carrier-modulated PWM and programmed PWM schemes. Carrier modulated PWM schemes can be described by three fundamental types: modulation using naturally sampled sine wave-modulating wave intersections, regular sampling defined by sine wave-modulating wave intersections [2] and direct modulation [3]. The most common carrier based strategies are Sinusoidal PWM, Third Harmonic Injected PWM, Discontinuous or Dead Band PWM [4]. The actual PWM process in carrier modulated PWM methods is usually a simple comparison between a reference waveform and a saw tooth or a triangular carrier waveform. The ease of implementation on digital and analogue structures of these methods have made them widely accepted [5]. On the other hand the attenuation of wanted fundamental component of the output waveform, the increased switching frequencies and the generation of high

frequency harmonic components previously not present, are their main drawbacks [6]. Sophisticated techniques such as PWM harmonic elimination [7], [8], [9], Optimized Space Vector PWM or Optimal Switching Pattern PWM [10] have been developed to overcome these drawbacks. Many PWM techniques have been proposed for the rising multilevel inverters including multicarrier PWM [11], or harmonic elimination with programmed PWM methods [12] or even based on genetic algorithms [13]. The main disadvantage of these programmed PWM techniques is that for their practical implementation complicated algorithms for transcendental equations need large computational power [14]. Each method has different characteristics, advantages and disadvantages regarding the ease of implementation, harmonic spectra and maximum modulation index or switching losses.

Aiming at simplifying the implementation of a PWM-based system, this chapter presents a direct approach of programmed PWM modeling. The theory of equal areas that this chapter is focusing on has been presented in [3], [15] and [16]. The method has been analyzed and generalized for accurate production of the pulse-train with odd number of pulses. Simulation results are derived using MATLAB. The spectrum of the output is following the symmetric regular sampling discontinuous PWM pattern [2]. The total harmonic distortion is calculated using the equations derived for marginal values of the amplitude modulation ratio (m_a) inside the linear region of operation. Practical work has been carried out verifying the simulation results. The chapter is divided in five parts. In the first part, a review of the first approach with linear segments of Equal Areas PWM is given. In the second part, the accurate and analytical method for the Equal Areas PWM (EAPWM) pulse-train generation is analyzed. In the third part, the harmonic analysis of the output using the FFT is carried out. In the fourth part the calculation for the marginal amplitude modulation ratio is presented followed by the calculation of the Total Harmonic Distortion THD. In the last part simulation and experimental results are presented.

3.1 The equal areas theory using rectilinear segments

D. Nafpaktitis et al. [15] present and recapitulate the mathematical framework for the production of well-defined PWM pulses using equations that describe with satisfactory accuracy the width, the firing time and the ending time of each pulse. The EAPWM method can be briefly described as follows: A sinusoidal voltage signal can be approximated using rectilinear segments which define intervals with duration d as depicted in Figure 3.1. For each interval there is a corresponding pulse with amplitude U_{pmax}, active time t_P and inactive time t_δ. The active time t_P can be computed applying the condition of equal areas [11]. Each pulse is centered in its corresponding interval. In order to successfully approximate the sinusoidal target waveform using PWM, two crucial parameters are needed to be formulated: the pulse width/active time t_{pJ} at a J interval and its corresponding firing time $t_{\varepsilon J}$, derived by the area equality:

$$t_{pJ} = \frac{d}{2} \cdot \frac{U_{\max}}{U_{p\max}} \left\{ \sin\left[\left(J-1 \right) \omega \cdot d \right] + \sin(J \cdot \omega \cdot d) \right\} \tag{3.1}$$

$$t_{\varepsilon J} = \left(J-1 \right) d + \frac{1}{2} \left(d - t_{pJ} \right) \tag{3.2}$$

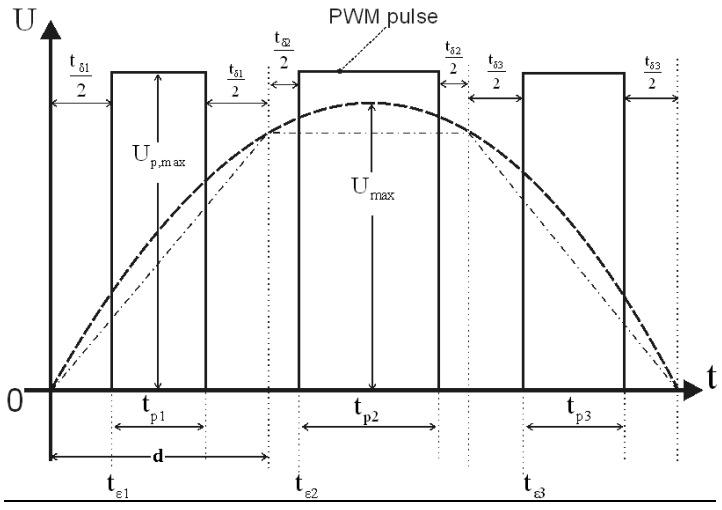


Figure 3.1 Approximation of sinusoidal voltage signal (dashed curve) by rectilinear segments (dot-dashed curve)

The approximation of the sinus wave (dashed curve) was firstly used in this research. The results showed significant deviations on low switching frequencies and that was the reason of choosing the integral of the actual reference waveform, since the computational effort was not changing drastically. The flow chart of the proposed PWM strategy is presented below in Figure 3.2.

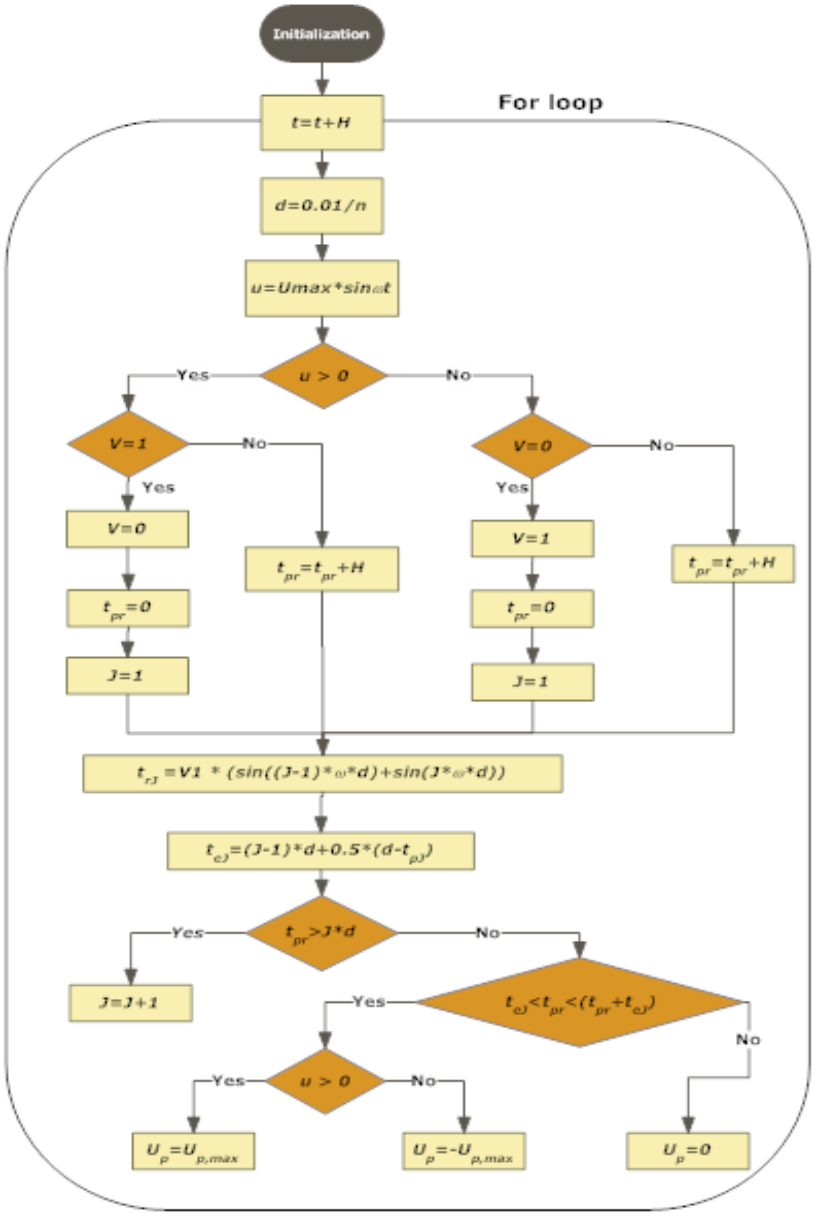


Figure 3.2 Flowchart for the calculation of pulses duration and firing times for the proposed PWM strategy.

3.2 Generation of the optimized and accurate EAPWM pulse

An example for producing accurate EAPWM pulses is presented. In EAPWM only odd pulse numbers per half cycle will be studied. The reason for this is that since the maximum necessity for amplitude is needed at the middle of the sinus wave (π/2 and 3π/2) then the center pulse must be present in the PWM pulse train to produce the needed amplitude. As per Figure 3.3 and assuming that the half sinusoidal signal can be split in five equal intervals (with duration *d*), the pulse's active time t_P (i.e. t_{p2} for the 2nd interval) can be found, beginning with the assumption that the area of the pulse (defined by ABCD points) must be equal with the area defined by EFGH points. Thus, using the integrals of the areas:

$$E_{ABCD} = E_{EFGH} \tag{3.3}$$

Eq.(3.3) can be expressed as following:

$$\omega t_{p_2} U_{p\max} = \int_{\omega d}^{2\omega d} U_{\max} \sin(\omega t) d\omega t \tag{3.4}$$

Solving Eq.4 leads to

$$t_{p_2} = \frac{U_{\max}}{\omega \cdot U_{p\max}} (\cos \omega d - \cos 2\omega d) \tag{3.5}$$

In generalized form, the pulse active time t_P in *j* interval will be:

$$t_{pJ} = \frac{U_{\max}}{\omega \cdot U_{P\max}} \left\{ \cos\left[(J-1)\omega d \right] - \cos(J\omega d) \right\} \tag{3.6}$$

where U_{Pmax} corresponds to the available DC link, J expresses the number of intervals (or equivalently the number of pulses A_p) that corresponds to a half period T/2 time. So, A_p and *d* are related as follows:

$$A_p = \frac{0.5T}{d} \tag{3.7}$$

The switching frequency over a complete fundamental cycle is then calculated as:

$$f_s = \frac{1}{d} = \frac{2A_p}{T} \tag{3.8}$$

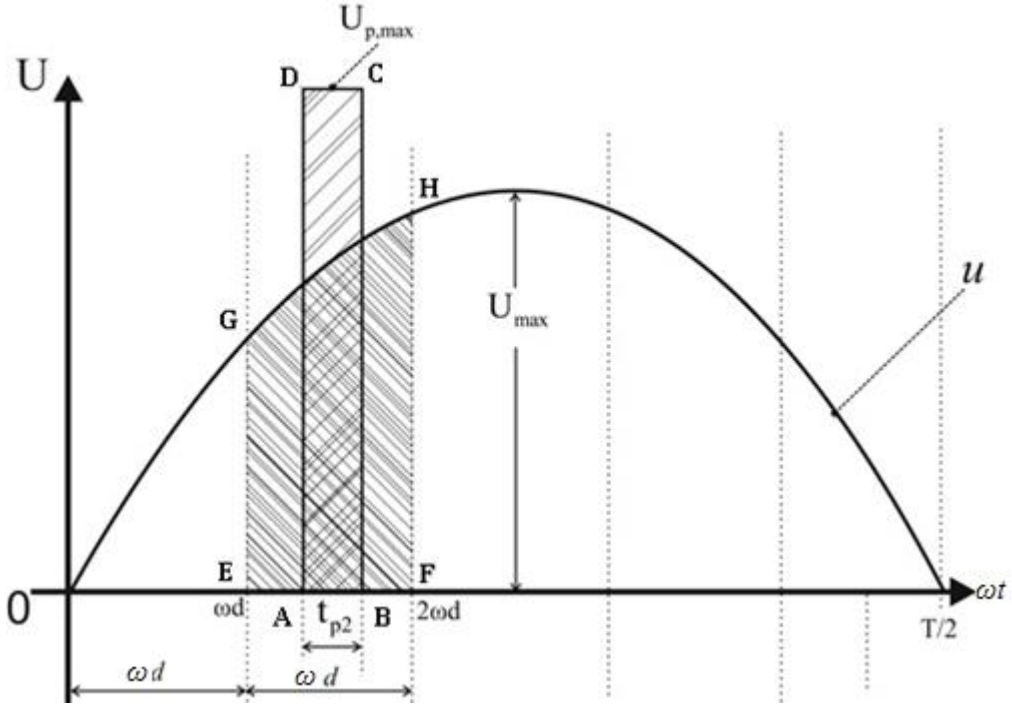


Figure 3.3 Generation of an accurate EAPWM pulse.

However, the phase leg switching frequency in discontinuous PWM schemes is modulated only for the 50% of the fundamental cycle (here it can be expressed as f_p=Ap/T since only one phase leg is being modulated). The frequency modulation ratio is defined as $m_f=f_s/f_0$ and amplitude modulation ratio or duty factor DF is defined as m_a=DF=U_{max}/U_{Pmax}. For odd A_P there is a central pulse at positions T/4, 3T/4, 5T/4, 7T/4 etc. where at sides (A_P-1)/2 symmetrical pulses occur. Using Eq.3.6 and Eq.3.2 we can calculate t_{Pj} active times and $t_{\varepsilon J}$ firing times respectively.

3.2.1 Evaluation of the Marginal m_a and Harmonic Analysis of the Voltage output.

The decrease of $U_{p,max}$ value, implies a corresponding increase at the duration of the pulse. The value of modulation index m_a cannot be set higher than one because overlaps between the pulses will occur (first overlap is going to take place on the centred-middle pulse). The necessity here is to decrease the $U_{p,max}$ in such a level where the corresponding duration of the pulse, t_p, will be less or equal to space ωd. Then, as shown in Figure 3.4, the $U_{p,max}$ will occur between U_{max} and $\overline{FE}$. The minimum $U_{p,max}$ ($U_{p,max\text{-}min}$, U_{pmm} hereafter) can be calculated using the equation where, the area ABCD must be equal with the hatched area ABEGF. This equation is formulated as:

$$\omega d \cdot U_{pmm} = \int_{\frac{A_p-1}{2}\omega d}^{\frac{A_p+1}{2}\omega d} U_{\max} \sin(\omega t) d\omega t \qquad (3.9)$$

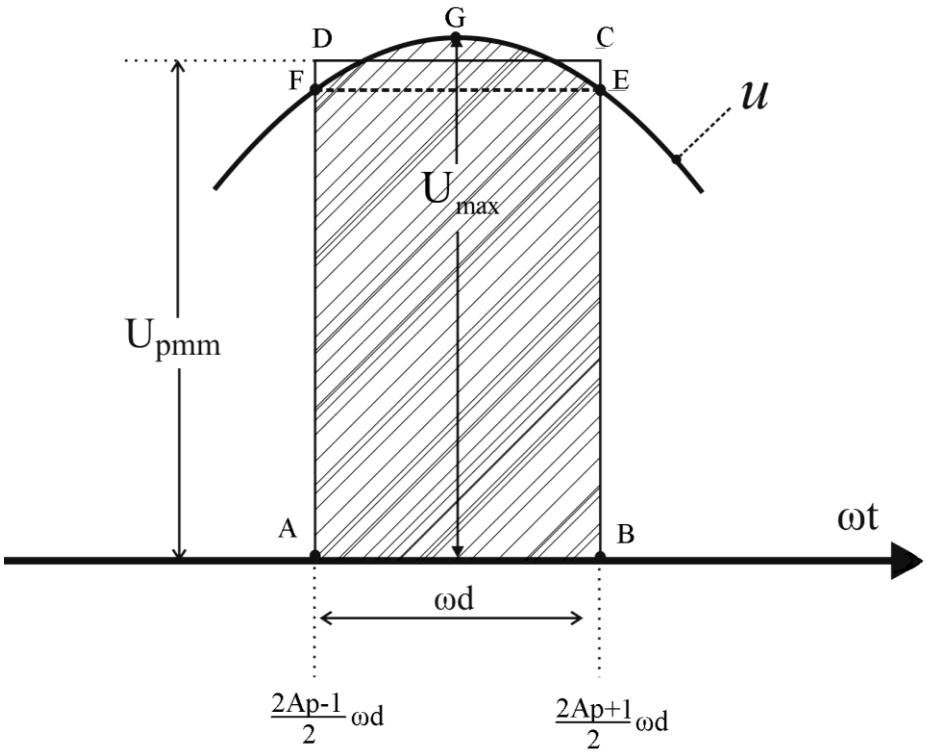


Figure 3.4 Calculation of U_{pmm}

Solving Eq.3.9 in relation to U_{pmm} becomes

$$U_{pmm} = U_{\max} \frac{2A_p}{\pi} \sin\left(\frac{\pi}{2A_p}\right) \tag{3.10}$$

But since:

$$\lim_{A_p \to \infty} \left(\frac{2A_p}{\pi} \sin\left(\frac{\pi}{2A_p}\right) \right) = 1 \tag{3.11}$$

It holds that:

$$\lim_{A_p \to \infty} U_{pmm} = U_{\max} \tag{3.12}$$

From Eq.3.12 one can deduce that for high switching frequency of pulse-train (high A_p values) the U_{pmm} coincides with U_{max} . Table 3.1, presents some indicative values of the optimum-marginal modulation index ratio (U_{max} /U_{pmm}) in relation with A_p that correspond to minimum THDv.

Table 3.1. Representative values of $m_a = U_{max} / U_{pmm}$ ratio in relation with A_p for minimum THDv

A_p	**$m_f = f_s / f_0$**	**$m_a = U_{max} / U_{pmm}$**
3	6	0.95493
5	10	0.98363
11	22	0.99163
…	…	…
15	30	0.99817
…	…	…
25	50	0.99934

3.2.2 Harmonic Analysis of the EAPWM using FFT.

Recalling the generalized Fourier equations

$$u(t)=\{a_0/2+a_1\cos\omega t+a_2\cos\omega t+a_3\cos\omega t+.....+b_1\cos\omega t+b_2\cos\omega t+b_3\cos\omega t+....\} \quad (3.13)$$

$$a_n=\frac{1}{\pi}\int_0^{2\pi}u(t)\cos(n\omega t)d\omega t \quad (3.14)$$

$$b_n=\frac{1}{\pi}\int_0^{2\pi}u(t)\sin(n\omega t)d\omega t \quad (3.15)$$

The term $\alpha_0/2= 0$ for *AC* signals. The coefficients α_n are also zero since the function u(t) is odd and the following equation holds

$$u(-t)=-u(t)\Rightarrow a_n=0 \quad (3.16)$$

At the same time, the b_n coefficients are zero due to half wave symmetry

$$u(t)=-u(t+\frac{1}{2}T) \quad (3.17)$$

the b_n coefficients are also zero for *n* even:

$$n:even\Rightarrow b_n=0 \quad (3.18)$$

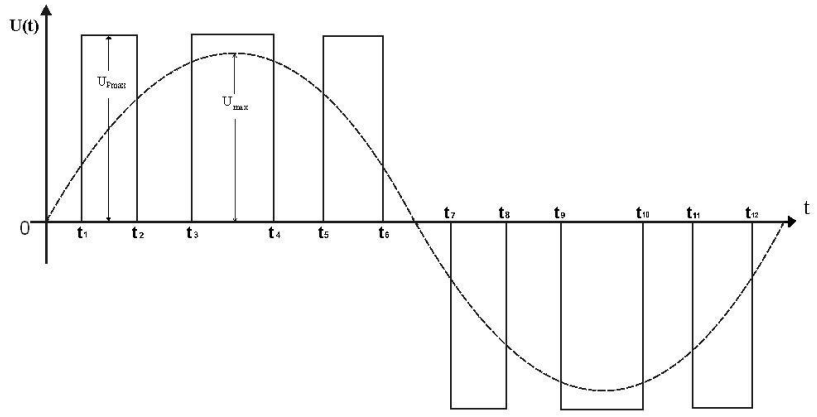


Figure 3.5 Time assignment at the beginning and at the end of each pulse.

Assigning the times t_1, t_2, t_3, t_4 ..... t_n at the beginning and the end of each pulse (as presented in Figure 3.5), the following equation for b_n coefficients is derived:

$$b_n = -\frac{4U_{p\max}}{n\pi}\left(-\cos(n\omega t_1)+\cos(n\omega t_2)-\cos(n\omega t_3)+.....-\cos(n\omega t_{A_p})\right) \tag{3.19}$$

where A_p defines the number of pulses. Eq.15 can be rearranged as below:

$$b_n = -\frac{4U_{p\max}}{n\pi}\sum_{k=1}^{k=A_p}(-1)^k\cos(n\omega t_k) \tag{3.20}$$

For the pulses' function u(t) becomes:

$$u(t)=\left\{b_1\sin(\omega t)+b_3\sin(\omega t)+b_5\sin(\omega t)+.....+b_n\sin(\omega t)+.....\right\} \tag{3.21}$$

With *n* odd integer, it holds:

$$u(t)=\sum_{n=1,3,5,..}^{\infty}b_n\sin(n\omega t) \tag{3.22}$$

Or equivalently:

$$u(t)=\sum_{n=1,3,5,...}^{\infty}\left[-\frac{4U_{p\max}}{n\pi}\sum_{k=1}^{k=A_p}(-1)^k\cos(n\omega t_k)\right]\sin(n\omega t) \tag{3.23}$$

The firing and closing time t_k of the *J* pulse in respect to duration t_{pJ} and $t_{\varepsilon J}$

$$J=\frac{1+2k+(-1)^{k+1}}{4} \tag{3.24}$$

$$t_k = t_{\varepsilon J}+[\frac{1+(-1)^k}{2}]t_{pJ} \tag{3.25}$$

3.3 Calculation of Total Harmonic Distortion

The Total Harmonic Distortion of Voltage is expressed (per cent) by the following expression:

$$THDv = 100\sqrt{\left(\frac{U_{rms}}{U_{1,rms}}\right)^2 - 1} \tag{3.26}$$

In order to calculate the THDv one must calculate the rms value of pulse-train, U_{rms} as well as the rms value of 1st harmonic of pulse-train, $U_{1,rms}$. For U_{rms} with A_p=3, and U_{dc} as the voltage DC link:

$$U_{rms} = U_{dc}\sqrt{\frac{2}{T}\left(2t_{p_1} + t_{p_2}\right)} \tag{3.27}$$

For A_p=5,

$$U_{rms} = U_{dc}\sqrt{\frac{2}{T}\left(2t_{p_1} + 2t_{p_2} + t_{p_3}\right)} \tag{3.28}$$

Eq.23 & Eq.24 concludes to a general expression for U_{rms}

$$U_{rms} = U_{dc}\sqrt{\frac{2}{T}\left(2t_{p_1} + 2t_{p_2} + ... + 2t_{p_{n-1}} + t_{p_n}\right)} \quad \text{with} \quad n = \frac{1+A_p}{2} \tag{3.29}$$

Substituting in Eq. 3.29, the t_{pj} terms from Eq. 3.6 and solve, many coefficients will be equal to zero. This will transform Eq. 3.25 to a new expression:

$$U_{rms} = \sqrt{\frac{2\cdot U_{grid}\cdot U_{dc}}{\pi}\left\{1 - 0.5\cos\left[\left(\frac{A_p - 1}{2}\right)\frac{\pi}{A_p}\right] - 0.5\cos\left[\left(\frac{A_p + 1}{2}\right)\frac{\pi}{A_p}\right]\right\}} \tag{3.30}$$

It is easy to prove that the result between brackets equals 1. Thus,

$$U_{rms} = C \cdot \sqrt{U_{dc}}$$
$$\text{with} \quad C = \sqrt{\frac{2U_{grid}}{\pi}} \tag{3.31}$$

Eq. 3.31 dictates that the voltage U_{rms} is independent by the number of pulses A_p and with constant U_{grid}, U_{rms} is affected only by U_{dc}.

The *rms* value of 1st harmonic, $U_{1,rms}$ can be calculated using Eq. 3.15 as $U_{1,rms} = \frac{b_1}{\sqrt{2}}$ or

$$U_{1,rms} = 0.9U_{dc}(\cos\omega t_1 + \cos\omega t_2 + ... + \cos\omega t_{A_p}) \tag{3.32}$$

Or alternatively

$$U_{1,rms} = -0.9U_{dc}\sum_{k=1}^{k=A_p}(-1)^k \cos\omega t_k \tag{3.33}$$

The *k* coefficients and the times t_k derived from Eq. 3.24 and Eq. 3.25

The minimum THDv corresponds to the best possible EAPWM pulse-train. This is achieved by increasing the frequency of pulse-train (high A_p values) or margining-"optimising" the value of the modulation index ratio $m_a=U_{max}$ / U_{pmm} using Eq. 3.23.

Considering the values of U_{pmm} shown on table 1 and using Eq. 3.6 and Eq. 3.23, the maximum active time for a pulse at interval *J* for U_{pmm}, can be calculated as below:

$$t_{p_{J\max}} = \frac{T}{4A_p}\frac{\left\{\cos\left[(J-1)\frac{\pi}{A_p}\right] - \cos\left(J\frac{\pi}{A_p}\right)\right\}}{\sin\frac{\pi}{2A_p}} \tag{3.34}$$

Solving Eq. 3.33 one can find that the limit of $U_{1,rms}$ for high values of A_p, is the rms value of sinusoidal voltage $u=U_{max}sin\omega t$ which is $U_{max}/\sqrt{2}$. Thus,

$$\lim_{A_p \to \infty} U_{1,rms} = \frac{U_{\max}}{\sqrt{2}} \tag{3.35}$$

Substituting Eq. 3.35 and 3.31 to Eq. 3.26 the minimum value of THDv holds as:

$$THDv_{\min} = 100\sqrt{\frac{4 \cdot U_{p\max}}{\pi \cdot U_{\max}} - 1} \tag{3.36}$$

From Eq. 3.36 one can presume that for constant U_{max}, $THDv_{min}$ is affected only by $U_{p,max}$ thus the ratio $m_a=U_{max} / U_{pmax.}$

In Figure 3.6 and 3.7, a range of THDv series vs. A_p is plotted, using the marginal modulation index ratio $m_a=U_{max} / U_{pmm}$. The number of pulse A_p indicates also the switching frequency as described in Eq. 3.8. In Figure 5, THDv is calculated using Eq. 3.26. For $A_p>11$ all the THDv values coincide to corresponding minimum values, $THDv_{min}$. The U_{pmm} for $3 \geq A_p \geq 11$ is lower even than U_{max}. For $A_p \geq 12$, $THDv=THDv_{min}$ which is 52.27% as calculated from Eq. 3.36.

Since Eq. 3.26 is applied to a full bridge inverter, it can be assumed that by proper control [18] the negative and positive semi-periods of the voltage output are symmetrical meaning no DC or even harmonics are present, the total harmonic distortion can be reduced to

$$THD = \sqrt{\sum_{n=3,5,7,..}^{\infty} \left(\frac{U_n}{U_1} \right)^2} \tag{3.37}$$

To calculate accurately the THDv, it is usually necessary to calculate all the significant side-band harmonics up to the fifth harmonic of the carrier. The frequency carrier depends on the number of pulses A_p (or the frequency modulation ratio m_f used). Calculating until the 899^{th} harmonic and until $A_p=79$

(f_s=7.9 kHz) as calculated from Eq. 3.37 the THD vs. A_p is shown in Figure 3.7. The DC link voltage Udc is chosen as the Ugrid (311.127 volt). The minimum THDv is achieved for A_p=77 which is 48.88%. It has to be remembered that on the conventional unipolar SPWM each phase leg is switching at a frequency derived from the carrier signal frequency f_s. Since only one phase leg is modulated, the carrier ratio for discontinuous modulation has to be double to all examples to achieve the same number of switch transitions for each phase leg over a complete fundamental cycle to compare it with the natural or regular sampled PWM schemes. So, for example if one would like to compare the results of case A_p=21 (i.e. f_s=2.1 kHz and f_p=1.05 kHz), they would have to compare it with carrier frequency f_s=f_p=1.05kHz of a regular or natural sampled PWM in order to achieve the same switching transitions. The advantage of discontinuous PWM is that phase legs are stressed less than conventional PWM schemes.

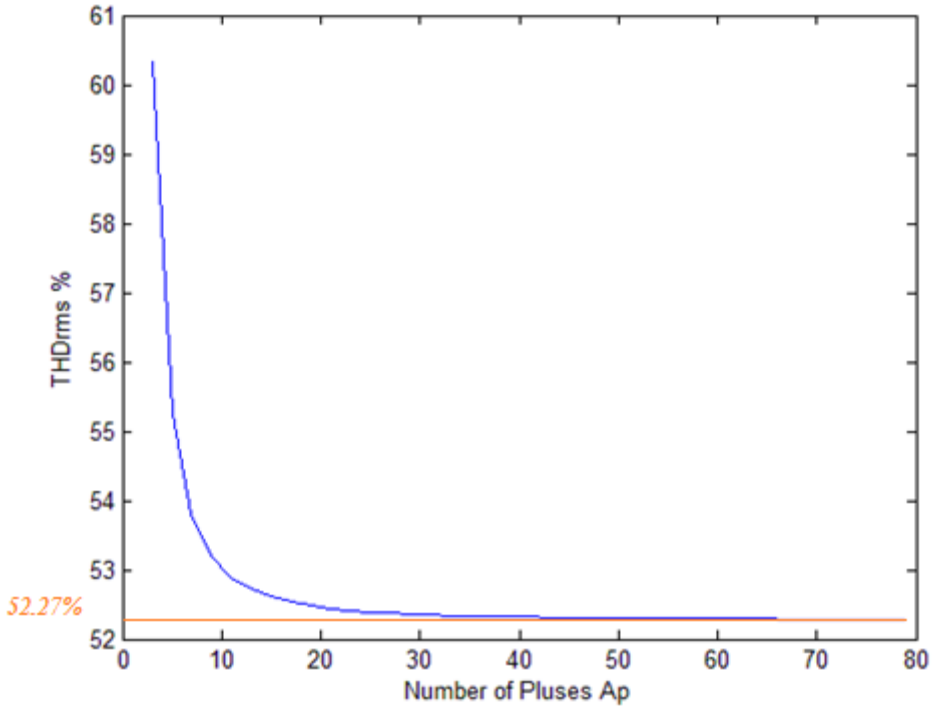


Figure 3.6 THDv series vs. number of pulses (A_p) using marginal m_a, calculated by eq. (26).

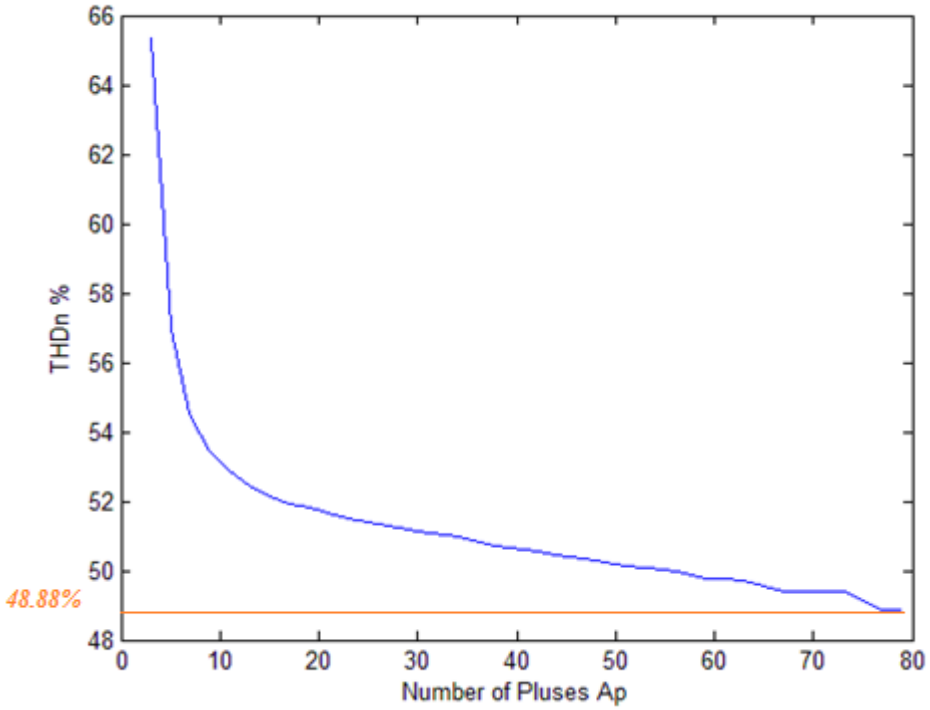


Figure 3.7 THDv vs. Number of pulses (A_p) using marginal m_a, calculated by eq.(3.37).

3.4 Simulation and experimental results

To verify the proposed method, two simulation and practical scenarios with two different numbers of pulses are implemented. In the first case A_p=11 is used, meaning a frequency modulation ratio of m_f =22 and switching frequency of phase leg, f_p=550 Hz. In the second case A_p=21 is used meaning a frequency modulation ratio of m_f =42 and switching frequency for each phase leg at f_p=1.05 kHz. The simulation voltage output for both cases and its normalised FFT analysis are shown in Figures 3.8, 3.9, 3.10, 3.11, respectively and calculated for both cases until the 100th harmonic. The m_a =U_{max} /U_{pmm} ratio for both cases is the optimum-marginal. The proposed method is to be used for a grid tie VSI. Since for linear operation modulation ratio has to be kept below unity (m_a<1) the inverter never enters the over modulation region. As expected for unipolar discontinuous PWM the low order harmonics are clustered around multiples of m_f rather than 2m_f [17]. However, discontinuous

switching halves the phase leg switching frequency for the same carrier frequency, since each phase leg is only modulated for 50% of the fundamental cycle. The DC link voltage Udc for simulation cases is chosen at 311.12 Volt and for connection with the utility grid. For both cases $U_{1,rms}$ indicates the RMS voltage amplitude of the fundamental harmonic.

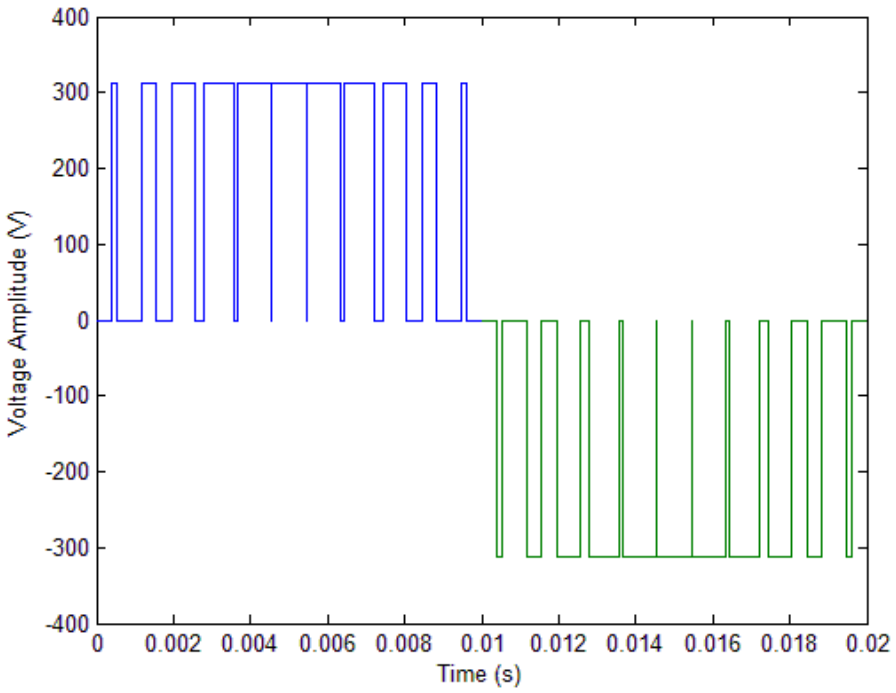


Figure 3.8 Voltage Output for A_p=11 (f_p=550 Hz).

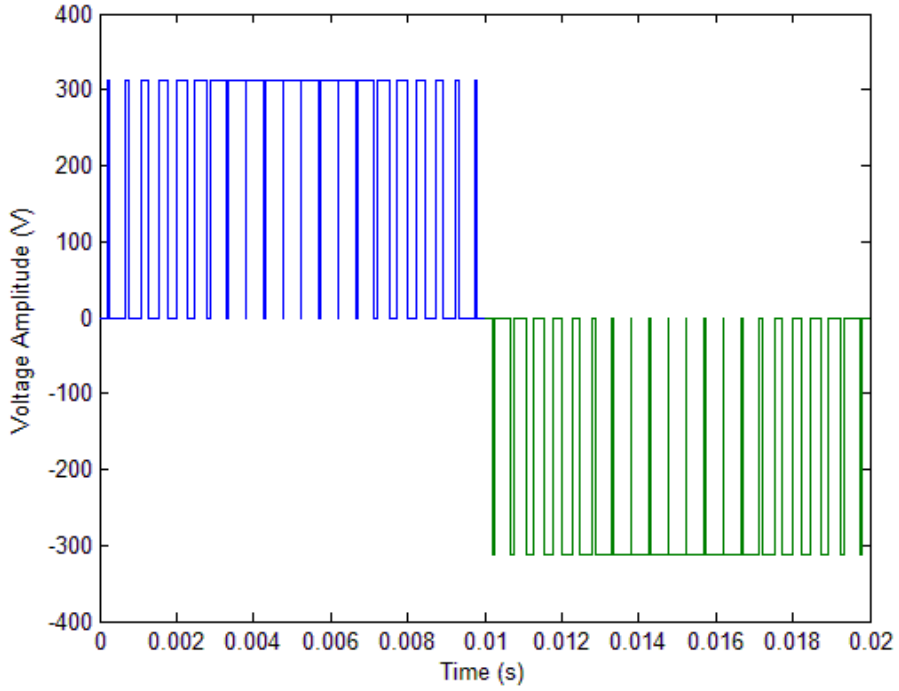
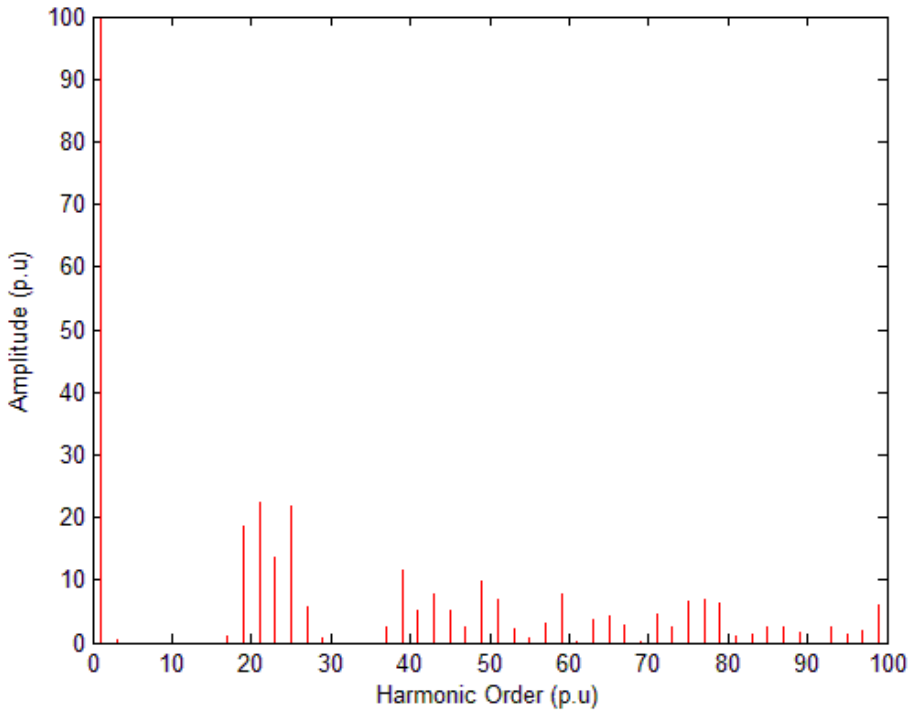


Figure 3.9 Voltage Output for A_p=21 (f_p=1250 Hz).



. *Figure 3.10 Voltage Spectrum for A_p=11 (f_p=550 Hz, m_a=0.9966, THD=51.0845 %, $U_{1,rms}$=219.4 V).*

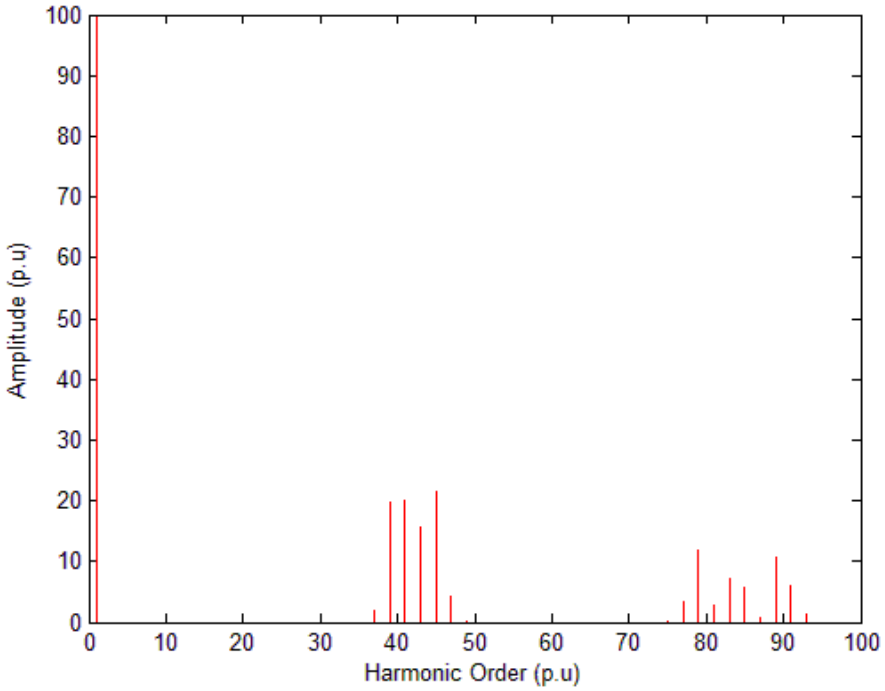


Figure 3.11 Voltage Spectrum for A_p=21 (f_p=1250 Hz, m_a=0.99907, THD=48.4495 %, $U_{1,rms}$=219.8 V).

For simulation purposes, besides MATLAB for numerical and harmonic analysis, Proteus ISIS was used to simulate the whole system along with all switching devices, MOSFET drivers and the AVR microcontroller programming. Proteus ISIS 7 Professional is a powerful tool since it can simulate the whole system at once, taking in consideration both the microcontroller programming and the electrical variables of the circuit elements. In Figures 3.11-3.15 below the schematic used for the simulation with Proteus ISIS 7 Professional is shown as well as the results of FFT harmonic Analysis and the voltage output for A_p=11, f_s=1.1 kHz switching frequency and maximum modulation index. In Figure 3.12, the full schematic circuit is illustrated. The PWM signals produced by the AVR microcontroller are driven to simple transistors (BD649) for pull-up to 12 volts fin order to feed the IR2110 driver. Then, the IR2110 drivers send the PWM signal to power switches IRF830 of the full bridge.

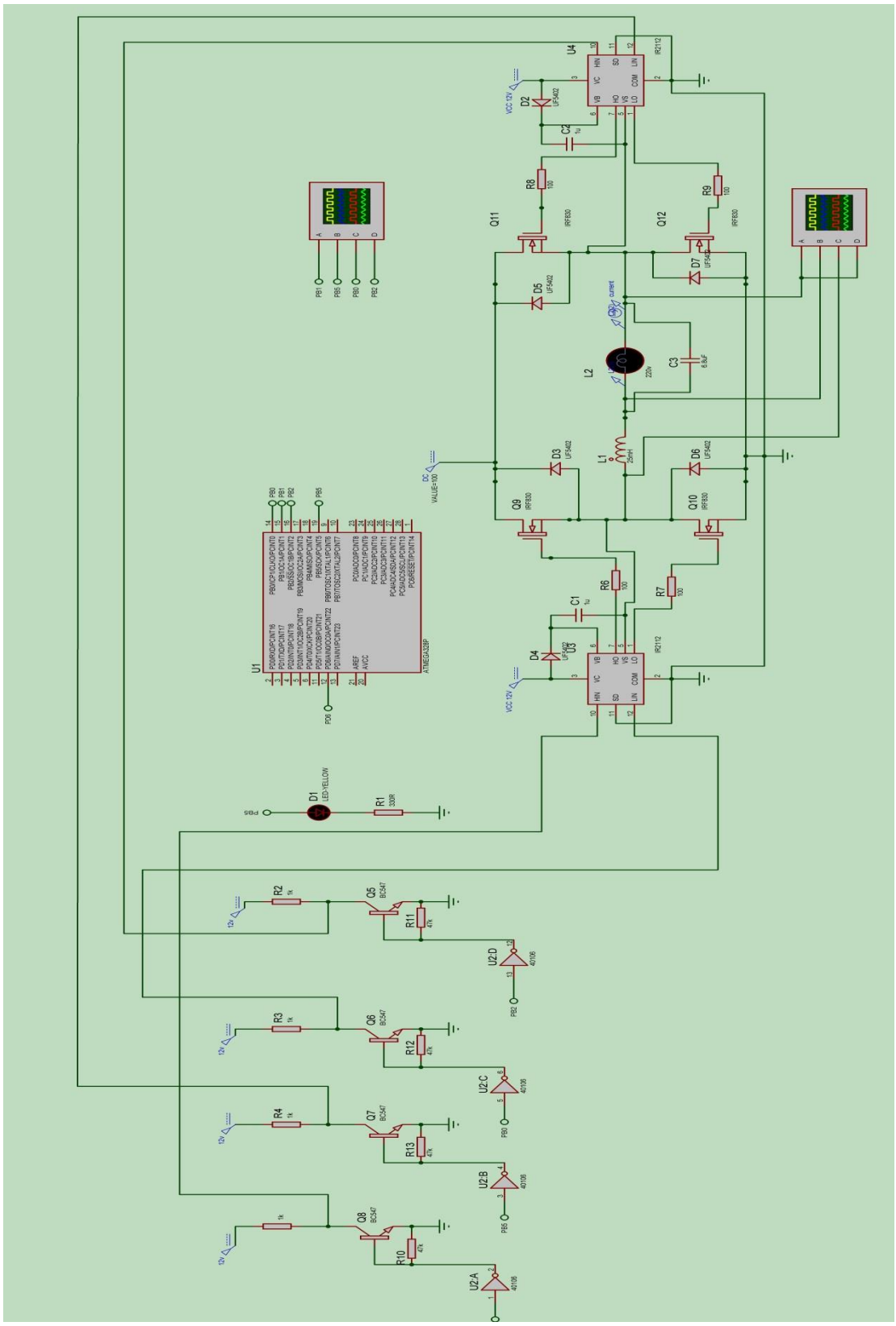


Figure 3.12 Schematic used for Proteus ISIS 7 Professional.

The PWM signals generated for number of pulses A_p=11 (fs=1.1 kHz) by the AVR microcontroller are illustrated in Figure 3.13.

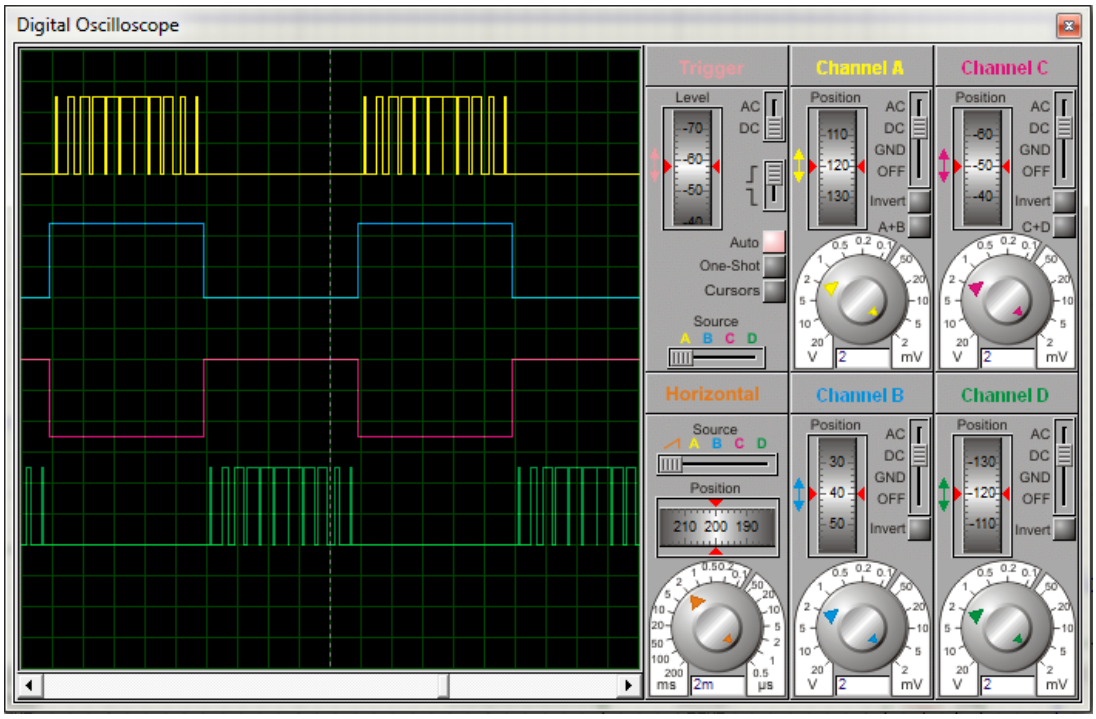


Figure 3.13 PWM signals generated for number of pulses Ap=11 (fs=1.1kHz) by the AVR microcontroller.

In Figure 3.13 it is clear how the signals are driven to the inverter switches using the discontinuous PWM scheme. The one leg is switching at the half of the carrier frequency while the other leg is switching at fundamental frequency. The modulation index is calculated using the marginal m_a. In the case of A_p=11 the marginal modulation index is m_a=0.99163 (from Table 3.1). The output voltage of the full-bridge inverter without using any filtering is illustrated in Figure 3.14. The DC link is set to 100 volts in order to compare it with practical results generated in the lab where a DC link of 100 volts was also used.

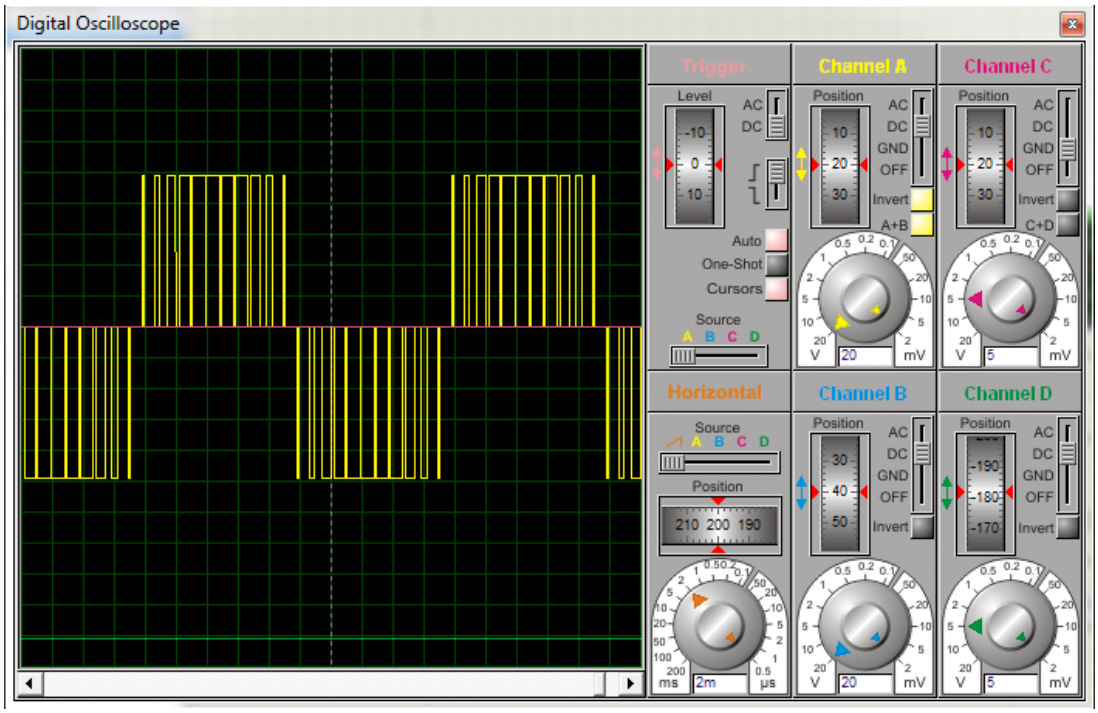


Figure 3.14 The output voltage of the full-bridge inverter without using any filtering.

In Figure 3.15, Fourier Analysis using Proteus is illustrated for number of pulse A_p=11 (fs=1.1 kHz).

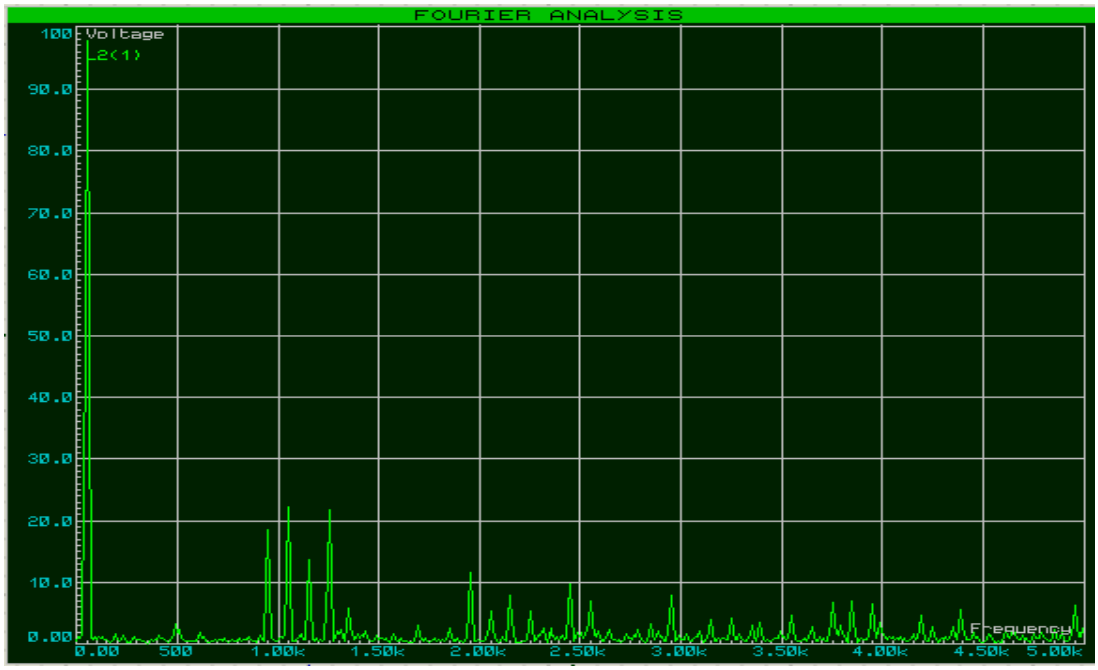


Figure 3.15. Fourier Analysis using Proteus for number of pulse A_p=11.

In Figure 3.16 the voltage and current output is illustrated using the LC filter of 10 mH inductor and 6.8 uF capacitor.

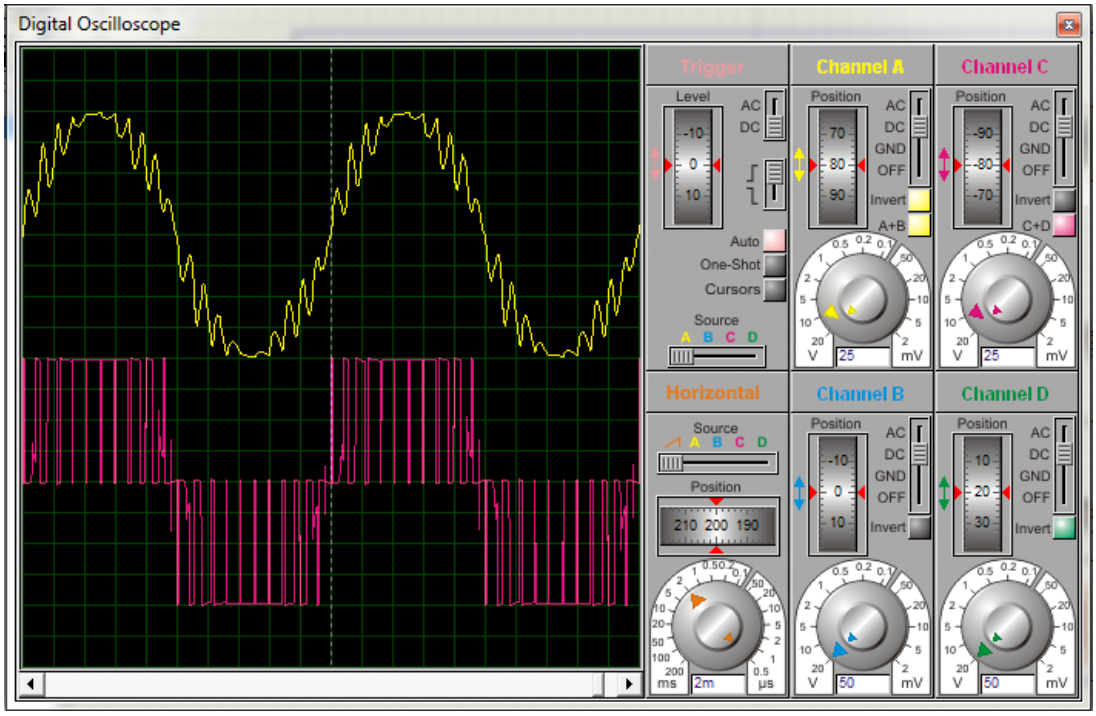
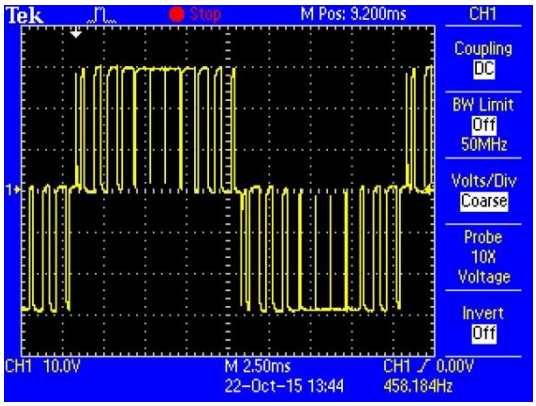


Figure 3.16 Voltage and current output waveforms using LC filter at the output.

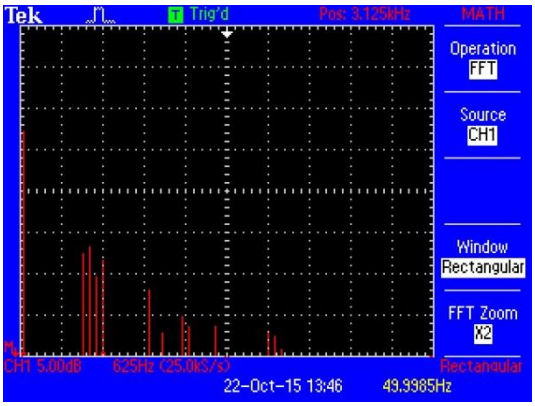
The program used for programming the AVR microcontroller was CodeVisionR. The full code of programming the PWM signals using the equal areas method is provided in appendix [B1].

For experimental implementation a prototype inverter was constructed. The PWM scheme was implemented in MOSFETs IRF840 using an ATMEL ATMEGA328P. For better comparison, the number of pulses A_p used in the experiment were the same ones used in the simulation. The voltage waveform and its frequency spectrum are shown in Figures 3.17, 3.18. It can be seen from figures that the experimental results agree well with simulation.

In Figure 3.19 the current waveform is shown for each case. The inductor used is L=25 mH and the capacitor is C=2.2 µF.

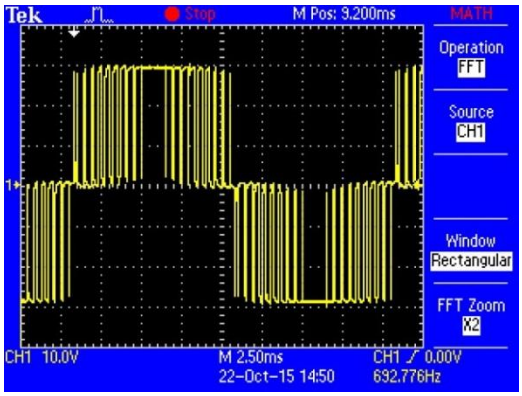


(a)



(b)

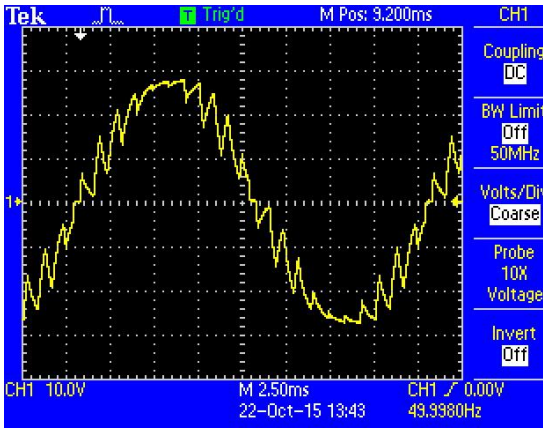
Figure 3.17 Experimental waveform with EAPWM (Ap=11). (a) Output voltage. (b) Frequency Spectrum.



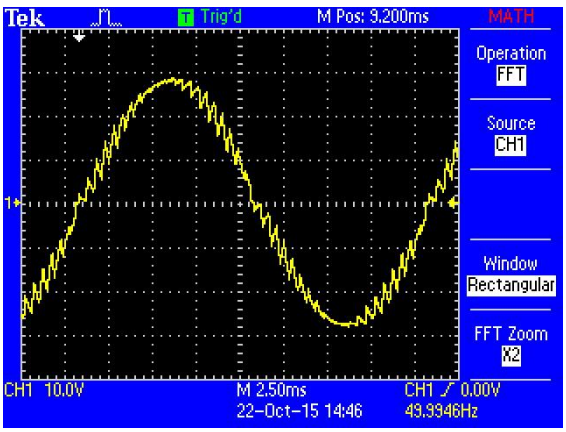
(a)

(b)

Figure 3.18 Experimental waveform with EAPWM (Ap=21). (a) Output voltage. (b) Frequency Spectrum.



(a)



(b)

Figure 3.19 Experimental current waveforms with EAPWM. (a) Ap=11. (b) Ap=21.

In Figures 3.20 and 3.21 the experimental prototype is illustrated along with the LC filter for the three-level voltage source inverter and the PCB layout.

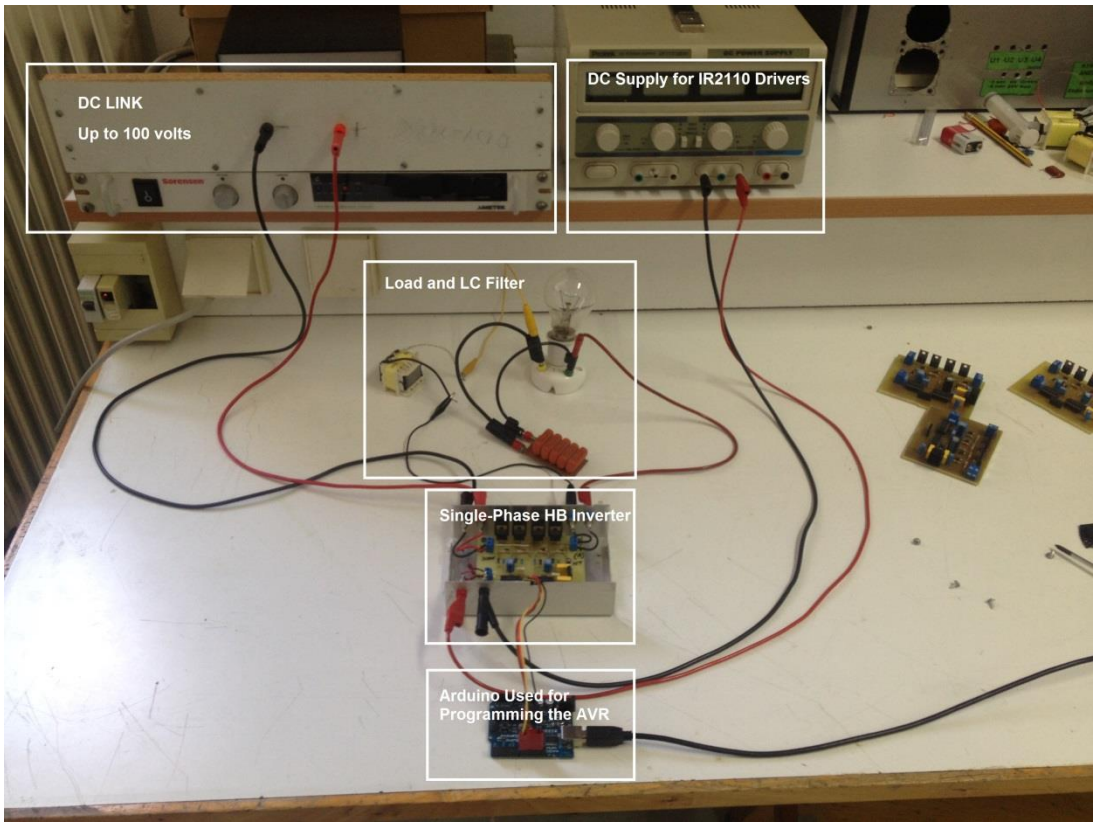


Figure 3.20 Device setup for the prototype inverter.

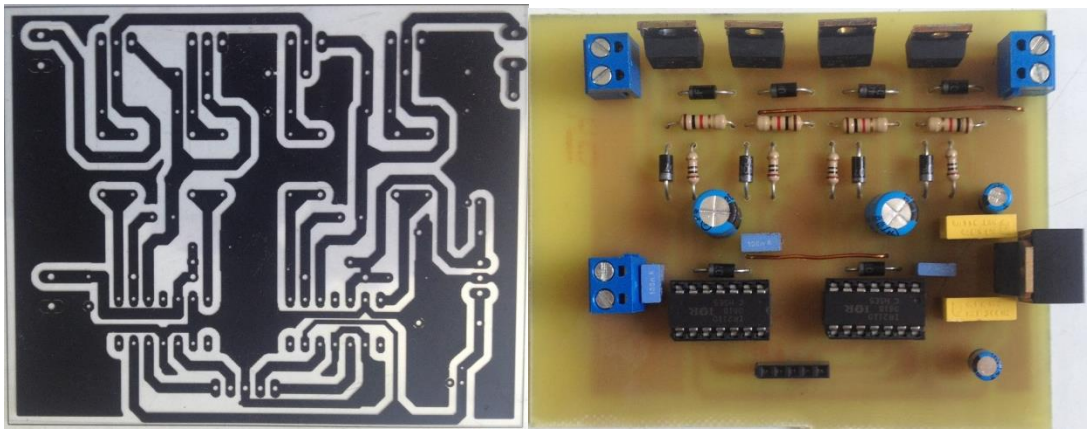


Figure 3.21 The PCB layout and the prototype inverter stage.

The inverter consists of two inverter legs and an LC filter. The inverter legs are utilized by the MOSFETS. They are supplied by a DC voltage, which is constant and is shown in Figure 3.20. The sinusoidal pulse width modulation generates unipolar voltage pulses between the terminals of the inverter legs. This means that the switched voltage is either zero or positive during the first half of the fundamental period and zero or negative during the other half of the fundamental period. The LC filter is used to observe the current waveform and to attenuate all harmonics of the switching operation sufficiently so that only the fundamental wave remains almost unaffected. In order to drive the MOSFETs, high and low side driver of the IC IR2110 is used. In Figure 3.22 the schematic for the single-phase inverter is provided.

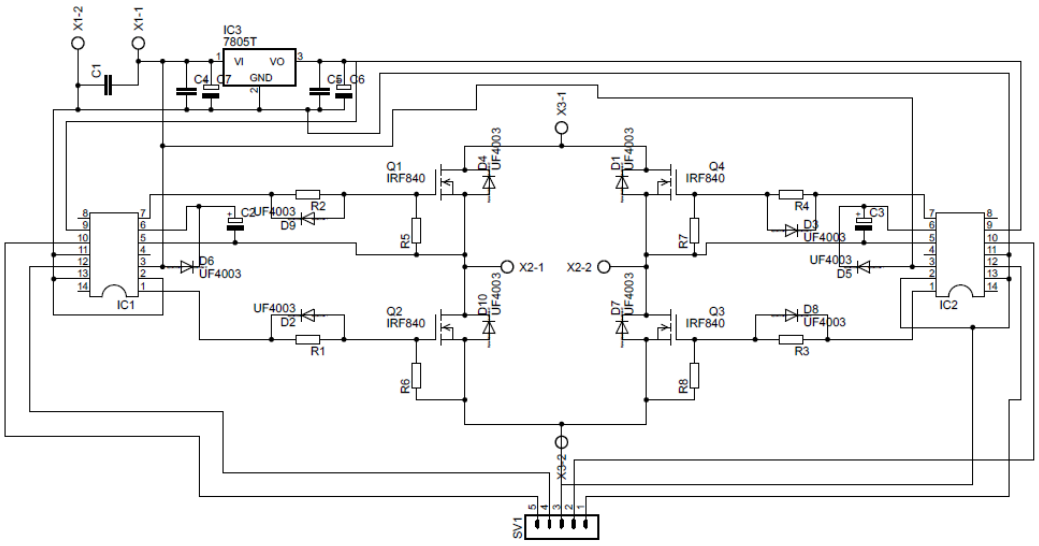


Figure 3.22 Schematic for the single-phase three-level VSI.

In Figure 3.22 SV1 is the connection point with the ATMEL ATMEGA328P microprocessor. IC1 and IC2 are the IR2110 drivers for high and low side switches of each leg. IC3 is a 5volts regulator, needed by the drivers. Further construction details for the use of IR2110 drivers can be found on application note AN-978 of IR and in AN-6076 of Fairchild.

3.4.1 Generating the unipolar PWM voltage output

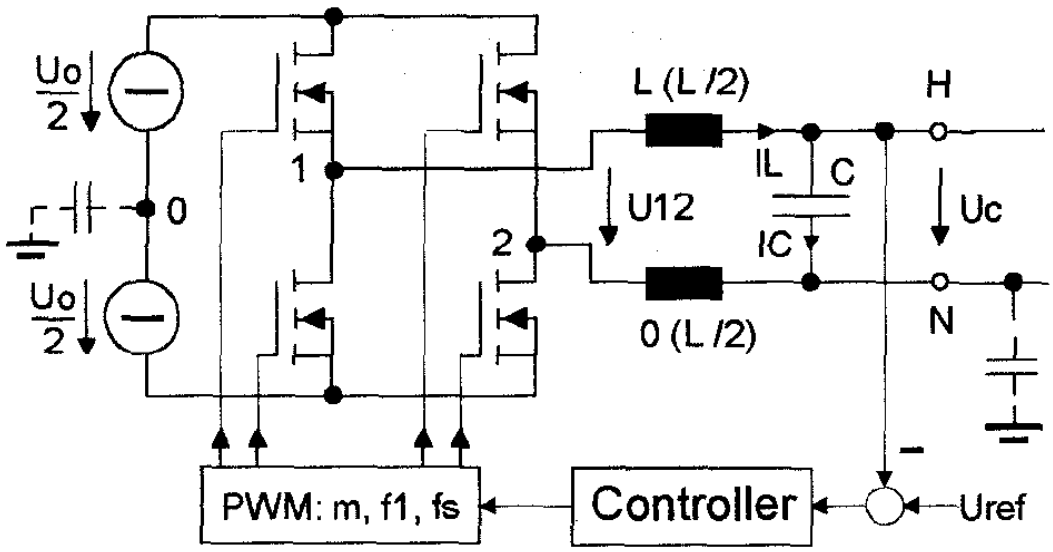


Figure 3.23 Single phase inverter with PWM voltage control.

Figure 3.23 shows the typical schematic including PWM and voltage control. Two possibilities are available in order to generate the unipolar PWM output voltage U_{12} of the full bridge. The inverter legs (s1, s2) can either be switched at half the pulse frequency (f_p) of the voltage output U_{12} *(fs1=fs2=fp/2)* or one inverter leg has to be switched at the full pulse frequency *(fs1=fp),* while the other one switches at the fundamental frequency *(fs2=f_1)* only. The first scheme is very often used because all transistors are stressed equally and the transistors duty cycles never become very small. However, this scheme causes common mode high frequency noise, which may lead to undesirable EMI problems. The noise voltage occurs between points *N* and *0* and the resulting common mode current is only limited by the parasitic capacitances between the DC input voltage (U_0) and ground and between neutral line *N* and ground. The EMI problems can be reduced by separate filter chokes, but in most cases they remain high so that further common mode filtering is needed.

By implementing the second PWM scheme, with only one filter choke between the first inverter leg and the line terminal H, the noise voltage is equal to the

voltage at the second inverter leg, which is switching at the low fundamental frequency f_1. Thus, the EMI problems do not exist. The disadvantages of this scheme are that transistors of the first leg are stressed differently and also that a small distortion can be seen at the LC filtered output voltage during zero voltage crossing. The first disadvantage can be dealt by using fast transistors for the first leg and slow transistors with lower saturation voltage for the second leg of the inverter. The second disadvantage is caused by the fact that the duty cycle decreases to zero during zero voltage crossing, which is always affected by certain delay times. However, these distortions can be kept very small. Figure 3.24 illustrates the two PWM schemes.

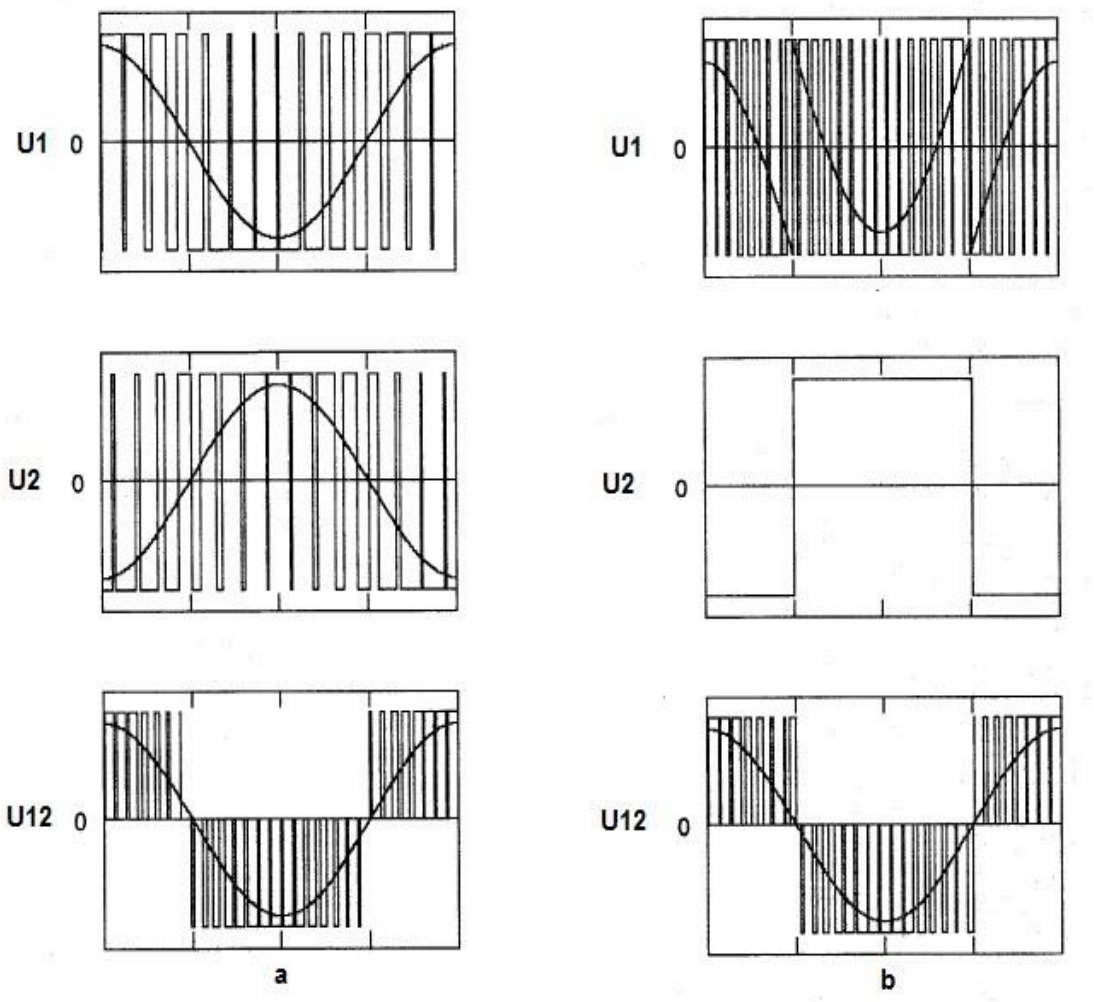


Figure 3.24 PWM schemes (a) and (b).

In this prototype inverter, the second scheme is used since EMI becomes more and more important in the industry.

3.5 Summary

The current study describes a contribution to the theory and first results for referential designed PWM waveforms. The described method based on well-defined equations, lets you set the desired amplitude modulation ratio between $0.1<m_a<1$ or evaluate the marginal modulation index being always close to 1. This algorithm has been modified to calculate the marginal m_a for a given switching frequency of the phase-leg (the number of pulses you set in the beginning). With this modification the m_a will be always be close to one in order to meet the equal area criteria. The significant advantage of the EAPWM is the well-defined mathematical formulation of the PWM that provides an ease of implementation in online digital power systems, without the need of large computational effort. Moreover, in the current thesis it is demonstrated that the results provided from the simulation are in agreement with the experimental results produced using the laboratory prototype, thus, verifying the expected inverter operation under the equal areas PWM method.

In the next chapter of this thesis, it will be illustrated the development of new algorithms for the optimization of the PWM process regarding the modulation index and the penetration in the overmodulation region introducing values of $m_a>1$. After obtaining the results of the new algorithms the next goal of this thesis is to illustrate the implementation of the Equal Areas theory in the field of Multi-Level inverters where the direct EAPWM method is applied for reference results.

CHAPTER 4

Three Modified Algorithms Based on the Equal-Areas PWM (direct PWM) for the Determination of the Switching Angles in a Single-Phase VS Inverter.

Introduction

In this chapter three different algorithms are being presented in order to determine the switching angles of a single phase voltage source inverter. EA-PWM uses only odd number of pulses per half-period in contrast to the direct PWM that uses even. All algorithms determine the pulse widths using the equal-area theorem (direct PWM). The first algorithm is simply the implementation of the basic theory of equal areas technique to determine the pulse durations. All other three (A, B, C) algorithms are modifications of the basic algorithm. We can notice differences between THD_{rms} and THD_n on each algorithm since they differ on one hand obviously because of the way they are calculated and on the other on the amplitude of the amplitude of the fundamental that each algorithm is able to create. The THDn is calculated up to the $n=200^{th}$ harmonic for all cases. Simulation figures will be presented to demonstrate the voltage output as well as the harmonic spectrum of the voltage output for each algorithm. For the comparison of each algorithm THDn as well as the normalized voltage amplitude of the fundamental harmonic, performance indicators are the chosen.

4.1 Review of the Basic Theory

The equal-areas PWM can be described as: switching so that the integrated area of the target reference waveform over the carrier interval is the same as the integrated area of the converter switched output (Figures 4.1 and 4.2).

Duration and firing time:

$$t_{pJ} = \frac{DF}{\omega}\left\{\cos\left[(J-1)\omega d\right] - \cos(J\omega d)\right\}$$

$$t_{\varepsilon J} = \left(J-1\right)d + \frac{1}{2}\left(d - t_{pJ}\right)$$

The firing and closing time t_k of the J pulse in respect to duration t_{pJ} and $t_{\varepsilon J}$

$$J = \frac{1+2k+(-1)^{k+1}}{4},$$

$$t_k = t_{\varepsilon J} + [\frac{1+(-1)^k}{2}]t_{pJ}$$

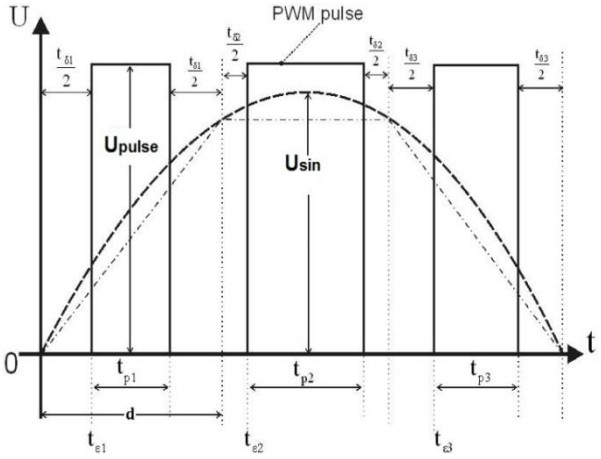


Figure 4.1 Generation of the EAPWM

The Fourier expansion of the unipolar waveform with n odd integer, it holds:

$$u(t) = \sum_{n=1,3,5,..}^{\infty} b_n \sin(n\omega t)$$

$$b_n = -\frac{4U_{p\max}}{n\pi}\sum_{k=1}^{k=A_p}(-1)^k \cos(n\omega t_k)$$

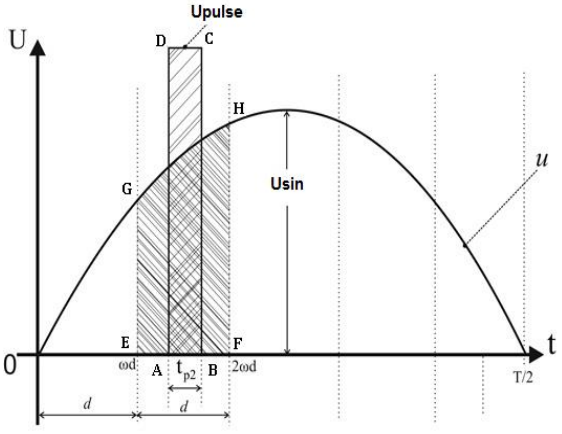


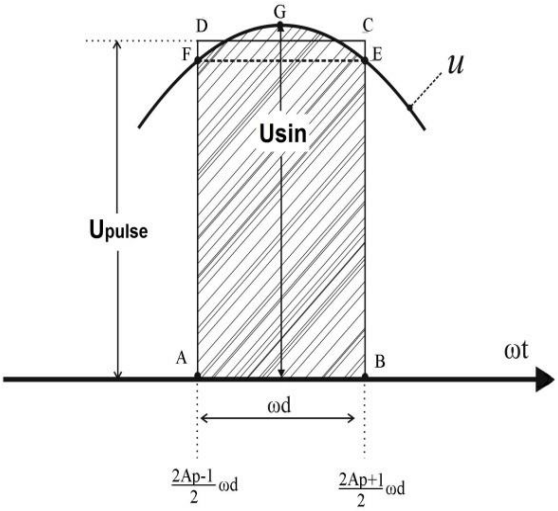
Figure 4.2 Equal area criteria.

4.2 Modified Algorithms – Simulation Results

4.2.1 Algorithm A

First algorithm A: Basic theory's algorithm lets one set the desired DF between 0.1<DF<1. One cannot set DF higher than one because overlaps between the pulses will occur (first overlap is going to take place on the centred-middle pulse). This algorithm can be modified to calculate the optimum-marginal DF for a given switching frequency of the phase-leg (the number of pulses one set in the beginning). With this modification the DF will always be close to one in order to meet the equal area criteria of the middle pulse. This modification is derived from Figure 4.3. The decrease of U_{pulse} value implies a corresponding increase of the duration of the pulse. The requirement here is to decrease the U_{pulse} in such a level that the corresponding duration of the pulse, t_p, will be less or equal to space ωd. Thus, as shown in Figure 4.3, the U_{pulse} will occur between U_{sin} and $\overline{FE}$. The minimum U_{pulse} can be calculated using the equality that, the area ABCD must be equal with the hatched area ABEGF. This equation can be expressed as:

$$\omega d \cdot U_{pulse} = \int_{\frac{A_p-1}{2}\omega d}^{\frac{A_p+1}{2}\omega d} U_{\sin}\sin(\omega t)d\omega t \quad (4.1)$$



So, the marginal U_{pulse} comes from:

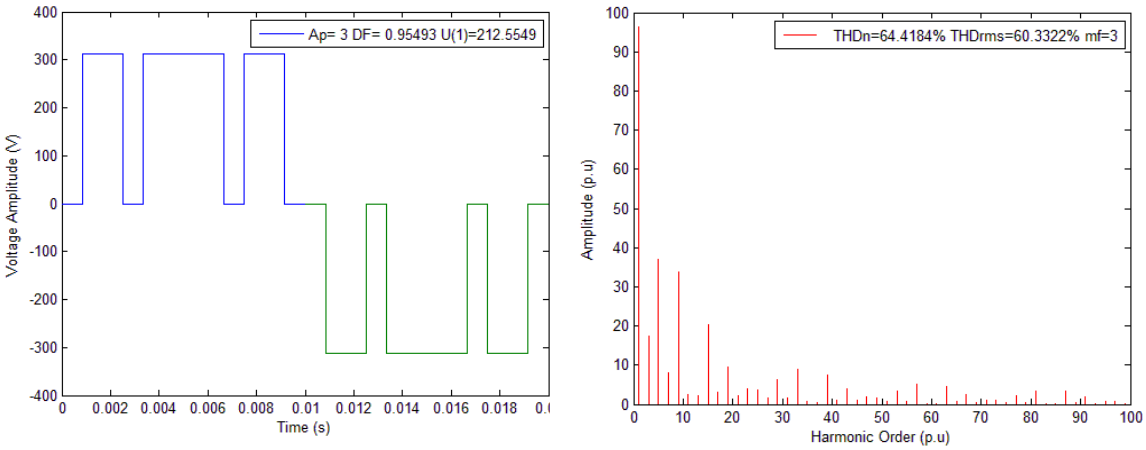
$$U_{pulse} = U_{\sin}\frac{2A_p}{\pi}\sin\left(\frac{\pi}{2A_p}\right) \quad (4.2)$$

Figure 4.3 Calculation of the marginal m_a

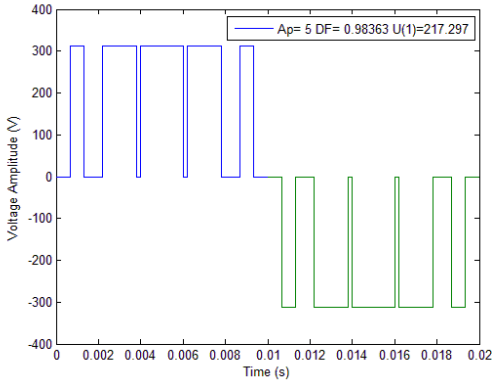
Examples of Algorithm A

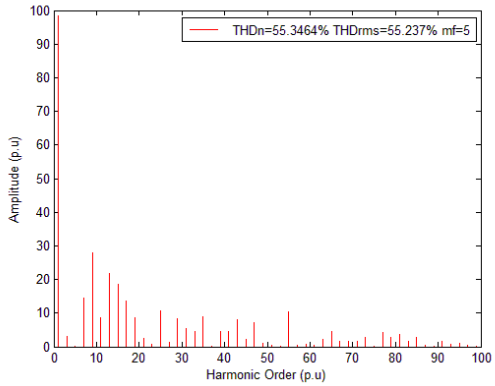
The examples shown below are using the modification mentioned above, so that the DF is always the marginal - close to one for each switching frequency (or A_p). It has to be mentioned that on the conventional unipolar SPWM each phase leg is switching at a frequency derived from the carrier signal. In this case since there is not a carrier signal the switching frequency and thus the frequency modulation ratio m_f is set through the number of pulses on a half-period, Ap. Each phase leg will then be switched at half the overall switching frequency f_s since the PWM pulses will be produced only for the half-period of the fundamental signal. Since the number of Ap pulses will always be an odd integer the frequency modulation ratio m_f will be an odd integer as well (i.e. if A_p=11, f_s=1.1kHz but for each phase-leg f_p=550 Hz so m_f= f_p/f_0=11).

A_p=3, fs=300 Hz, mf=3, DF=0.955

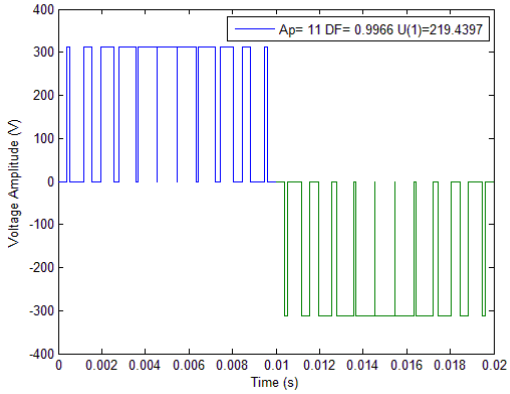


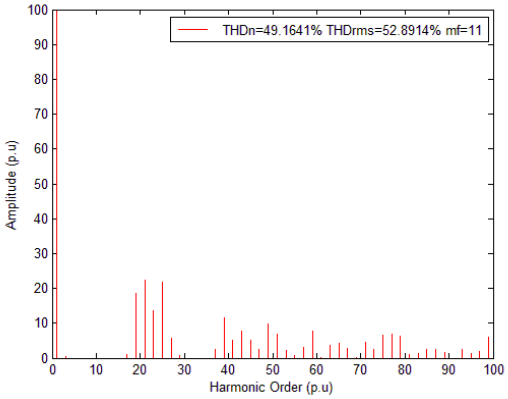
A_p=5, fs=500 Hz, mf=5, DF=0.983



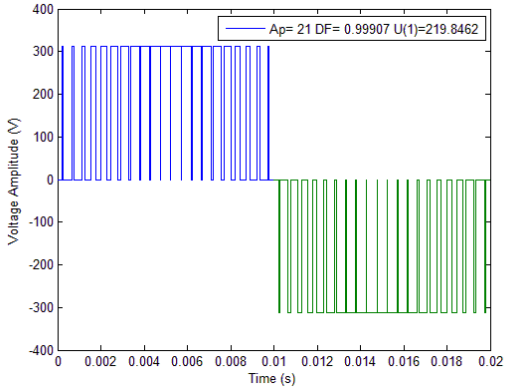


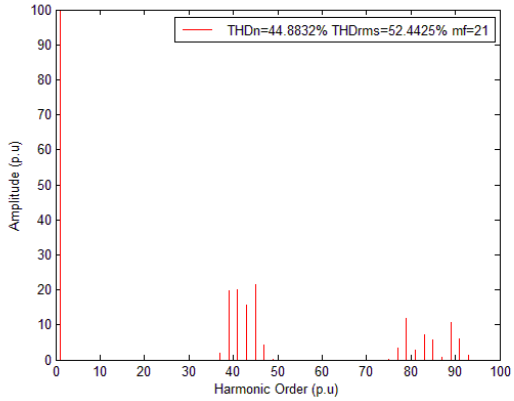
A_p=11, fs=1.1kHz, mf=11, DF=0.996





A_p=21, fs=2.1kHz, mf=21, DF=0.999





4.2.2 Algorithm B

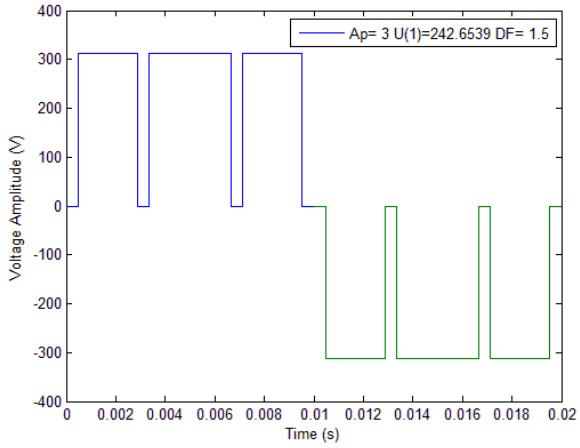
Algorithm B lets one set the desired DF between 0.1 to any value of DF higher than one until all pulses duration become equal to the time interval that has been set by the given switching frequency (the number of A_p). It is noteworthy that if for example A_p=5 then five intervals will be created in a half-period of the fundamental frequency meaning that if f_0=50 Hz, Period: T=20 ms, then the time interval will be 10ms/5=2 ms. The algorithm works as follows: if DF is set at DF=1.5, the program will start to calculate the time durations of first pulses using the DF=1.5. As it calculates the durations of pulses it also calculates the starts and endings of each pulse. After each calculation, the algorithm makes a check if the calculated duration time, overlapped the time interval. This check prevents overlaps between pulses. Now, if this is the case then it recalculates the duration time but now using the corresponding optimum-marginal DF (which is always close to one). That means that the early pulses are calculated with the initial DF=1.5 and the latter pulses that have exceeded the time interval are calculated with the optimum-marginal DF.

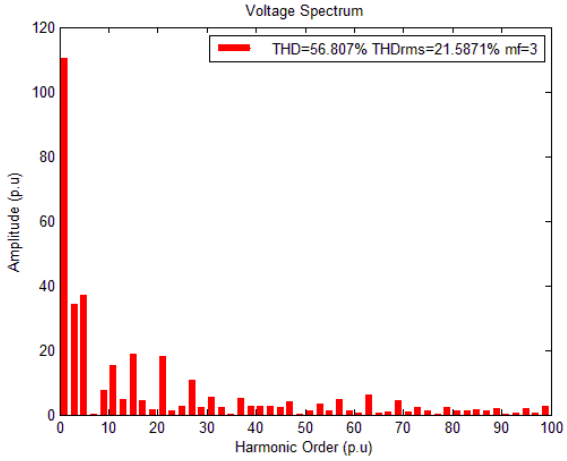
This algorithm gives the advantage of entering the overmodulation region that was previously impossible. This is demonstrated on the harmonic content of examples following, where the fundamental harmonic is increased significantly and low order harmonics are present for high switching frequencies. It is also noteworthy, that when this change on DF is made, the inverter enters a new linear region before the overmodulation region meaning that the amplitude of the fundamental component of the voltage output is still related with the input in a linear manner. In addition to what has been mentioned above, all times are calculated until $\pi/2$.

Examples of Algorithm B

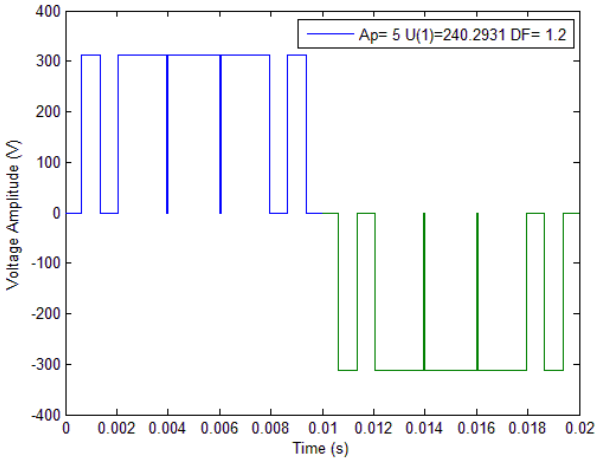
The examples shown below are demonstrating intermediate values of DF and not the marginal. That means that correction (recalculation) of some pulses have been done but not in all of them. Term k measures the pulse corrections that have been recalculated. If k=1 means that only the middle pulse has been recalculated with DF-marginal, or if k=3 means the middle and the two adjacent pulses have been recalculated and so on.

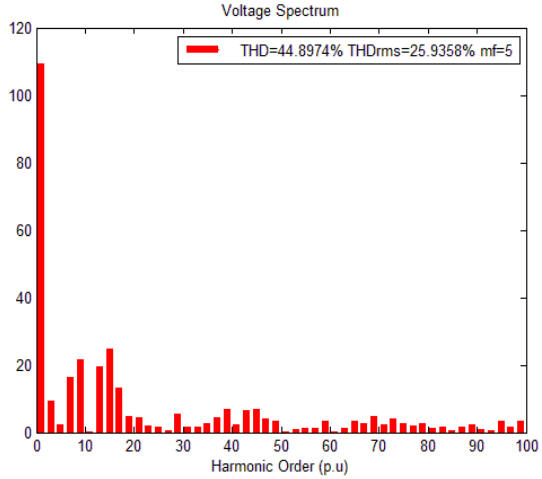
A_p=3, fs=300 Hz, mf=3, initial DF=1.5, k=1



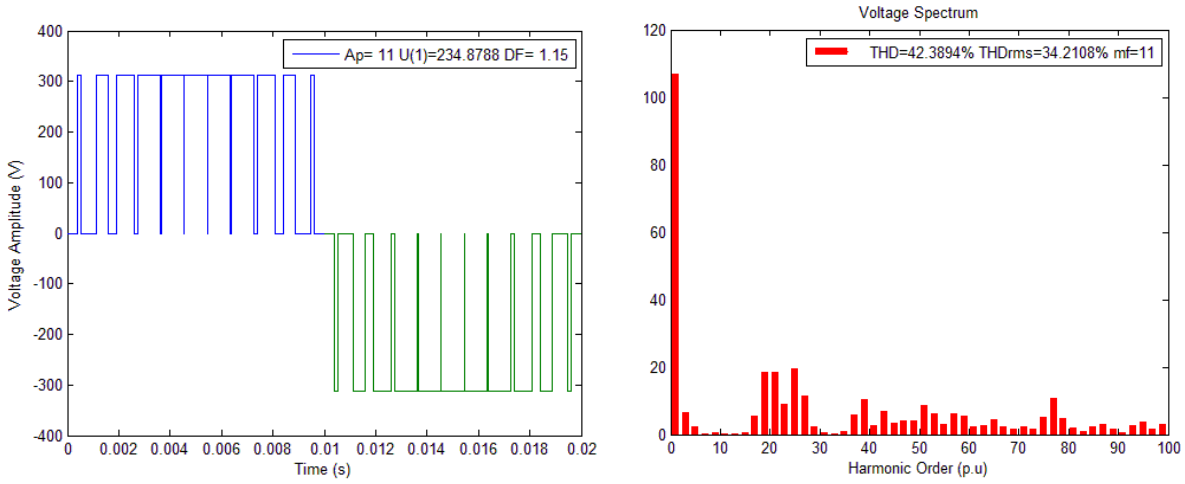


A_p=5, fs=500 Hz, mf=5, initial DF=1.2, k=1

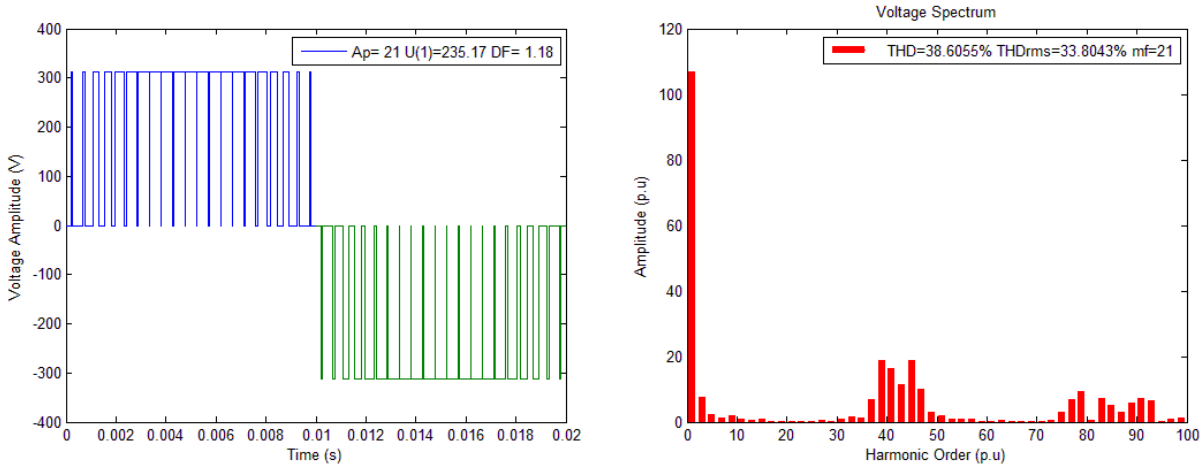




A_p=11, fs=1.1 kHz, mf=11, initial DF=1.2, k=3



A_p=21, fs=2.1 kHz, mf=21, initial DF=1.18, k=7



In all graphs of voltage spectra the harmonic analysis for all algorithms has been done calculating first the THD*n* which is the total harmonic distortion until the 200th harmonic while THD*rms* is the total harmonic distortion calculated using the *rms* values of the voltage output. The two equations used are shown below.

$$THDn = \sqrt{\sum_{n=3,5,7,..}^{\infty} \left(\frac{U_n}{U_1}\right)^2} \qquad (4.3)$$

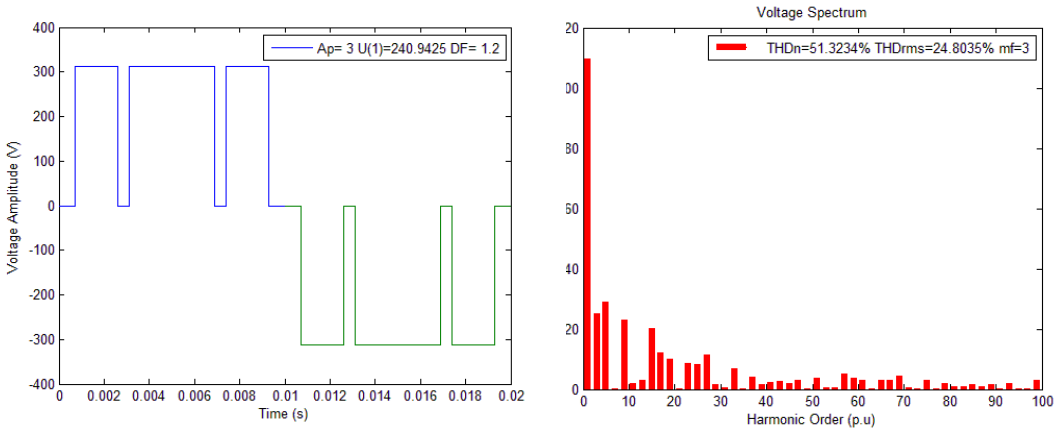
$$THDrms = 100\sqrt{\left(\frac{U_{rms}}{U_{1,rms}}\right)^2 - 1} \qquad (4.4)$$

4.2.3 Algorithm C

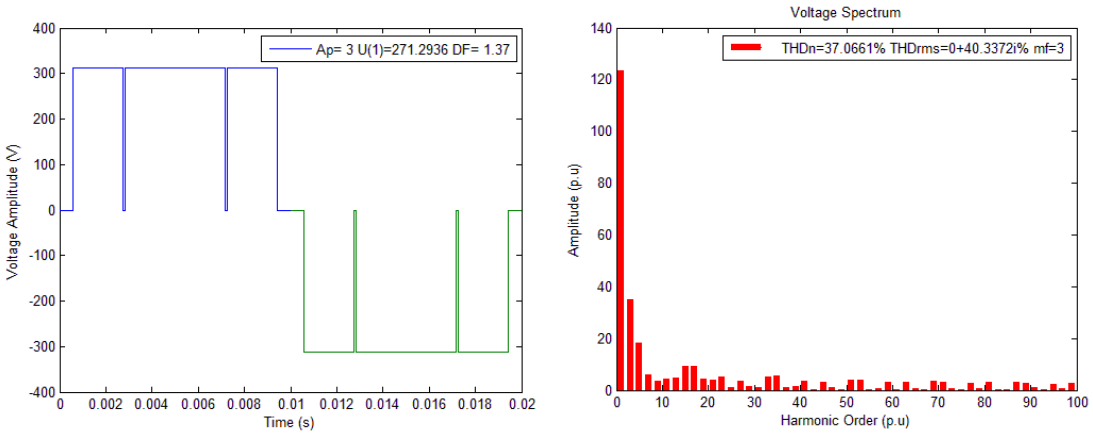
The third algorithm C lets one set the DF up to a certain point where there are no overlaps. It works as follows: after each calculation the algorithm makes a check of the firing (start) time of the next pulse if it is smaller than the ending time of the previous pulse. If this is the case then the upper limit of DF is reached and no further modification can be done. This algorithm brings better results in lower switching frequencies. This is justified since lower frequencies correspond to small amount of pulses meaning there is more space between each consecutive pulse for them to move. This algorithm converges to the first algorithm after a switching frequency of a few kHz (i.e. A_p=21…)

Examples of Algorithm C

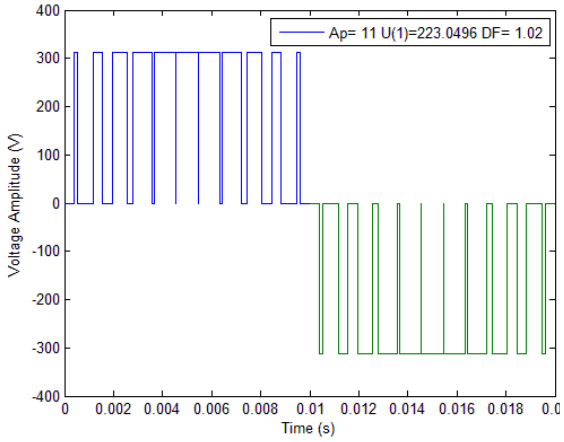
A_p=3, fs=300 Hz, mf=3, DF=1.2

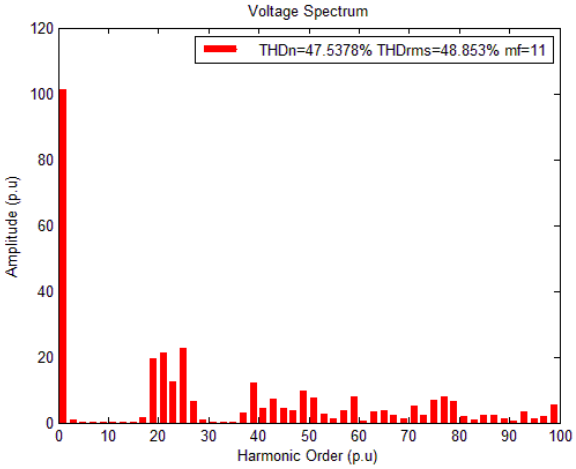


A_p=3, fs=300 Hz, mf=3, DF=1.37

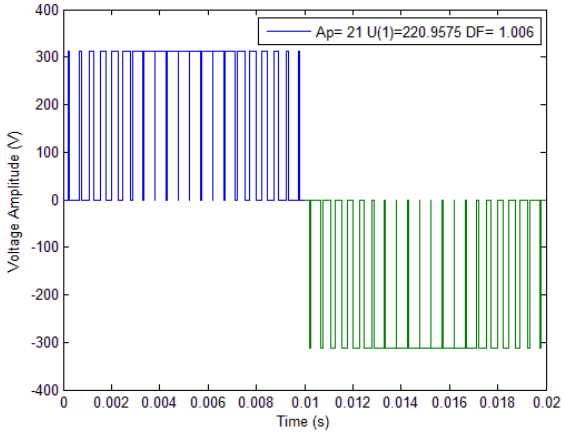


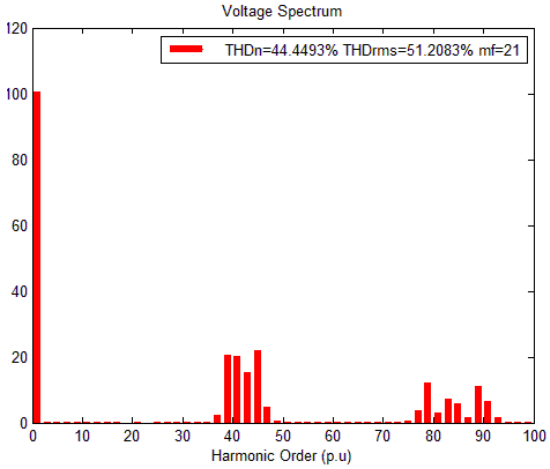
A_p=11, fs=1.1 kHz, mf=11, DF=1.02





A_p=21, fs=2.1 kHz, mf=21, DF=1.006





4.3 Experimental results for algorithms A, B, C

Using the prototype inverter constructed for this research, all different algorithms A, B, and C where implemented through the Arduino AVR ATmega 328p in order to extract experimental results. The algorithms where tested using only an ohmic load of 50 Ohms, and then retested using a filter of L=25 mH, C=10 uF and R=50 Ohms. In Figures below the PWM signals are illustrated along with the current waveform for the specific load. In Figure 4.4 the setup is illustrated. The program used for programming the AVR through the Arduino is Code Vision AVR. All codes can be found in the appendix section of this thesis [B2]. The DC link was at 60 volts.

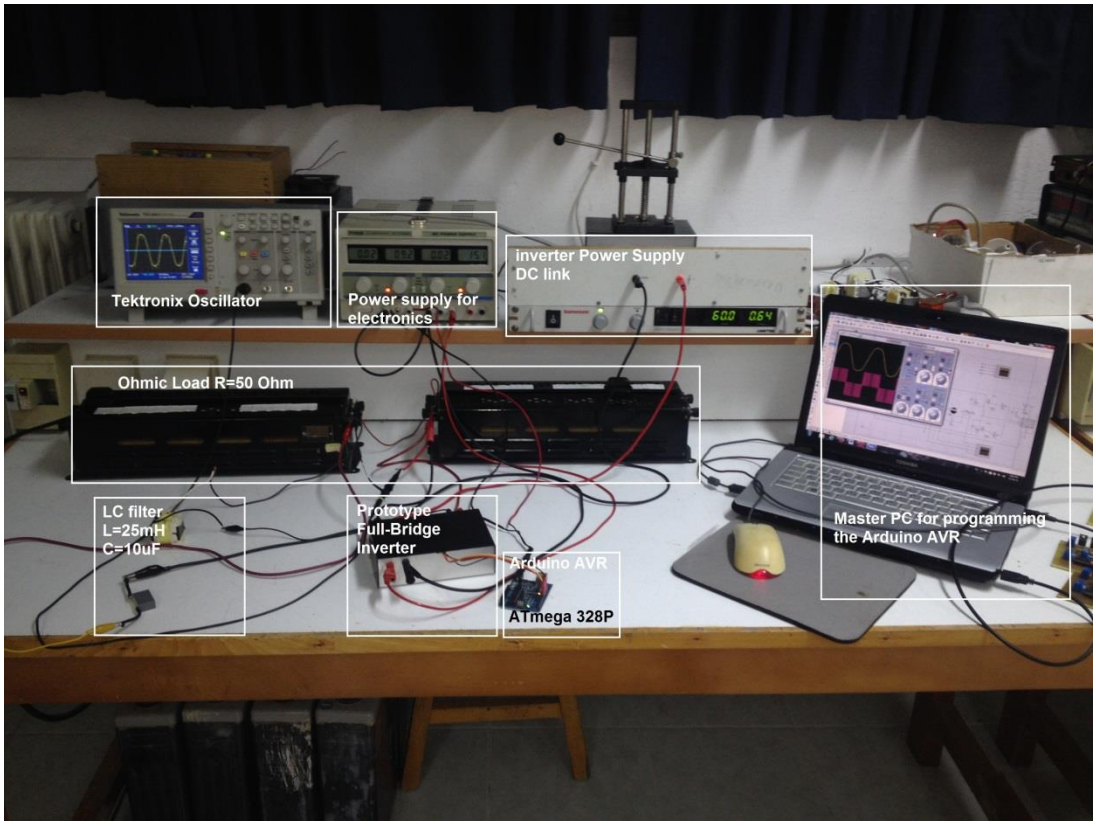


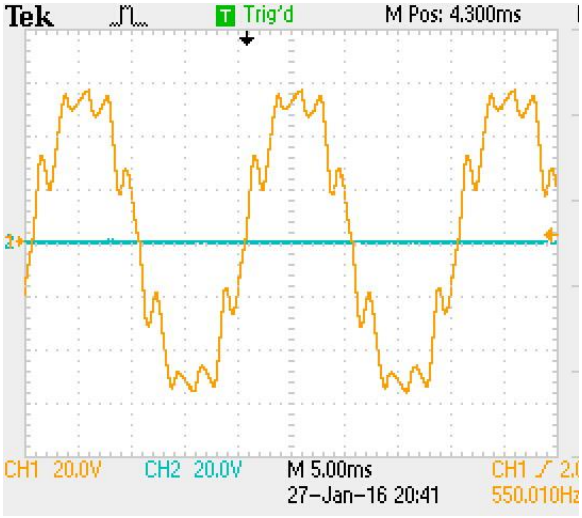
Figure 4.4 Devices setup for the implementation of different algorithms.

The experimental results illustrated are based on the switching frequency in terms of number of pulses A_p for three cases A_p=*5, 11, 21*. For better understanding of the results, the positive/half-period PWM signal from the AVR

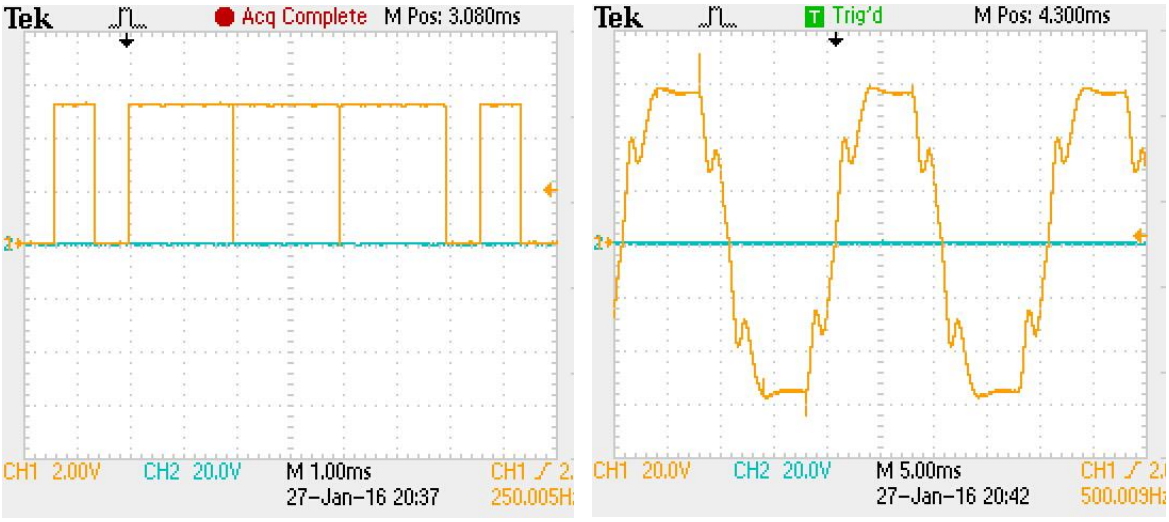
is illustrated on the left hand side followed by two periods of the current waveform when an LC filter is connected at the output of the inverter, and then the FFT for the output without any filter is illustrated. The actual PWM output for a full cycle has been previously illustrated on the theoretical and experimental results.

$A_p=5$

Algorithm A - A_p=5, fs=500 Hz, mf=5, DF=0.983

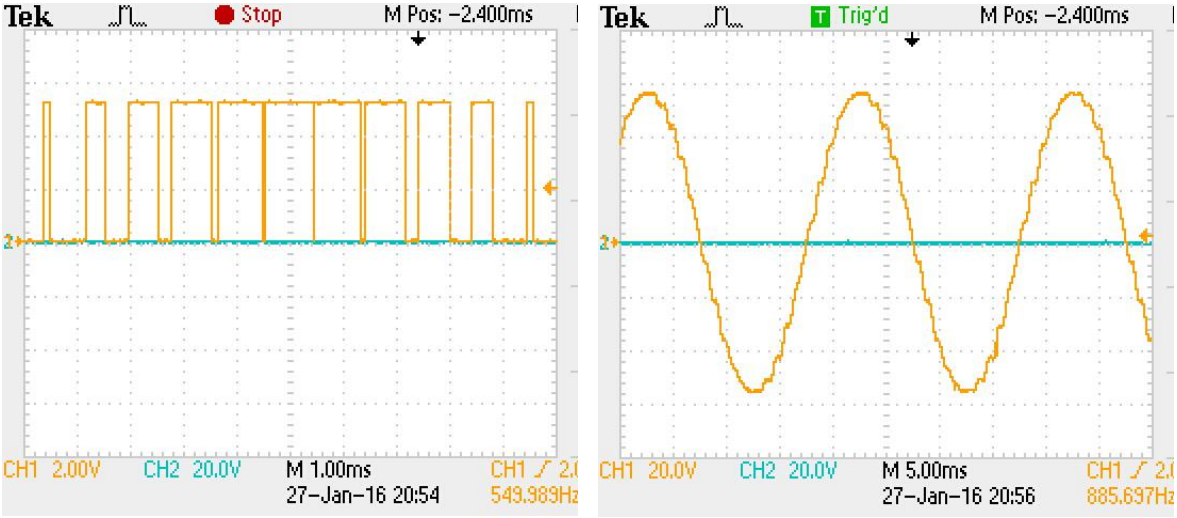


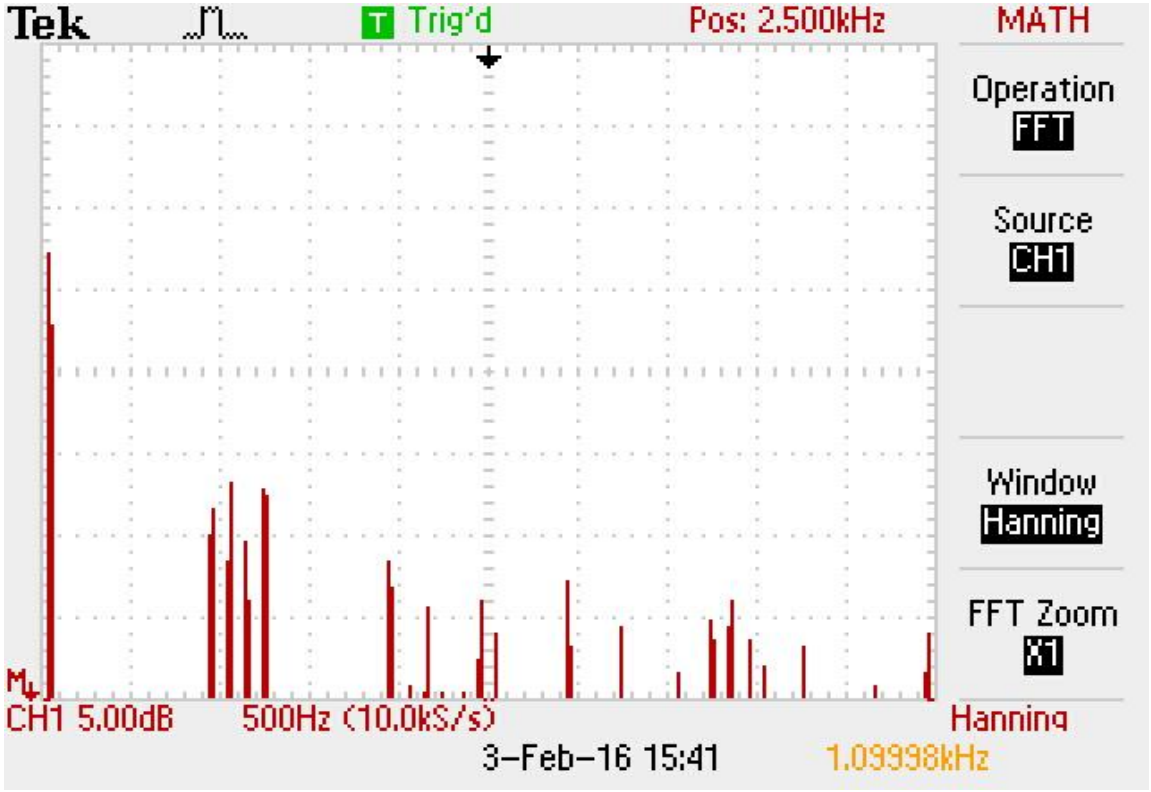
Algorithm B - A_p=5, fs=500 Hz, mf=5, initial DF=1.25, k=3



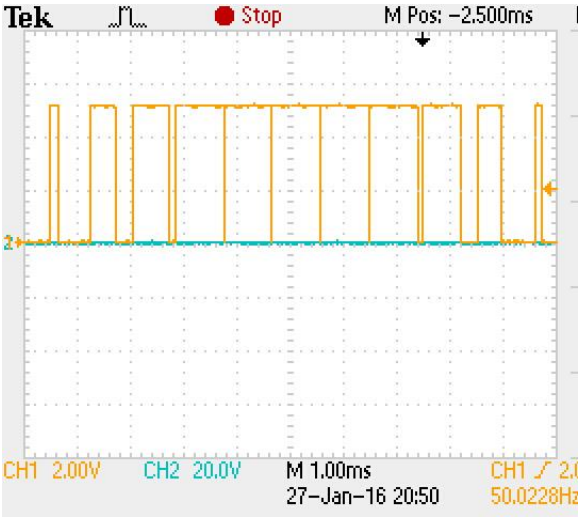
$A_p=11$

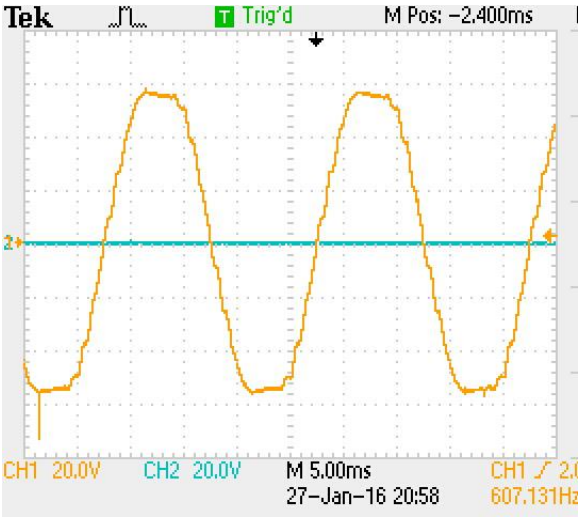
Algorithm A - A_p=11, fs=1.1 kHz, mf=11, DF=0.996





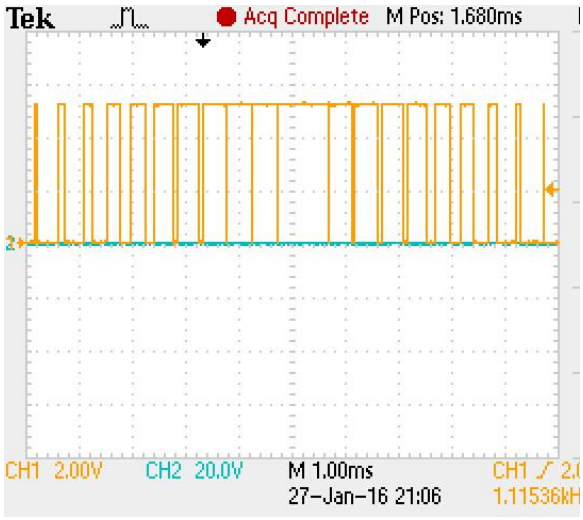
Algorithm B - A_p=11, fs=1.1 kHz, mf=11, initial DF=1.19, k=5

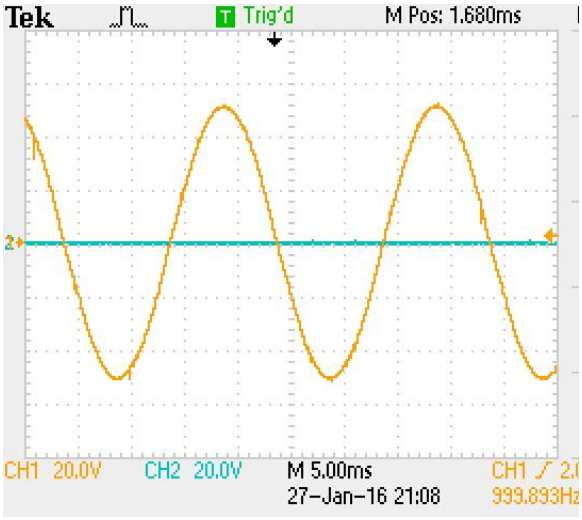




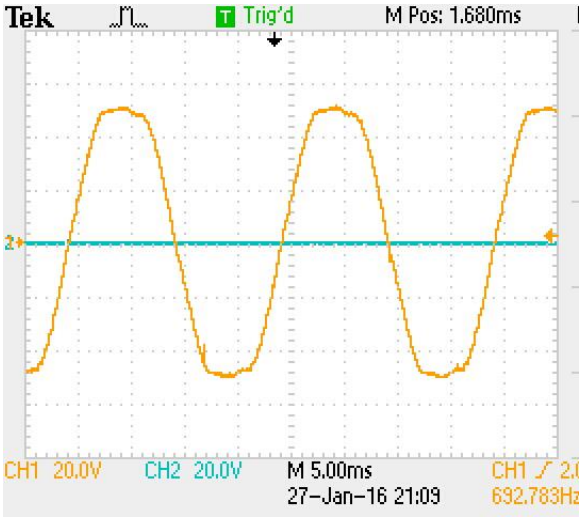
Ap=21

Algorithm A - A_p=21, fs=2.1 kHz, mf=21, DF=0.999





Algorithm B - Ap=21, fs=2.1 kHz, mf=21, initial DF=1.21, k=7



4.4 Comparison of modified algorithms in terms of THDn

In order to compare the algorithms in terms of their corresponding THD, a graph demonstrating the THDn vs. the Switching frequency (in terms of A_p) has been created for every algorithm. The THDn has been calculated until the n=199th harmonic and the switching frequencies until 10 kHz. Algorithm B presents greater interest since this scheme can be implemented to a wider range of the amplitude modulation ratio DF (or m_a) including the overmodulation region and achieves the lowest THD for a wider range of switching frequencies. This characteristic can also be beneficial since it can be implemented in various applications of a single phase voltage source inverter. From PV systems and motor drives where the U_{dc} can range, to UPS where a specific voltage output has to be meet. Algorithm B is also an automated algorithm that can run independently without the need of external correction by the user. Figures 4.5 to 4.7 show the THDn vs. A_p for each algorithm, while Figure 4.8 shows the comparison between them. The graphs also show that THDn can be very low at high values of A_p but this can be misleading, since in order to accurately determine the THD, numerically speaking it is usually necessary to include all significant sideband harmonics up to the fifth harmonic of the carrier, depending upon the PWM switching frequency.

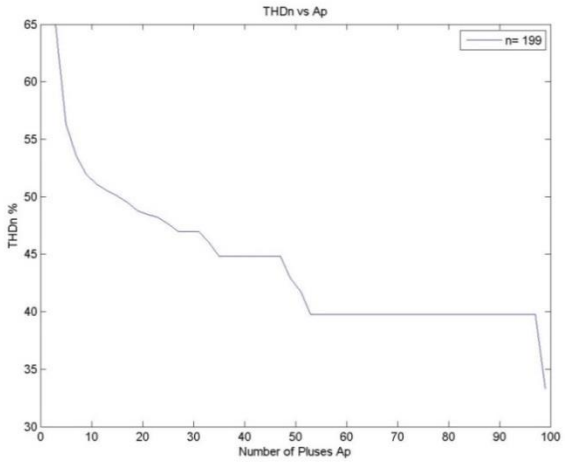


Figure 4.5 THDn vs. Ap for algorithm A

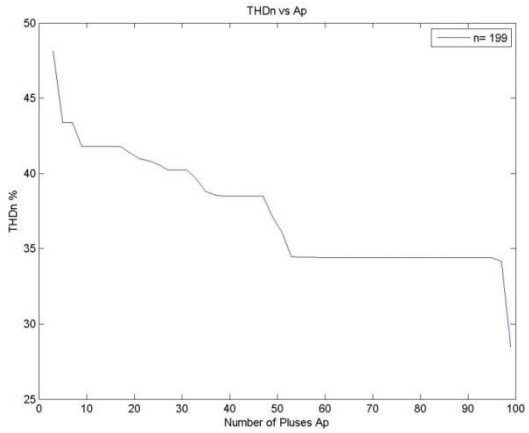


Figure 4.6 THDn vs. Ap for algorithm B

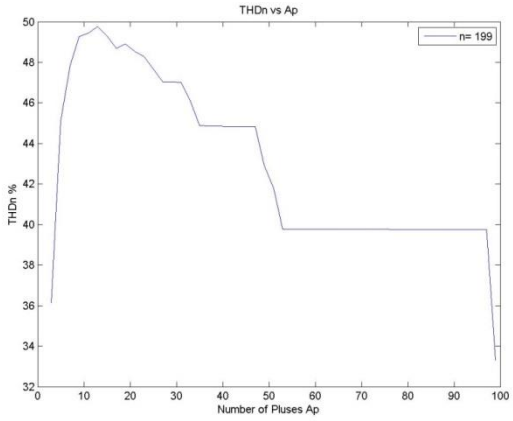


Figure 4.7 THDn vs. Ap for algorithm C

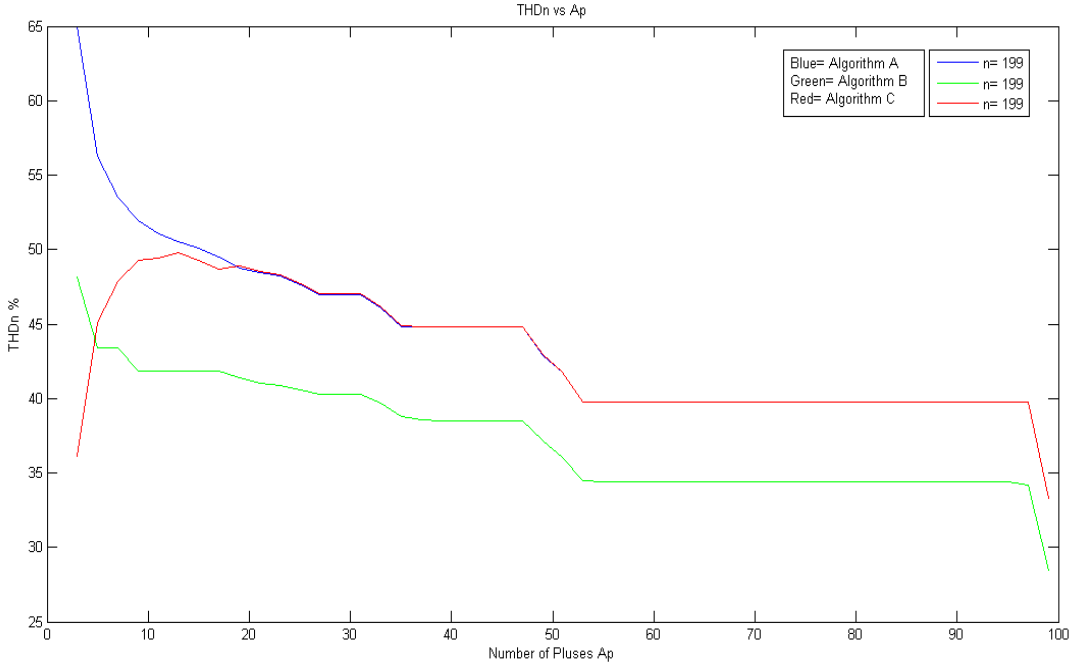


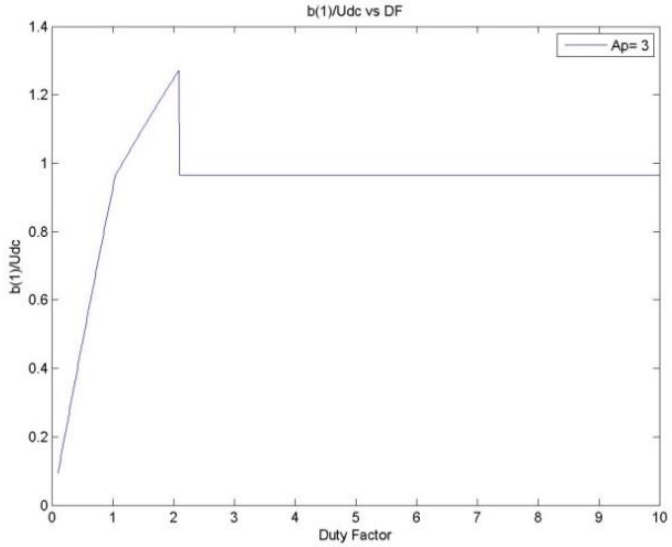
Figure 4.8 THDn vs. Ap Comparative graph for all algorithms

In Figure 4.7 it is clear that algorithm C performs better on low switching frequencies (Ap=3, 5, 7) where the space between the pulses can offer a greater degree of freedom in pulse placing. In Figure 4.8 the superior overall performance of algorithm B is illustrated, achieving the lowest THDn between all algorithms into a wider range of switching frequencies.

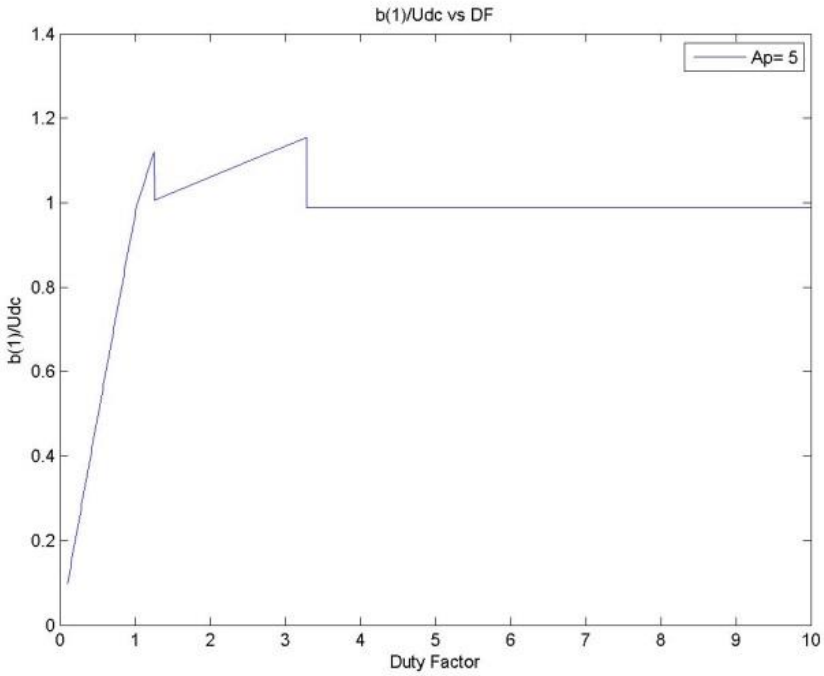
4.5 Comparison of modified algorithms in terms of the normalized amplitude of the fundamental harmonic b(1)/Udc

In all algorithms analyzed above the recalculations concern the modulation index DF which resets the width of the pulses. Algorithms were developed in order for modulation index to be set to a higher value than 1 to enter the over-modulation region. In each algorithm different criteria are imposed in order not to have overlaps between the pulses. Depending on the criteria of each algorithm, the modulation index is recalculated to a marginal value which is always the closest value to 1 according to the equation derived from the first algorithm A. Since the recalculated amplitude modulation index DF (or m_a) is closer to unity, after each recalculation the overall modulation index converges to unity as this becomes evident from the graphs.

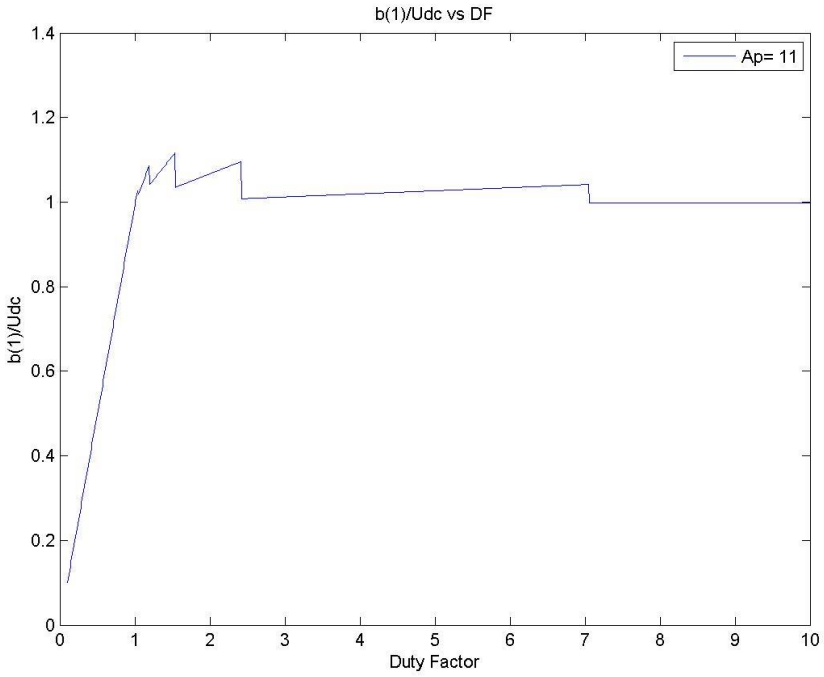
Since algorithm B is of more interest at this stage, Figure 4.9 below show the normalized amplitude of the fundamental harmonic versus the amplitude modulation factor DF for various switching frequencies (in terms of Ap). After every recalculation, by the use of curve fitting tools, the linearity before the overmodulation region was showed.



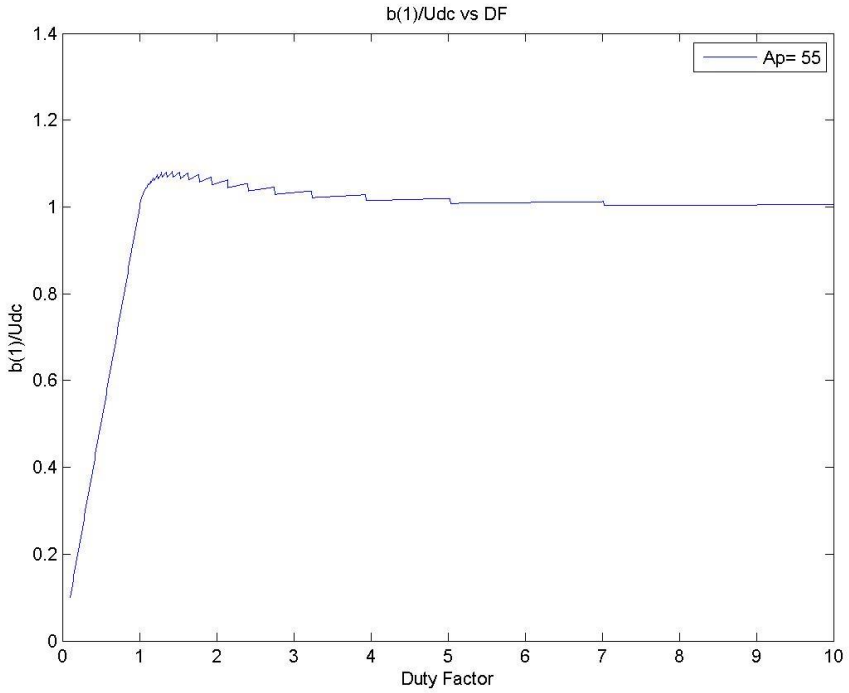
(a)


b(1)/Udc vs DF
Ap= 5
b(1)/Udc
Duty Factor
0
0.2
0.4
0.6
0.8
1
1.2
1.4
0
1
2
3
4
5
6
7
8
9
10

(b)


b(1)/Udc vs DF
Ap= 11
b(1)/Udc
Duty Factor
0
0.2
0.4
0.6
0.8
1
1.2
1.4
0
1
2
3
4
5
6
7
8
9
10

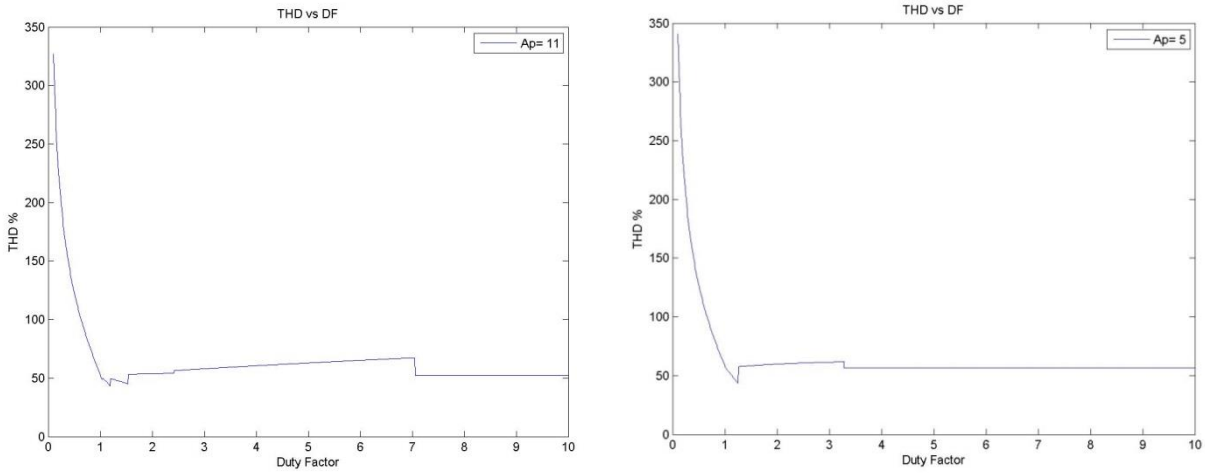
(c)



(d)

Figure 4.9 Normalized amplitude of the fundamental harmonic versus the amplitude modulation factor DF for various switching frequencies (in terms of Ap). (a) Ap=3, (b) Ap=5, (c) Ap=11, (d) Ap=55.

Figure 4.10 below show the relationship of THDn and amplitude modulation factor DF for algorithm B for various switching frequencies (in terms of Ap). THDn has been calculated until the 200th harmonic to acquire better results.



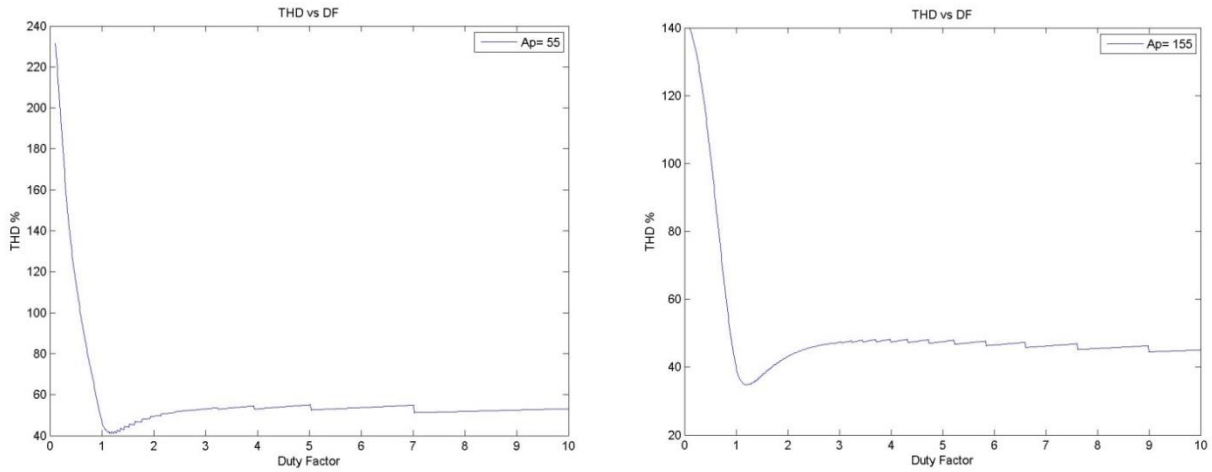


Figure 4.10 THDn and amplitude modulation factor m_a=DF for algorithm B for various switching frequencies (in terms of Ap).

Figure 4.11 shows, the variation of the fundamental harmonic component of the voltage output of the inverter versus the modulation index, using algorithm B. The case of a low switching frequency of 500 Hz (A_p=5 number of pulses) is used. The turning points of the curve are highlighted in red circles in order to demonstrate how the algorithm works. In every turning point of the curve, a recalculation is needed since new overlaps occurred. The modulating wave is changing every time an overlap occurs. The recalculated pulses are using the beneficial modulation ratio of m_a=DF=1 to avoid overlaps with the adjacent pulses. It can be observed that, after a finite number of recalculations, the curve is parallel to the horizontal axis and not to the 4/π where the rectangular waveform converges thru overmodulation. This occurs, as a result of the fundamental operation of algorithm B, as more and more pulses re-modulate their width using m_a=1. The number of available recalculations, for any number of pulses A_p can be found by: *1+(A_p-1)/2*, where first term '*1*' represents the middle pulse and the second term '*(A_p-1)/2*'the num. of pulses until π/2 excluding the middle pulse. So, for the case of A_p=5 the number of available recalculations until the gain of the fundamental component converges to unity is '3', as it is illustrated in Figure 4.11. In Figure 4.12 the re-formation of the modulating wave for a case of m_a=1.22 is shown. It is obvious that where the

overlaps occur the modulating sinus wave of m_a=1.22 has been replaced by the curve of m_a=1.

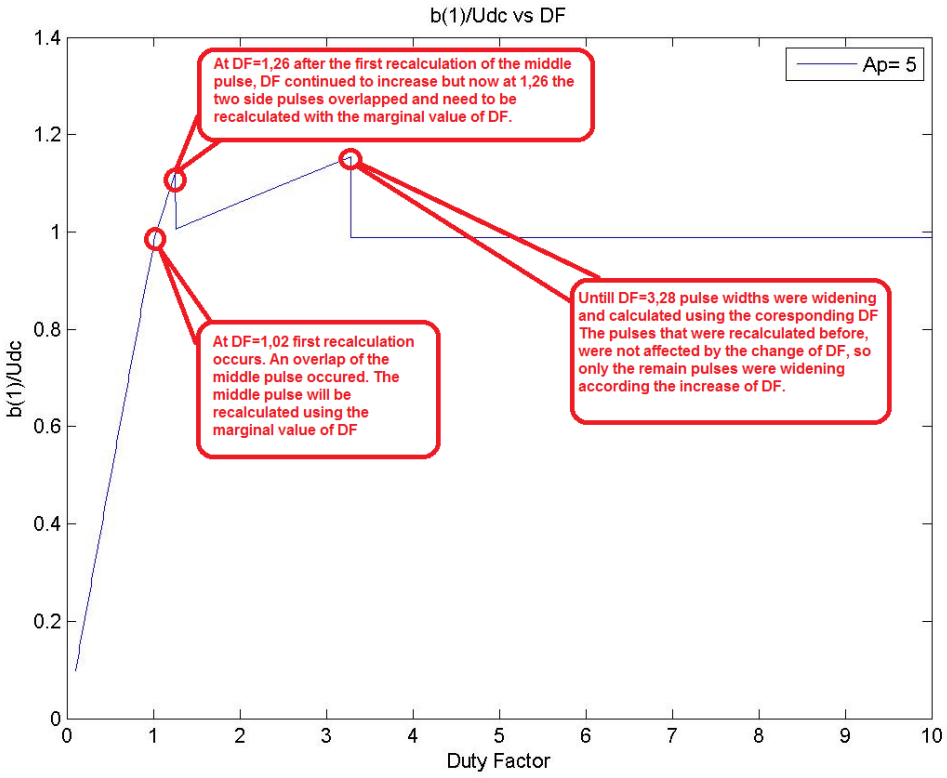


Figure 4.11 Variation of the fundamental harmonic component of the voltage output of the inverter, versus the modulation index DF, using algorithm B

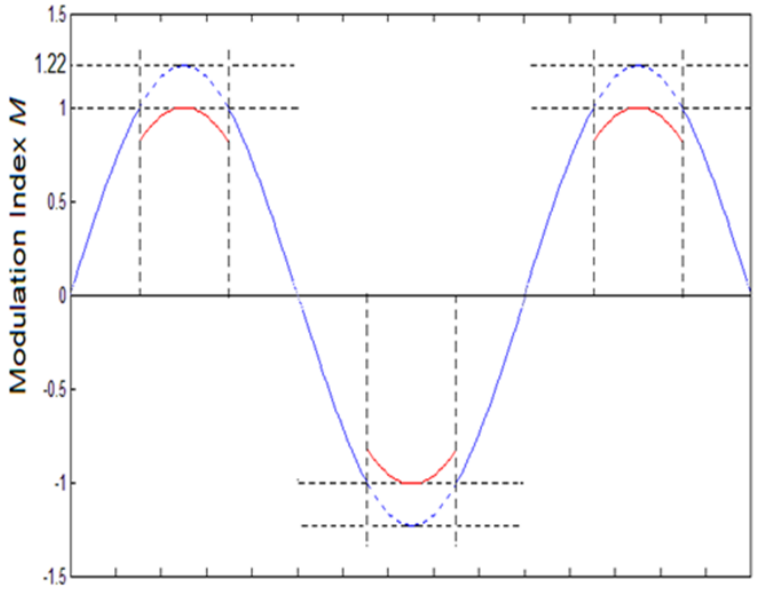


Figure 4.12 Re-formation of the modulating wave.

4.6 Summary

The implementation of the EAPWM to full-bridge single-phase voltage source inverters was a straightforward procedure. Experimental results validated the expected results from the simulation. The performance of the inverter showed almost similar harmonic performance with the regular sampled PWM, achieving a small improvement regarding the THD, at the same switching conditions. One of the main advantages of this method, against other PWM techniques, was the ease of implementation to the microprocessor for real time use. Using the equal areas criteria, a simple trigonometric equation was produced to determine the pulse widths, which then was used to generate the PWM directly with the introduction of an efficient microprocessor-based software algorithm.

The modification of the basic algorithm to enter the overmodulation region was much of an interest, thus three new algorithms were developed by this thesis. In particular, the key finding of this research algorithm B, showed a linear operation of the inverter into the overmodulation region. Furthermore, the principle of the modified algorithm B will also be implemented to modulate the multilevel inverter prototype since this algorithm can extend the linear region of the inverter.

This particular outcome constitutes a potentially significant contribution to PWM methods and certainly will be used in a multilevel inverter prototype in order to produce simulation and experimental results.

CHAPTER 5

The Equal Areas EAPWM in Multilevel Inverters

Introduction

In recent years, Multilevel Inverters have received more and more attention for medium and high voltage applications and FACTS (Flexible Alternating Current Transmission System) controllers. Their capability of high voltage operation, high efficiency and low electromagnetic interference (EMI) are the main reasons for their dominance in high power applications nowadays [3], [4]. The desired output of a multilevel converter is actually synthesized by a number of DC voltage sources. As the number of DC sources increases the converter voltage output waveform approaches the sinusoidal waveform, while keeping the switching scheme in a low fundamental frequency. That gives the advantage of low switching losses while the rate of change of voltage dV/dt in every switch is decreased due to the several DC sources. For high power applications such as utility applications and FACTS, the voltage output must meet specific requirements for THD. Many control and modulation strategies for multilevel inverters exist and can be classified according to the switching frequency, i.e. to those using a fundamental switching frequency and those using high switching frequency PWM [5], [6]. High switching frequency methods have many computation steps in one period of the output voltage while the low switching frequency methods perform one or two computations during one cycle of the

output voltage in order to produce the desired sinus waveform. The classic carrier-based sinusoidal PWM (SPWM) schemes are very popular methods using the phase shifting or level shifting technique to reduce the harmonic content [7], [8]. The multilevel Selective Harmonic Elimination and the Space Vector Control are typical examples of low switching frequency methods [9-13].

5.1 Implementation of the EAPWM in Multilevel Inverters

In an effort to simplify the computation procedure, the reformed theory of EA-PWM [1], [2] has been modified and implemented in a 9-level multilevel inverter. The results showed that this discontinuous digitally implemented PWM method can produce very low THD in low switching frequencies with less computational effort. The harmonic spectrum of the output is clear from higher order harmonics while harmonics around the switching frequency appear at a low percentage of the fundamental frequency. The simulation program for the EA-PWM method also offers the variation between different switching frequencies along with the variation of the number of the DC sources.

5.1.1. Derivation of the basic equations and calculation of times

In order to calculate what number of PWM pulses can fit in each level, the schematic in Figure 5.1 will be used, which shows a half period of a sine wave nested to a 9-level inverter with 4 equal DC sources V_{dc} creating a 9 level output. All corresponding times will be calculated until π/2, because of quarter wave symmetry.

The sinusoidal voltage in Figure1 can be expressed,

$$v = V_{\max} \cdot \sin \omega t \qquad (5.1)$$

where V_{max} is divided in four equal intervals.

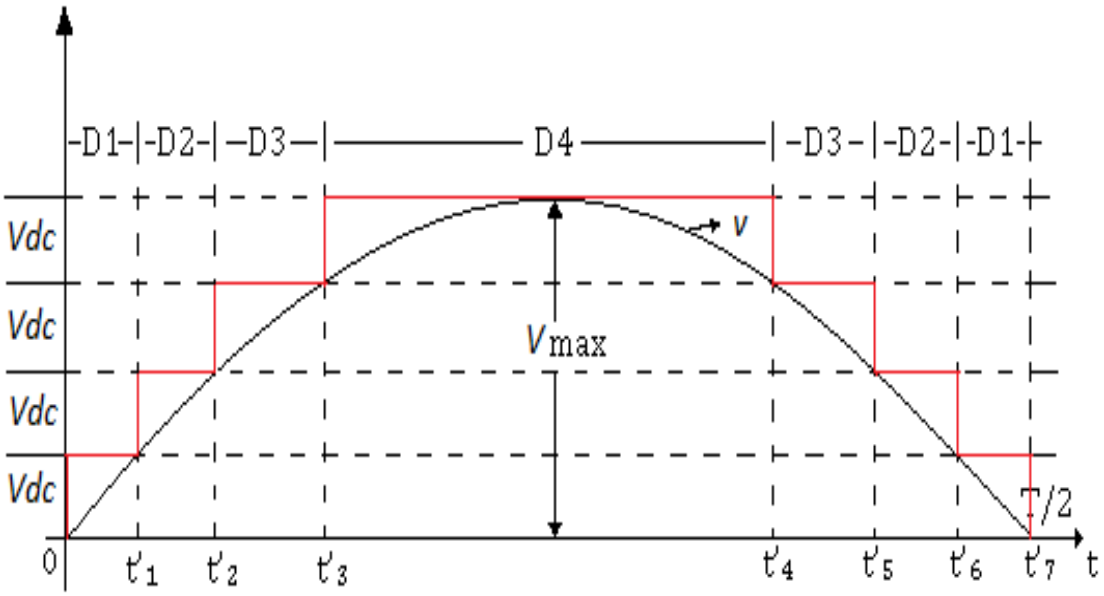


Figure 5.1 Pulse segregation of a 9-level inverter output.

So, for equal sources V_{dc} is,

$$Vdc = \frac{V_{\max}}{E} \qquad (5.2)$$

where, E is the number of sources and the m-levels of the inverter are related with sources E as, $m=2E+1$. So for $E=4$ the levels m of the inverter are 9. For a grid tie inverter where reference voltage target is V_{rms} =220 V, V_{max}=311.127 V and for $E=4$, V_{dc}=77.78 V.

Times t'_1, t'_2, t'_3... are fixed for a predefined number of sources E. They define the cross sections of the DC voltage levels V_{dc} with the reference sinusoidal voltage waveform v. Time $t'_0=0$ since it is assumed that first level starts at zero point.

So for example, t'_2 can be calculated by:

$$2Vdc = V_{\max} \cdot \sin \omega t_2^{'}$$

$$\sin \omega t_2^{'} = \frac{2Vdc}{V_{\max}}$$

By substituting V_{max} according to eq. (5.2) we get:

$$\sin \omega t_2^{'} = \frac{2 \cdot Vdc}{E \cdot Vdc} = \frac{2}{E}$$

$$t_2^{'} = \frac{\arcsin(\frac{2}{E})}{\omega}$$

In the last equation numerator *"2"* is actually a pointer indicating the V_{dc} level we stand in every step of our calculations until π/2 and from now on it will be represented with the letter *"e"*.

So, generalizing for times *t'*:

$$t_e^{'} = \frac{\arcsin(\frac{e}{E})}{\omega} \qquad (5.3)$$

where, *e*=1…..(E-1)

Time $t_E^{'}$ can be calculated from equation (5.4), where T, the period of reference waveform *v:*

$$t'_E = \frac{T}{2} - t'_{E-1} \qquad (5.4)$$

All the remaining times t'_5, t'_6, t'_7, can be calculated easily through symmetry. In this chapter we calculate the necessary times t'_1, $t'_{2...and}$ t'_E.

D_1, D_2, D_3…D_E are time intervals demonstrating the duration of each level and can be calculated by equation:

$$D_e = t'_e - t'_{e-1} \qquad (5.5)$$

Where here, *e*=1….E

The overall distribution of pulses, for each time interval *De,* depends on the number of pulses that are being set initially for the first time interval D_1. The distribution to each interval D_e will be then determined in an analogue manner. For example for the 9-level inverter if in first interval D_1, A_{p1} (number of pulses) are being applied then the number of pulses A_{p2} in the second interval D_2 will be:

$$A_{p2} = A_{p1} \cdot \frac{D_2}{D_1}$$

Similarly,

$$A_{p3} = A_{p1} \cdot \frac{D_3}{D_1}$$

$$A_{p4} = A_{p1} \cdot \frac{D_4}{D_1}$$

Generally,

$$A_{pe} = A_{p1} \cdot \frac{D_e}{D_1} \qquad (5.6)$$

where $e=1...E$. Since, the number of pulses A_{pe}, is an integer, in each interval D_e the result of eq. 6 will also result in an integer. Each interval D_e is then divided by the corresponding number of pulses A_{pe}, to create equal smaller intervals (Figure 5.2) in order to apply the EAPWM. These smaller intervals will be represented by the small letter d_e where indicator *"e"* shows the corresponding level. So, for d_e the following applies:

$$d_e = \frac{D_e}{A_{pe}} \qquad (5.7)$$

where, e=1….E.

5.1.2 Calculation of active and firing time in a D_e time interval.

With the assistance of Figure 5.2 we will calculate the firing and active times.

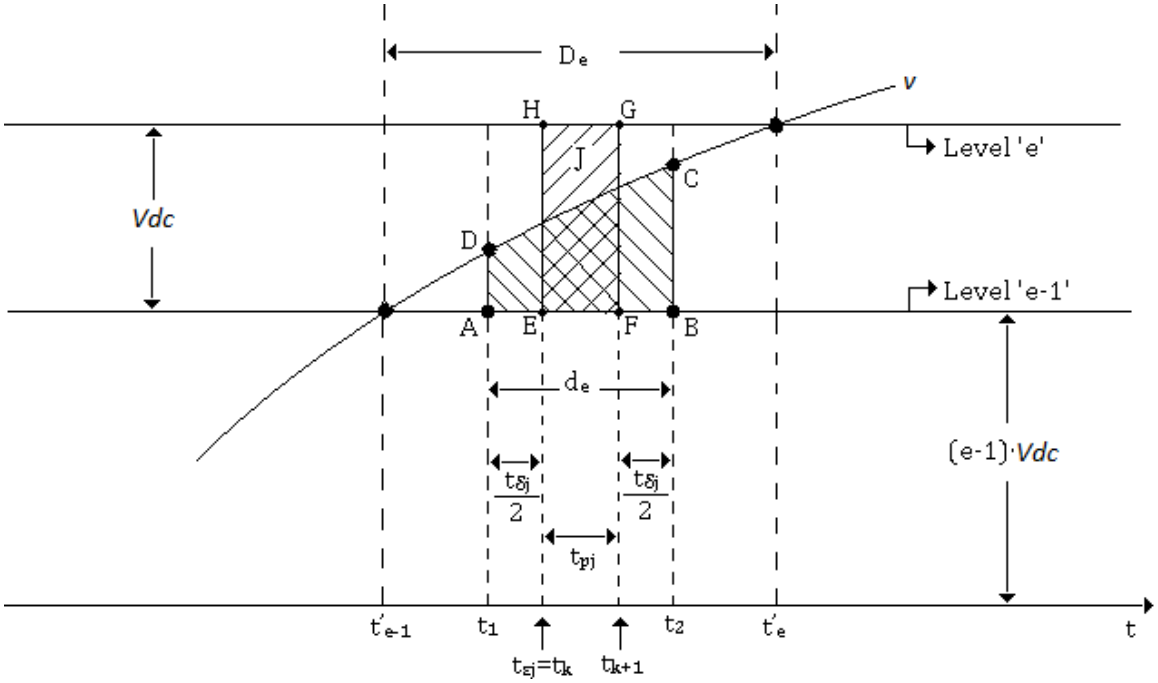


Figure 5.2 Calculation of active and firing time in a D_e interval.

In Figure 5.2 the sinusoidal reference waveform *v* intersects with levels *'e-1'* and *'e'* at times t'_{e-1} and t'_e, respectively. During a D_e time interval a pulse train is already been set with A_{pe} number of pulses. Calculations will take place for a random *J* pulse in *De* interval, where *J* shows the pulse position in the corresponding pulse train and can take values from 1 to A_{pe} ($J=1.... A_{pe}$). The position of the *J* pulse is determined by the times t_k and t_{k+1}, where *k* indicates the start and end of the pulse. *J* and *k* are related by the equation:

$$J = \frac{1+2k-(-1)^k}{4} \qquad (5.8)$$

where, $k = 1...2A_{pe}$

During D_e time interval, the duration of pulse's J is t_{pj} (active time) and the firing time is $t_{\varepsilon j}$. In either side of pulse J are the pausing times $\frac{t_{\delta j}}{2}$. For $t_{\delta j}$:

$$t_{\delta j} + t_{pj} = d_e \quad (5.9)$$

In order to calculate the firing and active times we will apply the Equal Areas theory, beginning with the fundamental assumption that the area of the pulse - defined by ABCD points- must be equal with the area defined by the EFGH points indicated in Figure 5.2.

$$\omega t_{pj} \cdot Vdc = E_{ABCD} = \int_{\omega t_1}^{\omega t_2} V_{\max} \cdot \sin \omega t \cdot d\omega t - \omega \cdot d_e \cdot (e-1) \cdot Vdc$$

$$t_{pj} = \frac{V_{\max}}{\omega \cdot Vdc} \cdot \int_{\omega t_1}^{\omega t_2} \sin \omega t \cdot d\omega t - \frac{\omega \cdot d_e \cdot (e-1) \cdot Vdc}{\omega \cdot Vdc}$$

$$t_{pj} = \frac{E \cdot Vdc}{\omega \cdot Vdc} \cdot \left[-\cos \omega t \right]_{\omega t_1}^{\omega t_2} - d_e \cdot (e-1)$$

For t_1 and t_2:

$$t_1 = \left[t'_{e-1} + (J-1) \cdot d_e \right]$$
$$t_2 = t'_{e-1} + J \cdot d_e$$

Finally, the active time (width) of the J pulse is,

$$t_{pj} = \frac{E}{\omega} \cdot \left\{ \cos(\omega t'_{e-1} + (J-1) \cdot \omega \cdot d_e) - \cos(\omega t'_{e-1} + J \cdot \omega \cdot d_e) \right\} - d_e \cdot (e-1) \quad (5.10)$$

Where, *'e'* can take values from 1 to E. For $e=1$, $t'_{e-1} = t'_0 = 0$.

According to Figure 5.2, at time interval D_e firing time $t_{\varepsilon j}$ can be expressed as

$$t_{\varepsilon J} = t'_{e-1} + (J-1) \cdot d_e + \tfrac{1}{2} \cdot t_{\delta J} \xrightarrow{or}$$
$$t_{\varepsilon J} = t'_{e-1} + (J-1) \cdot d_e + \tfrac{1}{2} \cdot (d_e - t_{pJ}) \quad (5.11)$$

where, *'e'* can take values from 1 to E.

The firing time $t_{\varepsilon j}$ and active time t_{pj} can produce the times for the beginning and the end of each pulse. These times will be called t_k, where times t_k are expressed by:

$$t_k = t_{\varepsilon j} + \left[\frac{1+(-1)^k}{2}\right] \cdot t_{pj} \qquad (5.12)$$

At this point it has to be addressed, that for time calculations of each level *"e"*, counters *J* and *k* are initialized to zero. Figures 5.3 and 5.4 illustrate the switched output voltage of two cases of the implementation of EAPWM for a *9*-level inverter with different number of initial A_{p1} pulses (*E=4,* A_{p1}*=1 and E=4,* A_{p1}*=2*).

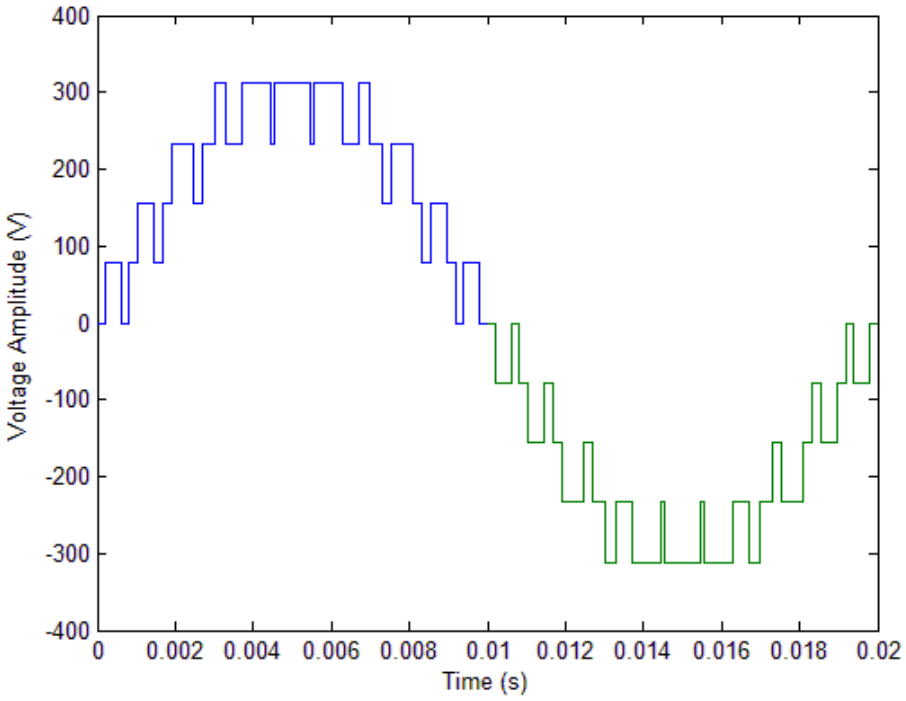


Figure 5.3 Voltage output for a 9-level inverter where E=4, A_{p1}*=1.*

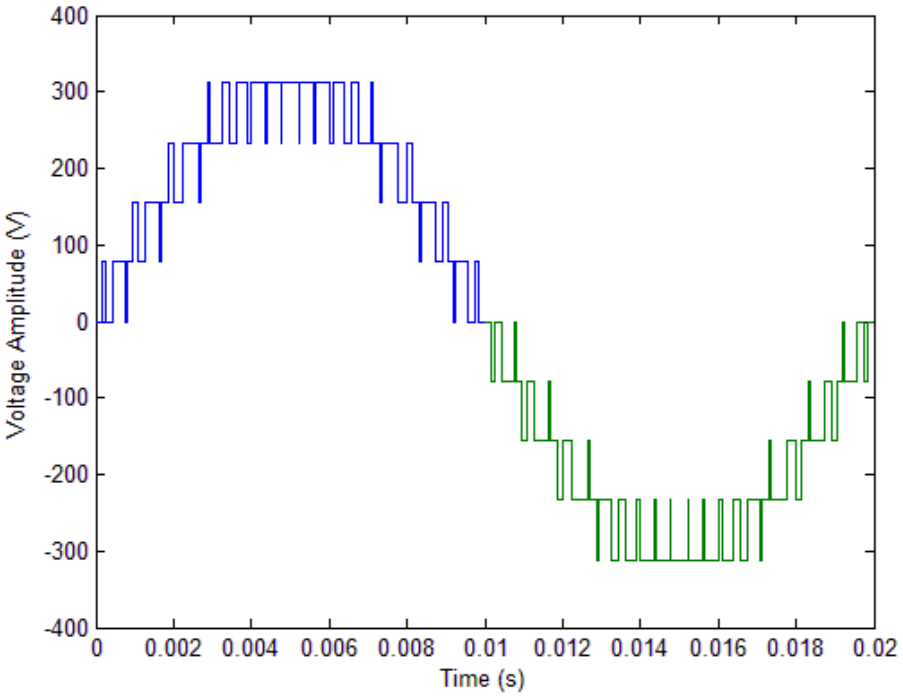


Figure 5.4 Voltage output for a 9-level inverter where E=4, A_{p1}=2.

5.2 Harmonic Analysis

Recalling the generalized Fourier equations

$$v(t) = \{a_0/2 + a_1\cos\omega t + a_2\cos\omega t + a_3\cos\omega t + ... + b_1\sin\omega t + b_2\sin\omega t + b_3\sin\omega t + ...\}$$

$$a_n = \frac{1}{\pi}\int_0^{2\pi} v(t)\cdot\cos n\omega t\cdot d\omega t$$

$$b_n = \frac{1}{\pi}\int_0^{2\pi} v(t)\cdot\sin n\omega t\cdot d\omega t$$

The term $\alpha_0/2 = 0$ for AC signals. The coefficients α_n are also zero since the function v(t) is odd and the following equation holds

$$v(-t) = -v(t) \Rightarrow a_n = 0$$

At the same time, the b_n coefficients are zero due to half wave symmetry

$$v(t) = -v(t + \frac{1}{2}T)$$

the b_n coefficients are also zero for n even:

$$n : even \Rightarrow b_n = 0$$

For n odd, $n=1,3,5,7.....$ b_n coefficients will give us the harmonic spectrum.

$$b_n = \frac{1}{\pi}\int_0^{2\pi} v_p(t) \cdot \sin n\omega t \cdot d\omega t \qquad (5.13)$$

Where, $v_p(t)$is the output pulse's voltage.

Substituting the integral by OL eq. (5.13) can be rewritten as:

$$b_n = \frac{1}{\pi} \cdot OL \qquad (5.14)$$

Integral OL can be split in as many integrals as the sources E of the inverter.

$$OL=OL_1+OL_2+OL_3+.....OL_E \qquad (5.15)$$

or
$$OL = \sum_{e=1}^{e=E} OL_e \qquad (5.16)$$

After calculations, the general integral OL_e takes the expression:

$$OL_e = -\frac{4 \cdot Vdc}{n} \cdot \left[-\cos n \cdot \omega t'_{e-1} + \sum_{k=1}^{k=k_{\max}} (-1)^k \cdot \cos n \cdot \omega t_k \right] \qquad (5.17)$$

With $k_{max}=2A_{pe}$ where $e=1....(E-1)$and $k_{max}=A_{pe}$ for $e=E$. The first term in brackets corresponds to the level changes and the second term to the actual PWM pulses.

For $e=1$, term $\cos n \cdot \omega t'_{e-1}$ becomes zero, since there is no level changing at t_0=0.

Substituting eq. 5.16 and eq. 5.17 into eq. 5.14 we have the final expression for b_n coefficients:

$$b_n = \sum_{e=1}^{e=E} \left\{ \frac{4 \cdot Vdc}{\pi \cdot n} \cdot \left[\cos n \cdot \omega t'_{e-1} - \sum_{k=1}^{k=k_{\max}} (-1)^k \cdot \cos n \cdot \omega t_k \right] \right\} \tag{5.18}$$

Figures 5.5 and 5.6 show the harmonic spectra of the implementation of EAPWM for a 9-level inverter for two switching frequency (f_{sw}) schemes, (*E=4, A_{p1}=1 or f_{sw}=1.1 kHz* and *E=4, A_{p1}=2 or f_{sw}=2.3 kHz*).

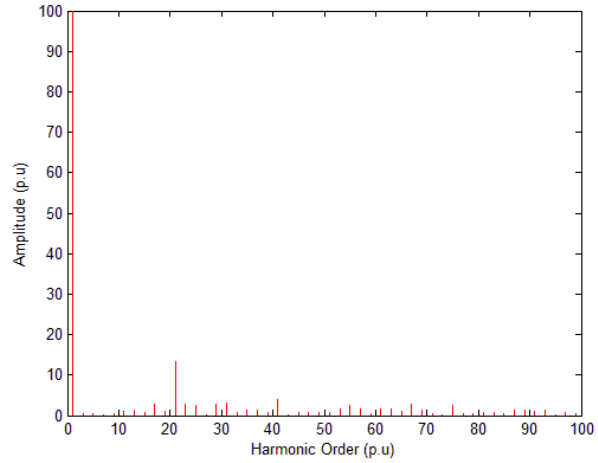


Figure 5.5 Voltage spectrum in a 9-level inverter where $V_{1,rms}$=218.6 volts and f_{sw}=1.1 kHz.

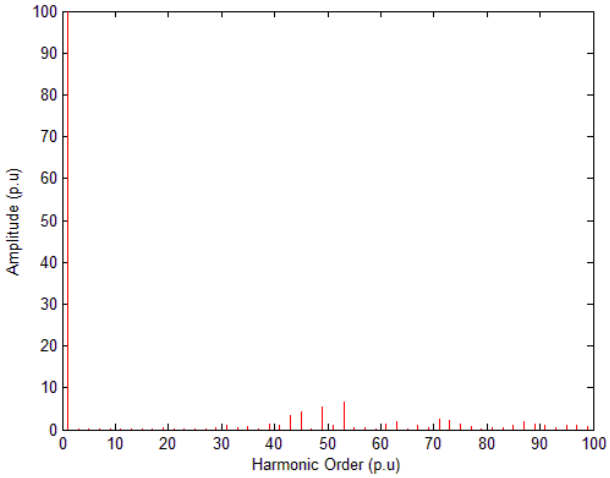


Figure 5.6 Voltage spectrum in a 9-level inverter where $V_{1,rms}$=219.7 volts and f_{sw}=2.3 kHz.

In Figures 5.5 and 5.6, f_{sw} represents the switching frequency, and $V_{1,rms}$ denotes the rms value of the fundamental harmonic. The total harmonic distortion factor (*THD*) for each case calculated until the 100th harmonic is 16.8% and 11.73% respectively.

5.3 Calculation of Total Harmonic Distortion

The percentage of total harmonic distortion (*THD*) of the voltage can be defined as

$$THD = 100 \cdot \sqrt{\left(\frac{V_{rms}}{V_{1,rms}}\right)^2 - 1} \qquad (5.19)$$

where V_{rms} is the root-mean-square (*rms*) of the output voltage, and $V_{1,rms}$ is the *rms* of the fundamental component, which can be defined as

$$V_{1,rms} = \frac{b_1}{\sqrt{2}} \qquad (5.20)$$

where, b_1 is the maximum value of the first harmonic which can be derived by eq. (5.17) setting *n=1*.

The V_{rms} can be calculated by the expression

$$V_{rms} = \sqrt{\frac{1}{T} \cdot \int_0^T v_p(t)^2 dt} \qquad (5.21)$$

For the integral of the eq. 5.21 because of the symmetry, it can be transformed to

$$\int_0^T v_p(t)^2 dt = 4 \cdot \int_0^{T/4} v_p(t)^2 dt = 4 \cdot S \qquad (5.22)$$

where, *S* is the sum of squares of $u_p(t)$ from *0* to *T/4*.

S, can also be expressed as,

$$S=S_1+S_2+S_3+\ldots. +S_E/2$$

$$\text{Or, } S=\sum_{e=1}^{E-1} S_e + \frac{S_E}{2} \qquad (5.23)$$

Where, $S_1, S_2, S_3,\ldots S_E$ are the areas of the voltage squares in each level. Since all calculations have been derived from 0 to $T/4$ the areas of upper level E are expressed as $S_E/2$. Figure 5.7 represents graphically the S_e areas.

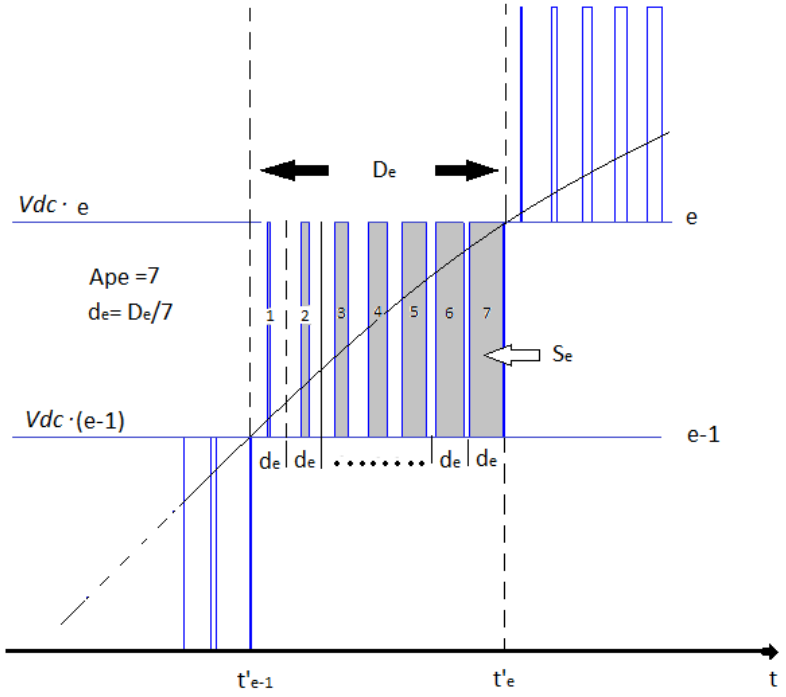


Figure 5 .7 PWM pulses between random levels "e" and "e-1".

Figure 5.7 shows a pulse series from the first pulse to the A_{pe} pulse, in a random level *"e"*. As mentioned before, between t'_{e-1} and t'_e , the number of pulses A_{pe} will determine the equal intervals d_e. In the example of Figure 5.7, number of pulses is $A_{pe}=7$ so from eq.7 the equal time intervals are $d_e=De/7$.

The area S_e in each interval in respect of t_p active time and t_δ pausing time can be expressed by

$$S_e = (e-1)^2 \cdot Vdc^2 \cdot t_{\delta 1} + e^2 \cdot Vdc^2 \cdot t_{p1} + (e-1)^2 \cdot Vdc^2 \cdot t_{\delta 2} + e^2 \cdot Vdc^2 \cdot t_{p2} + ...$$
$$... + (e-1)^2 \cdot Vdc^2 \cdot t_{\delta Ape} + e^2 \cdot Vdc^2 \cdot t_{pApe}$$

Substituting pausing time t_δ according to eq.(9) we get $t_\delta = d_e - t_p$ so,

$$S_e = Vdc^2 \cdot \left[(2e-1) \cdot \left(t_{p1} + t_{p2} + t_{p3} + ... + t_{pApe} \right) + A_{pe} \cdot (e-1)^2 \cdot d_e \right]$$

Substituting eq. 7 ($D_e = A_{pe} \cdot d_e$)

$$S_e = Vdc^2 \cdot \left[(2e-1) \cdot \sum_{J=1}^{J=A_{pe}} t_{pJ} + (e-1)^2 \cdot D_e \right] \qquad (5.24)$$

For total sum of S:

$$S = Vdc^2 \cdot \sum_{e=1}^{E-1} \left[(2e-1) \cdot \sum_{J=1}^{J=A_{pe}} t_{pJ} + (e-1)^2 \cdot D_e \right] + \frac{S_E}{2} \qquad (5.25)$$

For V_{rms}:

$$V_{rms} = 2 \cdot \sqrt{\frac{S}{T}} \qquad (5.26)$$

Since Eq. 5.19 is applied to a full bridge inverter, it can be assumed that by proper control [14] the negative and positive semi-periods of the voltage output are symmetrical, meaning no DC or even harmonics are present, and, the total harmonic distortion can be reduced to:

$$THD = \sqrt{\sum_{n=3,5,7,..}^{\infty} \left(\frac{U_n}{U_1} \right)^2} \qquad (5.27)$$

To calculate accurately the THD, it is usually necessary to calculate all the significant side-band harmonics up to the fifth harmonic of the switching

frequency f_{sw}. Equation 5.27 is also used in MATLAB to calculate the theoretical results.

5.4 Simulation and Experimental Results

To verify the proposed method, simulation and practical work in various switching frequencies and various levels were implemented. For simulation purposes a program was developed using software MATLAB R2012a to extract the voltage output and theoretical spectra of various multilevel inverters and switching frequencies. Representative examples regarding *THD* along with other significant performance factors are presented in Table 5.1, where the modulation index m_a=1. Detailed switching times for each case are presented in appendix [A2]. The MATLAB code is also presented in appendix [B3]. In order to demonstrate the EAPWM method in multilevel inverters in this chapter simulation and practical results for a 5-level and 7-level inverter with modulation indices $m_a=0.9$ and $m_a=1$ with modulation frequencies of $f_{sw}=1.1$ *kHz* and $f_{sw}=1.7$ *kHz* will be presented respectively. The switching frequencies are expressed in number of pulses in first level A_{p1}. It is important to notice that the number of pulses the user sets initially for the first level is very crucial since A_{p1} actually determines the switching frequency of the inverter. The total number of pulses per half period is always an odd number and in the first case is 11 resulting in a switching frequency $f_{sw}=1.1$ *kHz* and 17 ($f_{sw}=1.7$ *kHz)* for the second case. For the experimental results of the multilevel inverter the technical characteristics of the devices used are listed in Table 5.2.

The amplitude modulation ratio for multilevel inverters is given by

$$m_a = \frac{A_m}{(m-1)\cdot A_e} \qquad (5.28)$$

where, m is the number of levels, A_m is the reference voltage amplitude and A_e is the voltage amplitude of each *DC* source (or carrier's).

The average switching frequency for a phase-leg in all cases can be derived by the sum of the number of pulses A_{pe} divided by the period T of the reference waveform.

$$f_{sw} = \frac{(\sum A_{pe})}{T} \qquad (5.29)$$

Table 5.1: Intermediate simulation results of EAPWM in Multilevel Inverters with m_a=1.

Levels-m	Num. of A_{p1}	f_{sw} (kHz)	THD (%)	$V_{1,rms}$ (Volts)
5	1	0,5	35,57	214,4
	3	1,7	26,24	219.15
	5	3	24,3	219,8
7	1	0,8	23,2	217,6
	3	2,6	17,03	219,74
	5	4,4	15,6	219,9
9	1	1,1	17,35	218,6
	3	3,5	12,04	219,8
	5	6	10,06	219,9
11	1	1,4	13,86	219,08
	3	4,5	9,47	219,9
	5	7,5	8,55	219,96

Table 5.2: Technical characteristics of the devices used for the experimental work.

Load: resistive load (50 ohm, to limit the current)
Topology: cascaded H-bridge capable of 100V DC link for each bridge
Microprocessor: 8-bit AVR Atmel 328p
Switches: MOSFETS IRF830

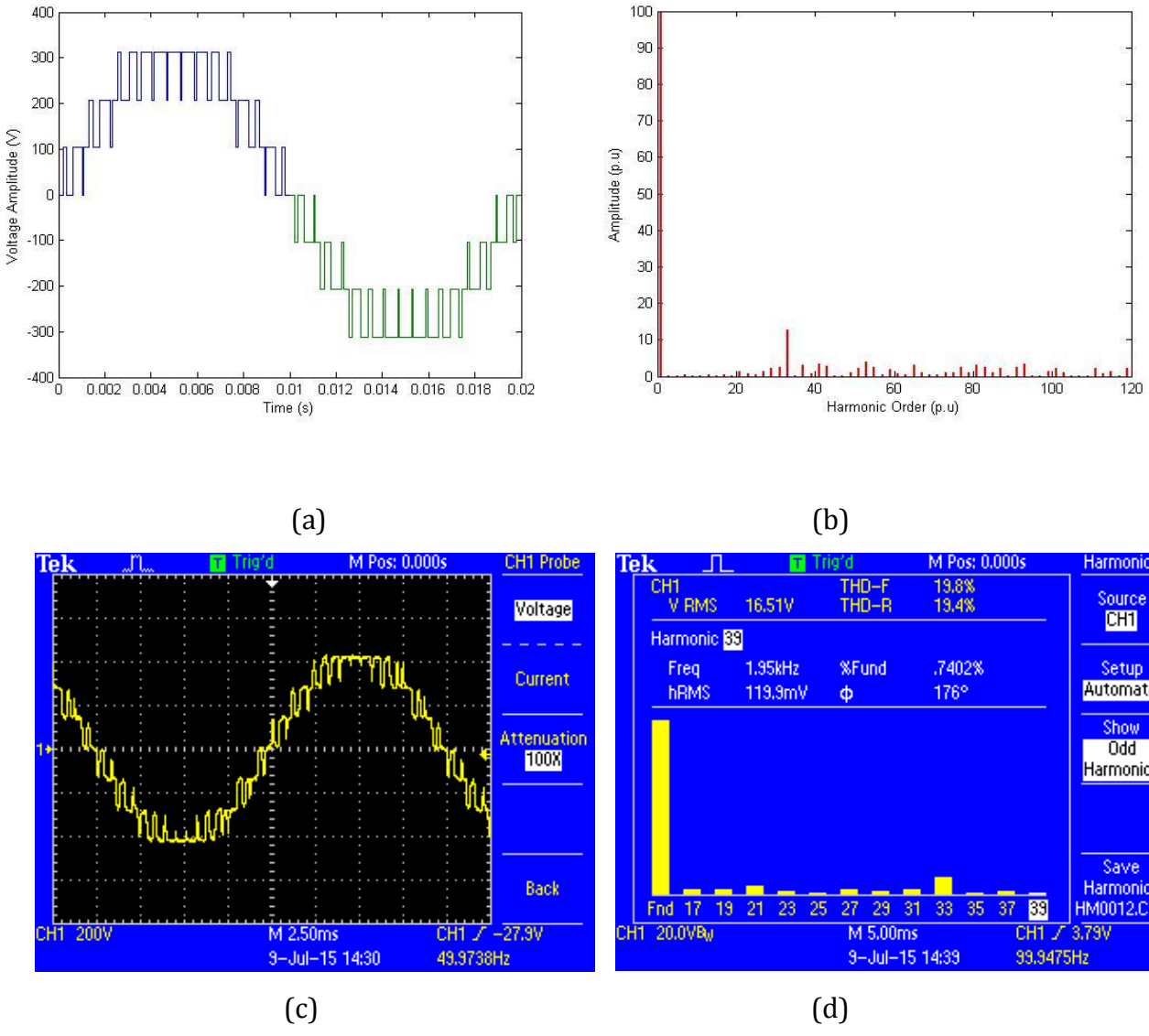


Figure 5.8 Simulation and experimental results for 7-level inverter with modulation index m_a=1 and A_{p1}=2 or f_{sw}=1,7kHz.(a) simulation switching output,(b) theoretical harmonic spectra, (c) experimental switching output, (d) experimental harmonic spectra.

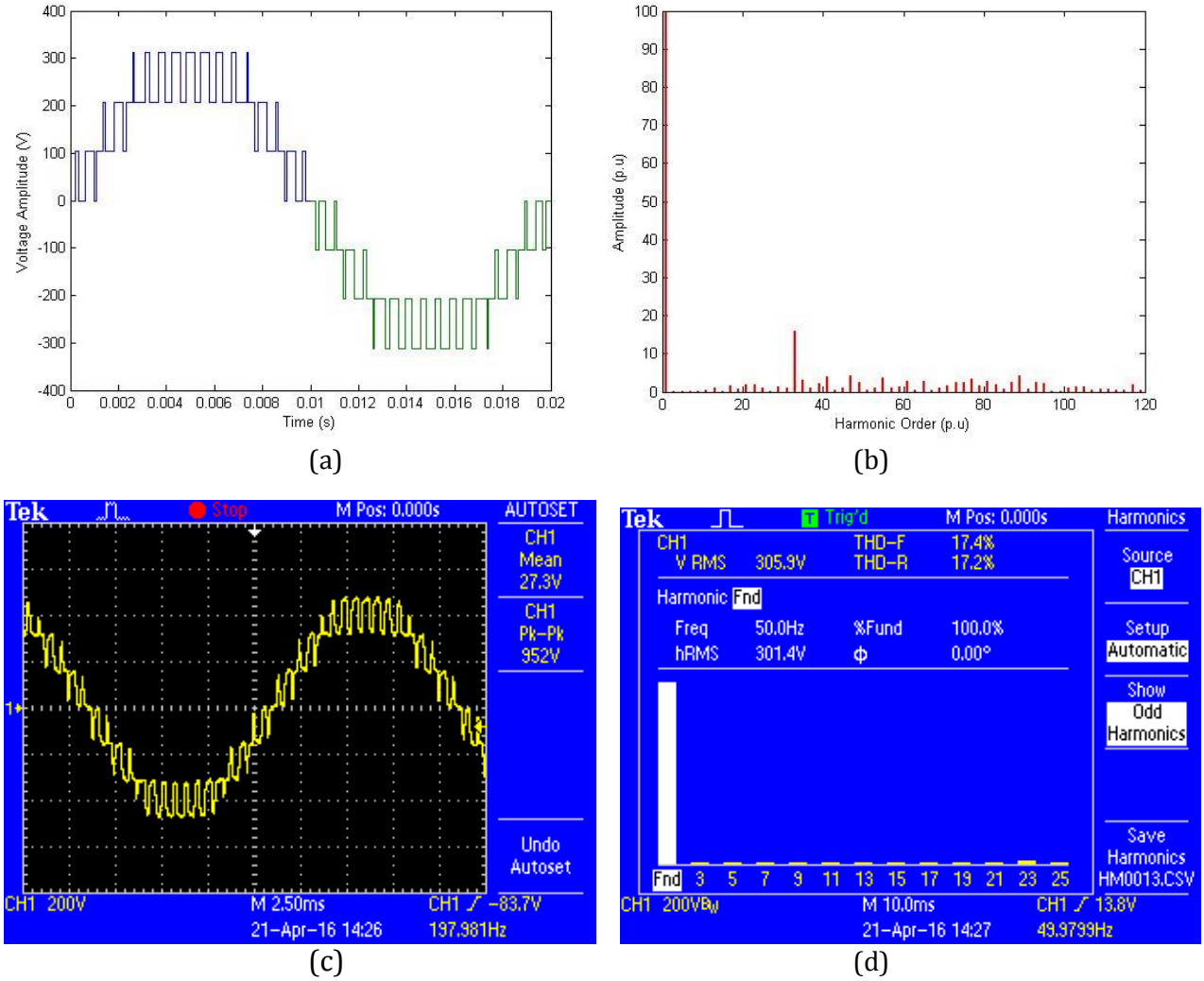


Figure 5.9 Matlab Simulation and experimental results for 7-level inverter with modulation index m_a=0.9 and A_{p1}=2 or f_{sw}=1,7kHz. .(a) simulation switching output,(b) theoretical harmonic spectra, (c) experimental switching output, (d) experimental harmonic spectra.

For simulation purposes, besides MATLAB for numerical and harmonic analysis, Proteus ISIS was used to simulate the whole system along with all switching devices, MOSFET drivers and the AVR microcontroller programming. The microcontroller used was the ATmega 328p at 16Mhz. Figure 5.10 illustrates the schematic diagram of the 7–level inverter. Optocouplers were

used in order to drive the MOSFETS and for isolation purposes for each H-Bridge inverter.

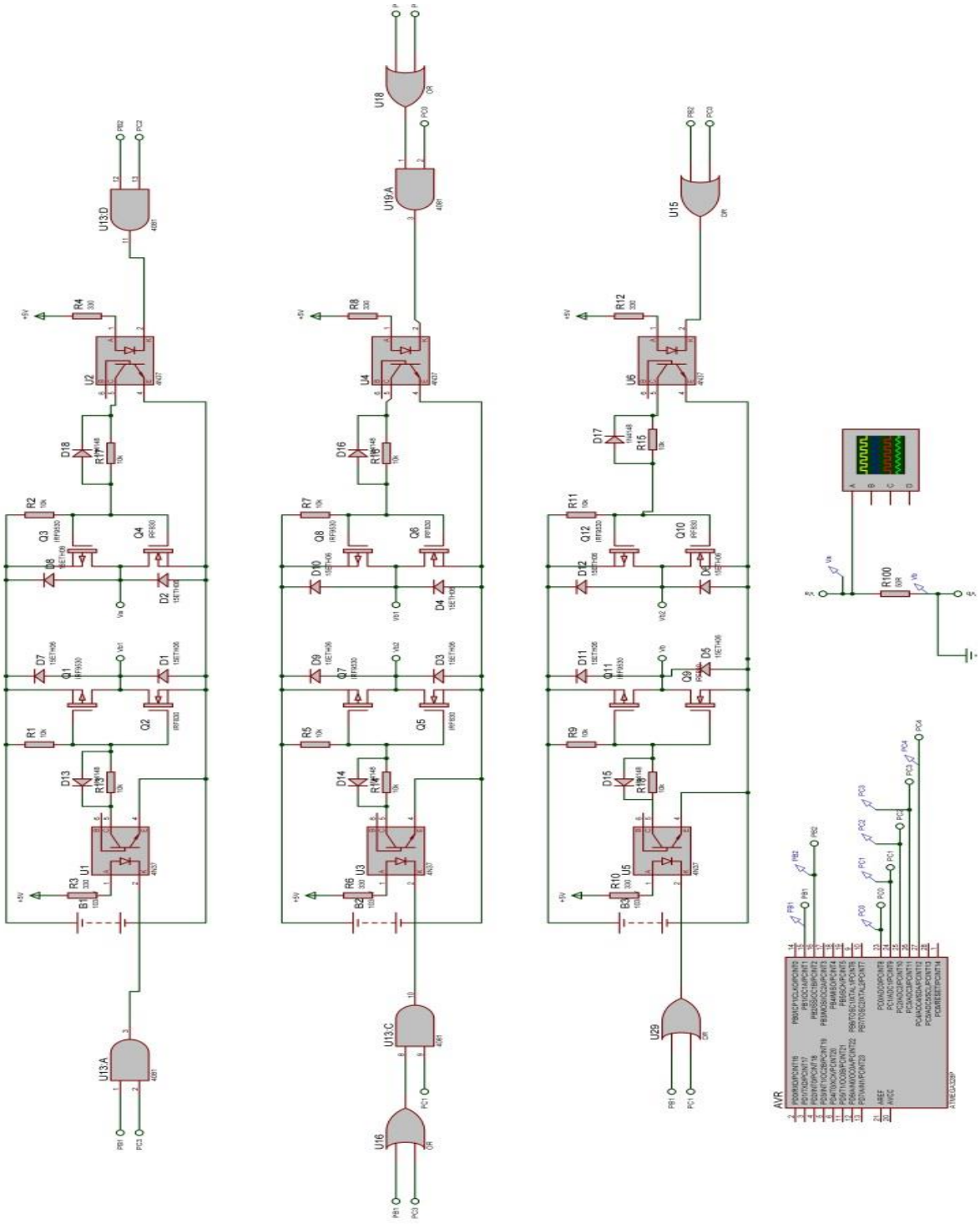


Figure 5.10 Schematic in Proteus ISIS for the simulation of a 7_level inverter.

The signals produced by the AVR where used to formulate the appropriate outputs for each H-Bridge cell. Figure 5.11 shows the initial signals produced by the AVR. In EAPWM, the switching frequency is not constant for the fundamental cycle, for the case of the 7-level inverter, the reference waveform was divided into three different areas with the associated switching frequencies.

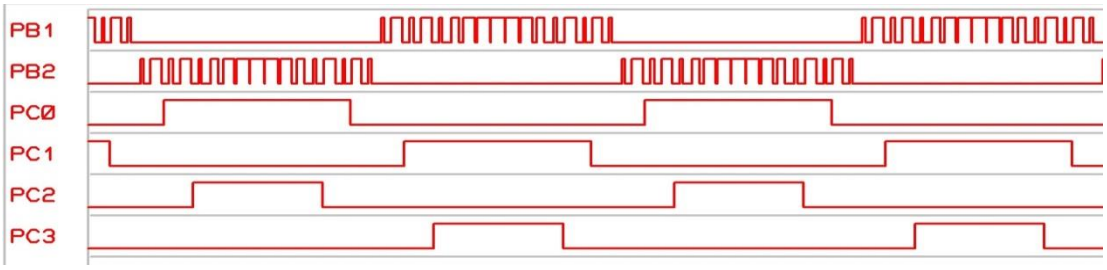


Figure 5.11 Signals produced by the programming of the AVR output.

Figure 5.12 illustrates the reference arrangement and the divisions of time intervals used for programming the AVR. In Table 5.3 (p. 134), the switching states for the 7-level inverter are illustrated along with the voltage levels and time intervals for each level. Figure 5.13 illustrates the signals produced for each phase leg of H-bridges, in order to synthesize the voltage output of the inverter.

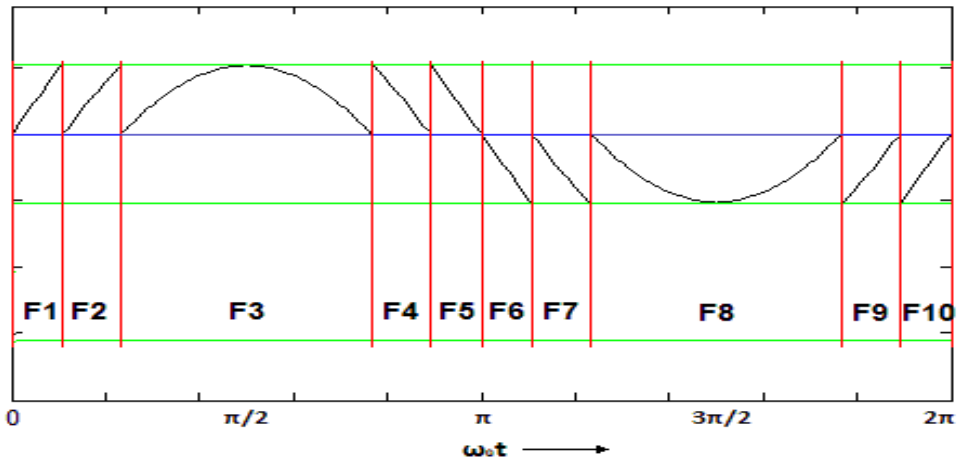


Figure 5.12 Reference arrangements for the EAPWM. F1,F2 and F3 have different time intervals. At π/2, time intervals are mirror repeated.

The final signals used to drive the gates were produced using logic gates and then were introduced to optocouplers to drive the gates of the MOSFETS as shown in the schematic diagram below.

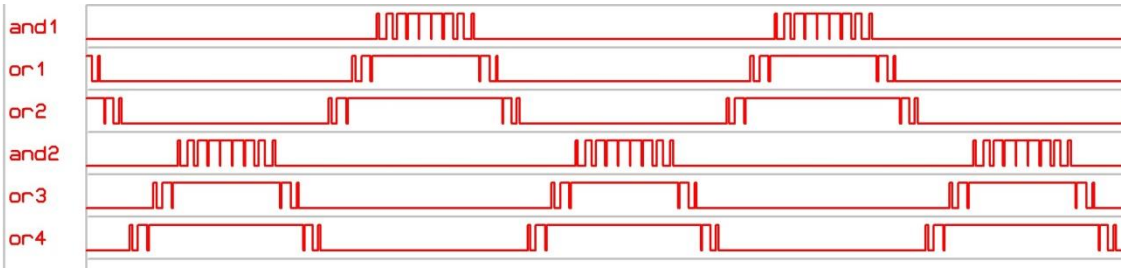


Figure 5.13 Reference waveforms. These signals feed each H-bridge phase leg in order to synthesize the output waveform.

It is evident that each H-Bridge handles different amount of switching transitions resulting in an unequal stressing for each H-Bridge. In literature, various ways of balancing this unequal stressing of the inverter cells are presented. This procedure was thought to be beyond the scope of this thesis and therefore any technique for stress balancing was not implemented. Investigation of various stress balancing techniques will be subject for further work in the future. The switched output of the inverter is shown in Figures 5.14 and 5.15. The harmonic spectrum of the output voltage is illustrated in Figure 5.16. It is clear from Figure 5.16 that the harmonic spectrum output voltage agrees with the MATLAB theoretical simulation.

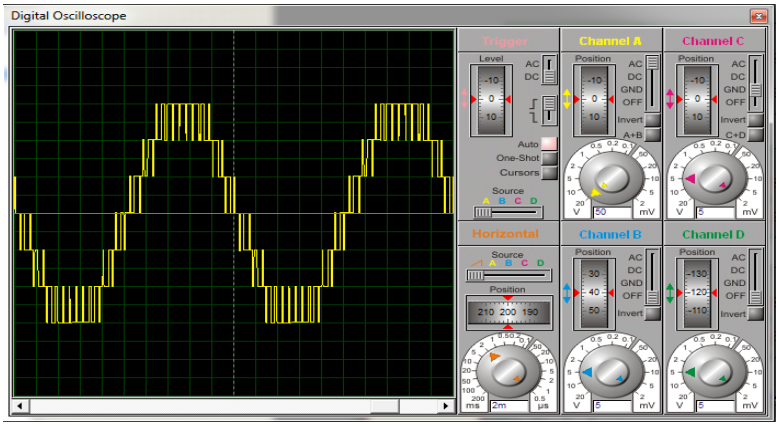
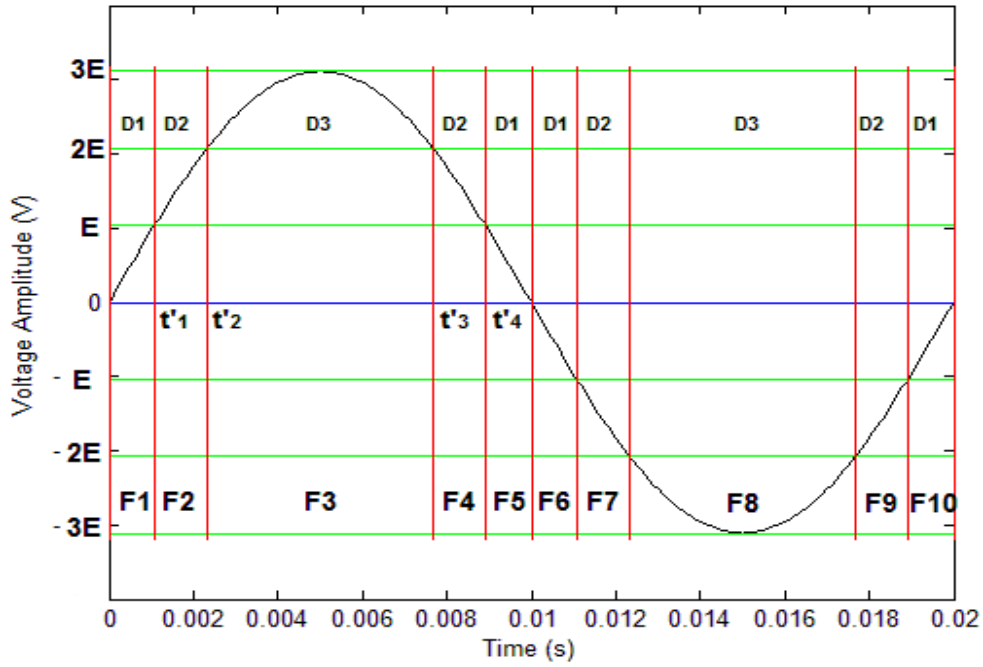


Figure 5.14 Proteus oscillator signal of the switched output of the 7-level inverter.

Table 5.3. Switching states - Voltage levels -Time intervals for the EAPWM (7-levelCascaded H-bridge inverter, m_a=1, f_s=1650Hz)

Timing	Voltage	Switching States											
		A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	C_1	C_2	C_3	C_4
F1	E	*PWM*	$\overline{PWM}$	0	1	0	1	0	1	0	1	0	1
F2	2E	*PWM*	$\overline{PWM}$	0	1	1	0	0	1	0	1	0	1
F3	3E	*PWM*	$\overline{PWM}$	0	1	1	0	0	1	1	0	0	1
F4	2E	*PWM*	$\overline{PWM}$	0	1	1	0	0	1	0	1	0	1
F5	E	*PWM*	$\overline{PWM}$	0	1	0	1	0	1	0	1	0	1
F6	-E	0	1	*PWM*	$\overline{PWM}$	0	1	0	1	0	1	0	1
F7	-2E	0	1	*PWM*	$\overline{PWM}$	0	1	1	0	0	1	0	1
F8	-3E	0	1	*PWM*	$\overline{PWM}$	0	1	1	0	0	1	1	0
F9	-2E	0	1	*PWM*	$\overline{PWM}$	0	1	1	0	0	1	0	1
F10	-E	0	1	*PWM*	$\overline{PWM}$	0	1	0	1	0	1	0	1



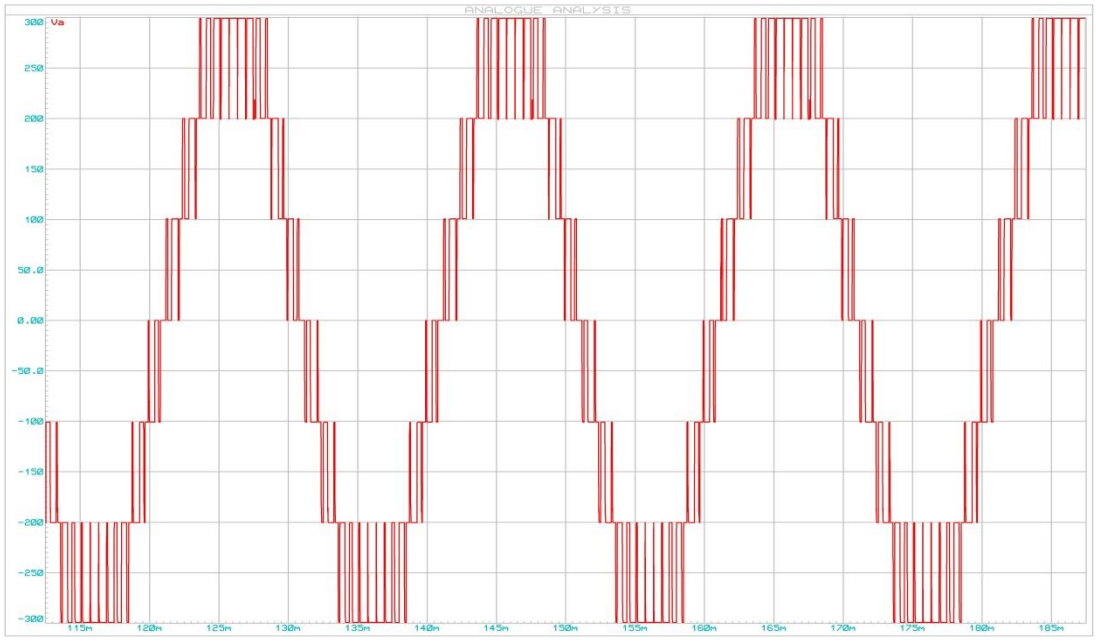


Figure 5.15 The voltage output of the 7-level cascaded multilevel inverter.

The voltage levels E are at 103.7 Volts to meet the grid requirements of 220 V (rms) for a grid tie inverter.

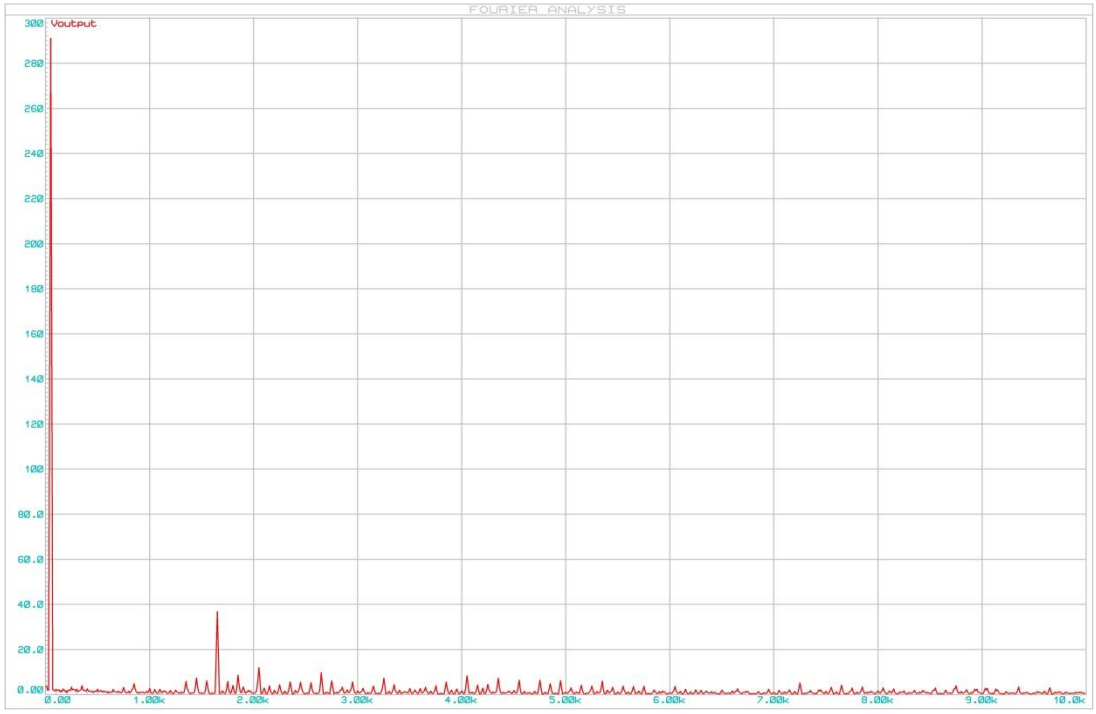
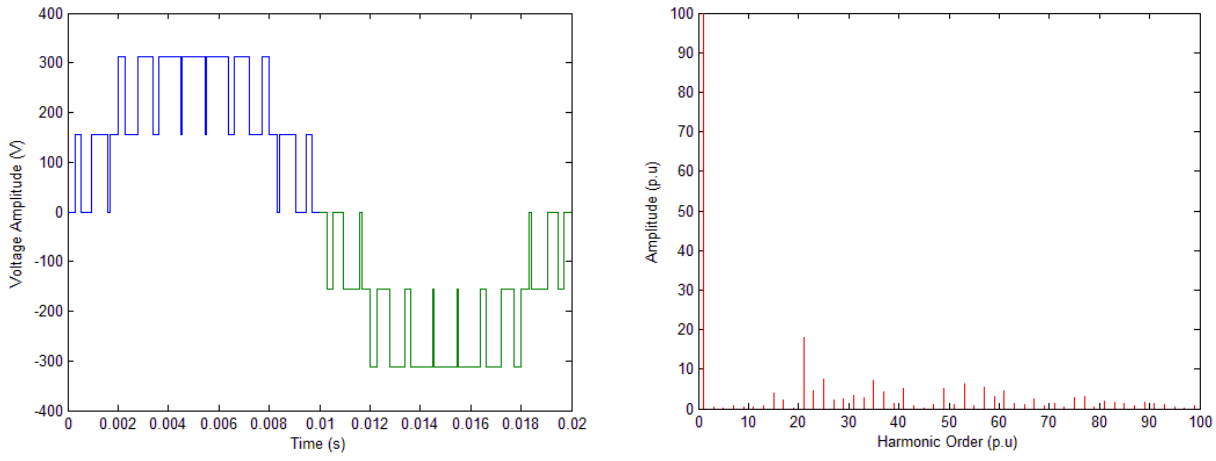


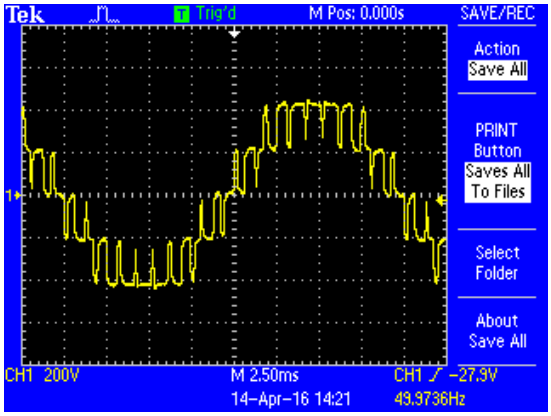
Figure 5.16 EAPWM m_a=1, fs=1650 Hz. Analytical spectrum.

Since, the overall switching transitions of one phase-leg in a discontinuous PWM scheme is occurring only in half the fundamental period T, in order to compare the results with the phase shifted PWM for the cascade topology, one has to match the number of switching transitions by doubling the switching frequency. As expected, the harmonic spectrum for $m_a=1$ is clearer from harmonics. As EAPWM is a discontinuous PWM scheme, the higher harmonic content of the output spectrum appears around the switching frequency region. This can be seen in Figure 5.8 and 5.9. For the case of 7-level inverter with $f_{sw}=1.7\ kHz$ and $m_a=1$ (Figure 5.8), the theoretical total harmonic distortion is 17.8% calculated until the 120th harmonic, while the $V_{1,rms}$ amplitude of the fundamental is 219.4V.

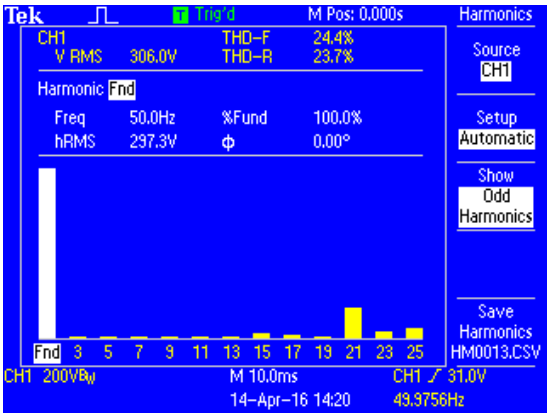
For the case of 7-level inverter (Figure 5.9), with $f_{sw}=1.7\ kHz$ and $m_a=0.9$, the theoretical total harmonic distortion is 21.08% calculated until the 120th harmonic, while the $V_{1,rms}$ amplitude of the fundamental is 197.5 V. The higher harmonic content appears at the 33rd harmonic around the switching frequency at a percentage of 15.9% of the fundamental for the case of $m_a=0.9$ and 12.7% for the case of $m_a=1$.



(a) (b)



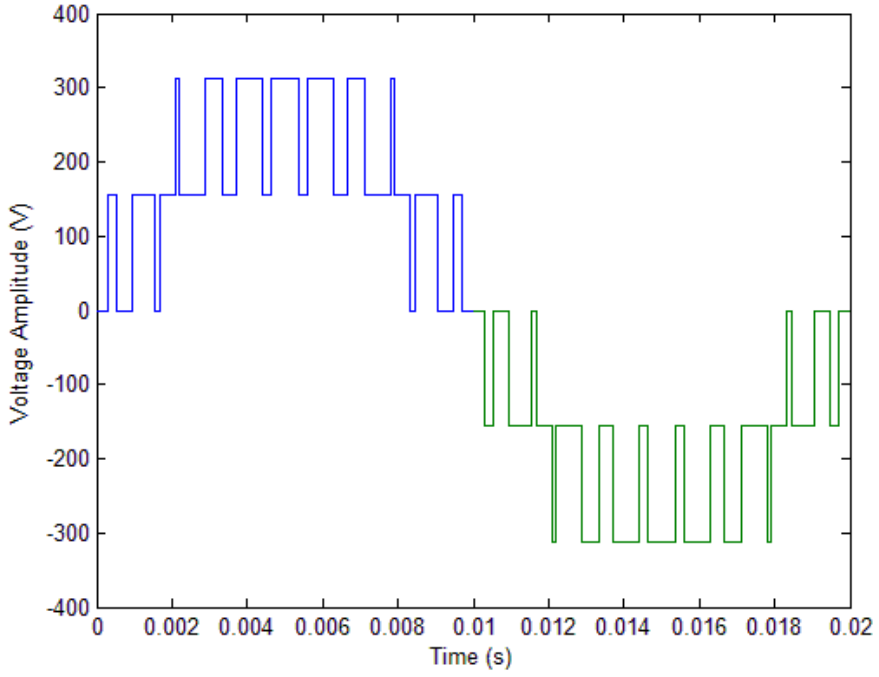
(c)



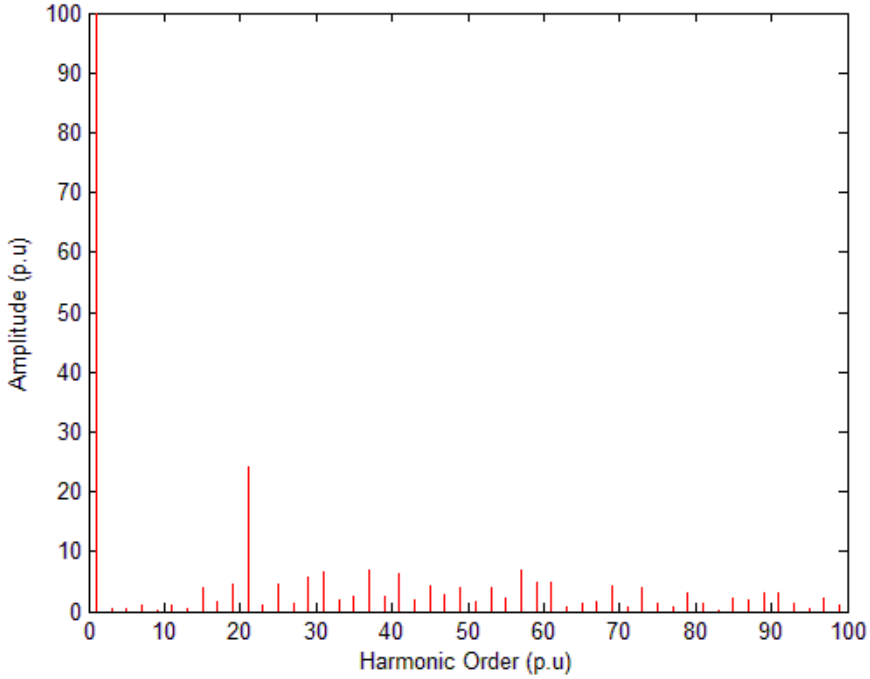
(d)

Figure 5.17 Simulation and experimental results for 5-level inverter with modulation index m_a=1 and A_{p1}=2 or f_{sw}=1.1 kHz.(a) simulation switching output,(b) theoretical harmonic spectra, (c) experimental switching output, (d) experimental harmonic spectra.

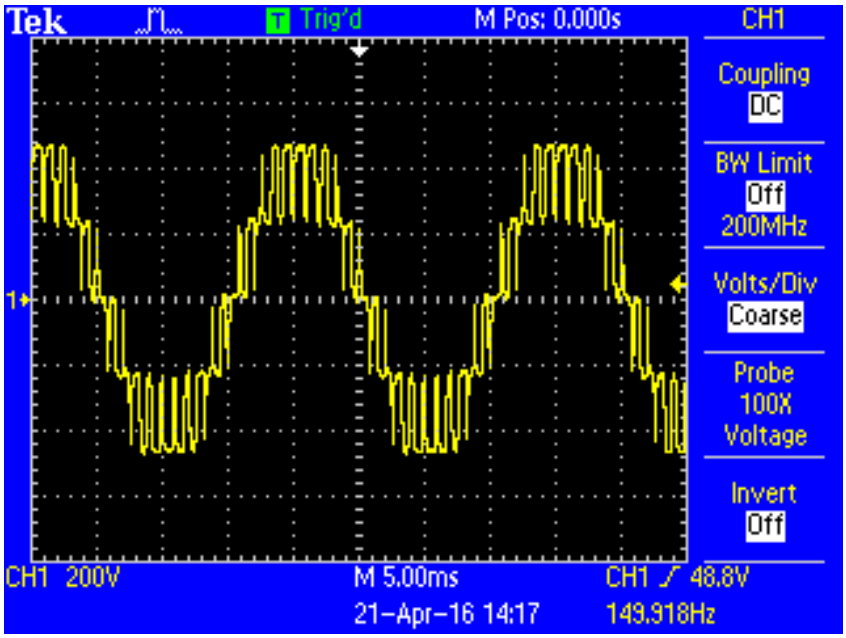
For the case of 5-level inverter with f_{sw}=1.1 kHz and m_a=1 (Figure 5.17), the theoretical total harmonic distortion is 26.72% calculated until the 120th harmonic, while the $V_{1,rms}$ amplitude of the fundamental is 218.7V.



(a)


Amplitude (p.u)
Harmonic Order (p.u)
0
10
20
30
40
50
60
70
80
90
100

(b)


Tek
Trig'd
M Pos: 0.000s
CH1
Coupling
DC
BW Limit
Off
200MHz
Volts/Div
Coarse
Probe
100X
Voltage
Invert
Off
CH1 200V
M 5.00ms
CH1 48.8V
21-Apr-16 14:17
149.918Hz

(c)

(d)

Figure 5.18 Simulation and experimental results for 5-level inverter with modulation index 0.9 and A_{p1}=2 or f_{sw}=1.1 kHz. .(a) simulation switching output,(b) theoretical harmonic spectra, (c) experimental switching output, (d) experimental harmonic spectra.

For the case of 5-level inverter in Figure 5.18, with f_{sw}*=1.1 kHz* and m_a*=0.9*, the theoretical total harmonic distortion is 32.7% calculated until the 120th harmonic, while the $V_{1,rms}$ amplitude of the fundamental is 196.9V. The higher harmonic content appears at the 21st harmonic around the switching frequency at a percentage of 24% of the fundamental for the case of m_a*=0.9* and 17.9% for the case of m_a*=1*.

Regarding the oscilloscope measurements, there are two typical definitions used when dealing with Total Harmonic Distortion. The following definitions are taken from the Tektronix oscilloscope manual - "*The two types of Total Harmonic Distortion are THD–F and THD–R. They both are figures of merit used to quantify harmonic levels in voltage and current waveforms; however, each one uses a different reference. THD–F is a comparison to the fundamental and THD–R is a comparison to the signal's RMS value. For power systems, the THD–F is the most accurate measurement especially when there is high harmonic content. The*

THD–R measurement can be prone to misinterpretation which can easily lead to measurement errors when measuring larger distortions. THD–F Total Harmonic Distortion in reference to (F) fundamental represents the ratio, in per cent, of the voltage/current harmonic components relative to the voltage/current of the fundamental. When the reference is not indicated (i.e. simply THD), then it is usually assumed the reference is fundamental." The difference that occurs between simulation and experimental results, regarding the THD measurements, comes also from the number of harmonics that are included on the theoretical calculations.

5.5 Modulation alternatives for the individual H-Bridge inverters of a multilevel inverter using the Cascade topology.

It is known that when the carrier frequencies are set to achieve the same number of inverter switch transitions over each fundamental cycle, alternative phase opposition disposition (APOD) PWM strategy for diode clamped multilevel inverters produces the same harmonic performance as phase shifted cascade PWM (PSCPWM) for cascade multilevel inverter topology. In diode clamped multilevel inverter topology, phase disposition (PD) strategy can achieve its best performance by placing most of the harmonic energy into the carrier harmonic in each phase leg and then relying upon the cancellation of this harmonic in the line-to-line voltages.

McGrath and Holmes, as mentioned in Chapter 2, utilizing the above concept, developed a PWM method for cascaded and hybrid inverters to achieve the same superior harmonic gains as phase disposition (PD) PWM achieves for diode-clamped inverters. Since, the method developed by McGrath and Holmes achieved superior harmonic results for the cascade multilevel inverters this thesis has adapted the same modulation strategy. In order to compare the results obtained from the experimental and simulation work of this thesis, first

it is useful to comprehend the modulation strategy used for the implementation of EAPWM in the cascade multilevel inverter topology.

Two alternatives could be formulated and applied for the modulation of individual H-bridge inverters of a multilevel inverter using the cascade topology. One alternative is to use continuous two-level modulation. This strategy can be achieved by comparing a single reference waveform (a sinus) against phase shifted carriers by 180^0. This solution is known to be harmonically inferior against three-level modulation and therefore is not chosen.

The second alternative is to use discontinuous modulation. This strategy can be achieved by PWM modulating only one of the two phase legs in each H-bridge at any one time. For the first positive half-period of the switched output, one phase leg is PWM modulated and the other is held to the negative dc voltage rail. For the negative half-period of the switched output, the first phase leg is held to the negative dc voltage rail, and the other phase leg is now PWM modulated. The outcome of this modulation strategy is the difference between the two phase legs resulting in a three-level PWM waveform which retains a main carrier harmonic component.

Furthermore, in order to maintain the same number of switching transitions as for three-level continuous modulation and since only one phase leg switches at a time, the carrier frequency can be doubled. After doubling the carrier frequency, the carrier sideband harmonics in the harmonic spectra, occur around the same effective carrier frequency as for three-level continuous modulation. It is worth noting that in order to maintain the same phase for the carrier harmonic at all times the carrier for each phase leg must be modulated with an 180^0 phase-shift. This is necessary for achieving the cancellation between the multilevel inverter phase legs.

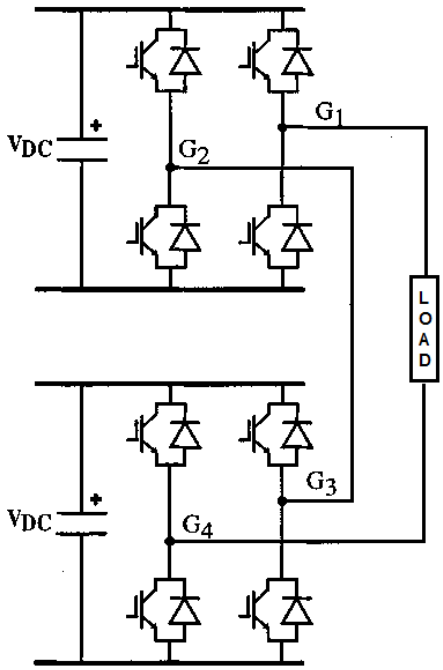


Figure 5.19 Five-level inverter using Cascade topology.

In Figures 5.19 and 5.20 a five level inverter and the modulation signals from each phase leg for the cascade multilevel inverter are illustrated, operating under discontinuous modulation. The reference waveform must be divided into sections, where each H-bridge inverter synthesizes the appropriate section of the switched output of the multilevel inverter. It can also be seen, that after one fundamental cycle the positive G1-G3 and negative G2-G4 output signals of each phase leg alternate their respective fundamental reference sections for the next fundamental cycle. This occurs in order to balance the switching load for each phase leg. This deliberate movement of the reference waveform sections between cascade inverters is also one more advantage of this strategy unlike the PD-modulated diode clamped inverter, where this imbalance cannot be corrected. While this strategy looks as a quite complex modulation strategy to formulate, for a digital modulator or a microprocessor this discontinuous scheme of this PWM pattern makes the process quite easy and straightforward.

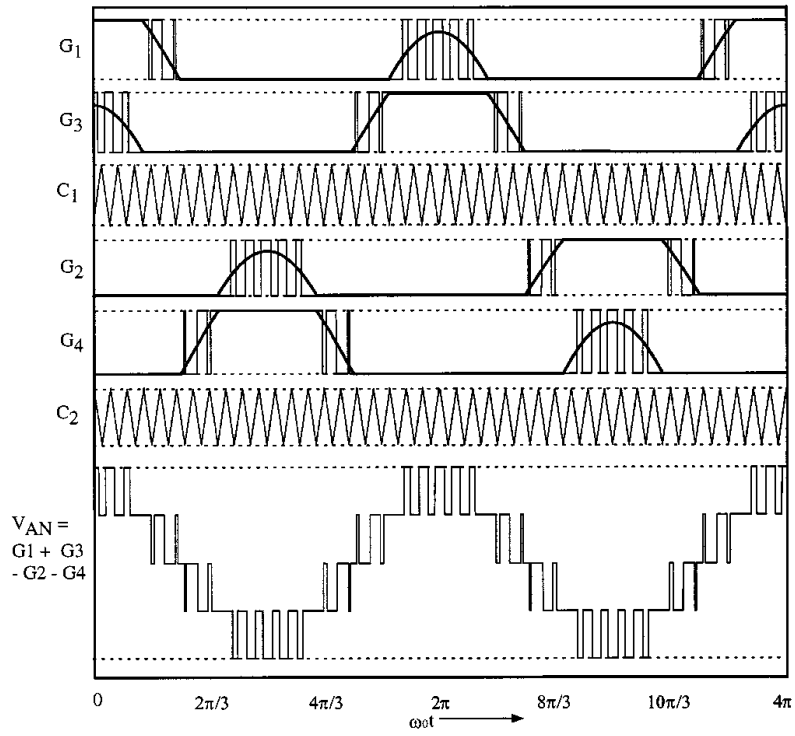


Figure 5.20 Reference and Carrier waveforms for 5-level cascaded inverter, with reference movement for balancing switching losses over two fundamental cycles.

5.6 Comparison of EAPWM results against the main PWM methods for MLI under Cascade topology.

In order to compare the experimental and simulation results obtained in this thesis, the case of a 5-level inverter will be used against the experimental and simulation results produced by McGrath and Holmes [6]. Two main PWM methods for multilevel inverters using Cascade topology exist, the phase shifted PSCPWM, and the PD for cascaded inverters developed by McGrath and Holmes in (2002). In Figure 5.21, simulation and experimental results of the EAPWM switched output along with the harmonic spectra of a 5-level inverter are illustrated. In Figure 5.22, the harmonic spectra of the phase leg voltage and the line-to-line voltage using the PSCPWM is illustrated. In Figure 5.23, the harmonic spectra of the phase leg voltage and the line-to-line voltage using the

PD PWM is illustrated. In all cases modulation index is m_a=0.9, and same switching conditions of f_s=1050 Hz are met.

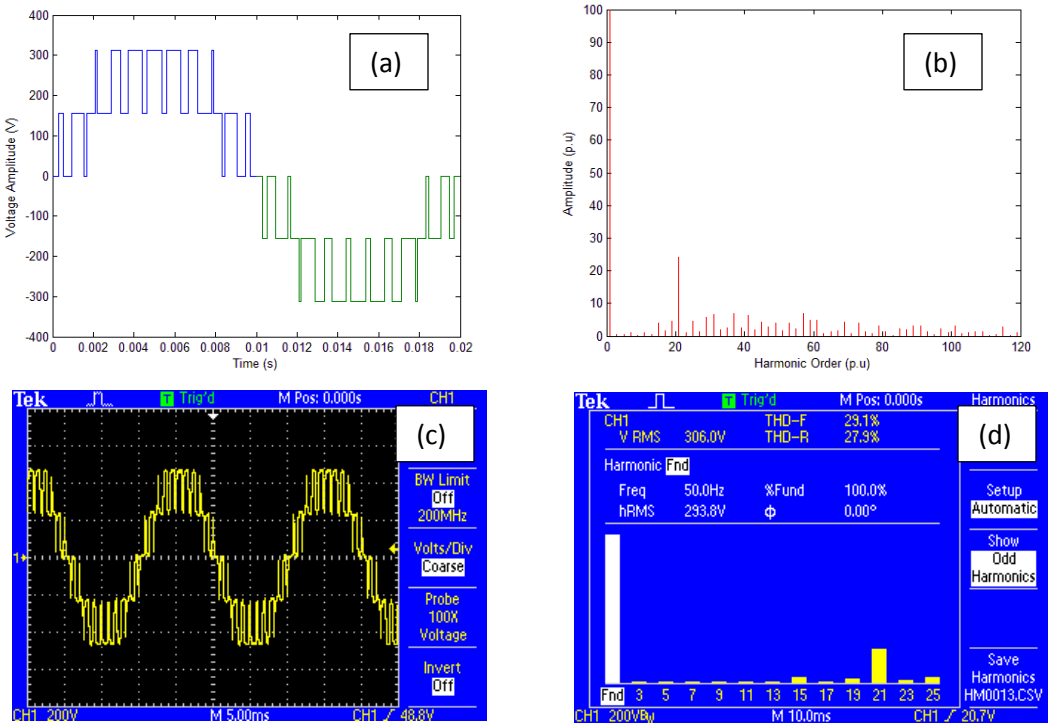


Figure 5.21 Simulation and experimental results of the EAPWM for 5-level inverter.

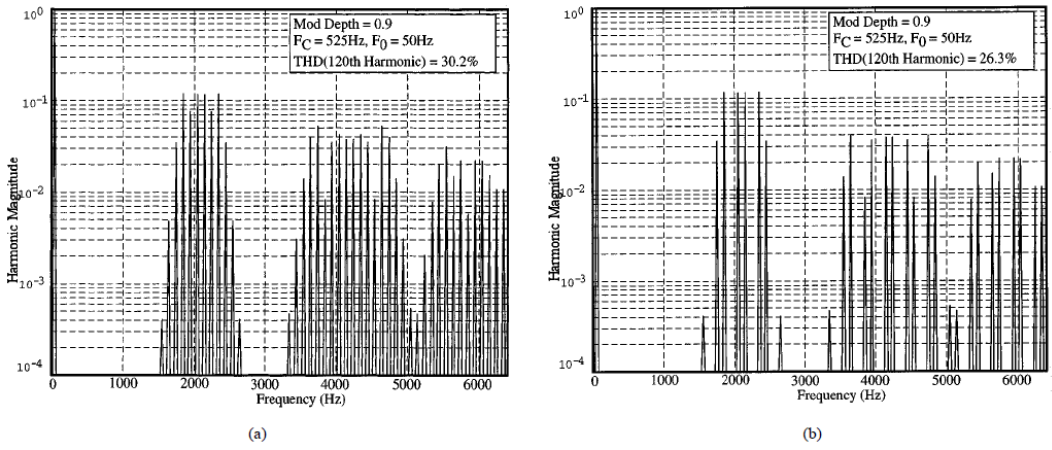


Figure 5.22 PSCPWM for 5-level inverter: (a) single-phase output voltage, (b) line-to-line voltage.

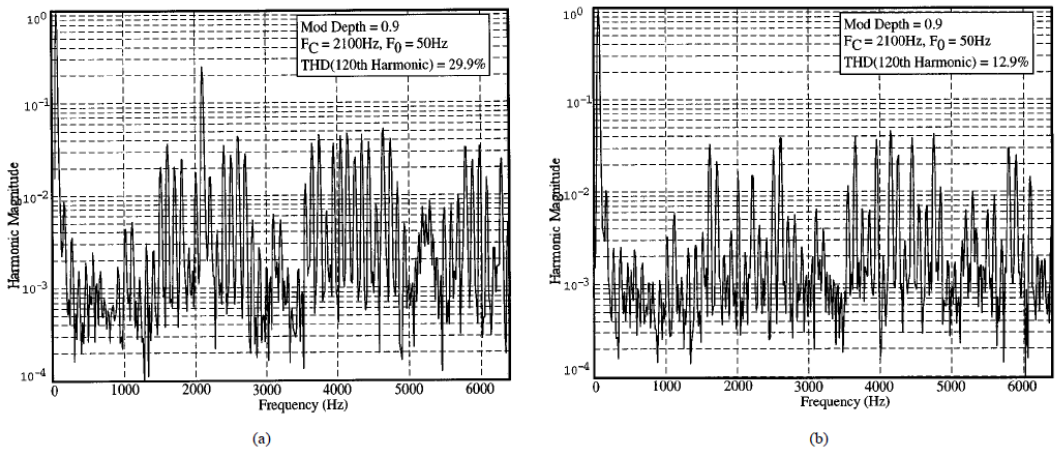


Figure 5.23 Bipolar Discontinuous PWM for cascaded 5-level inverter, single-phase output voltage- experimental spectrum, (b) line-to-line voltage- experimental spectrum.

The experimental results for the single-phase 5-level cascaded inverter showed a THD of the voltage output, of 29% using EAPWM, while PSCPWM a value of 30.2% and PD PWM a value of 29.9%, all calculated until the 120th harmonic. In Fig. 5.21(b),(d) and 5.23(a) it is illustrated that both, the proposed EAPWM and the bipolar discontinuous PD PWM, show a clear carrier component on the output voltage spectrum, since the higher harmonic energy is gathered around the first carrier group. Relying in the cancellation between the phase legs, on a three phase system, the carrier harmonic component can be eliminated resulting in a lower line-to-line voltage THD.

5.7 Summary

This chapter proposes an alternative micro-processor PWM technique for multilevel inverters implementing the Equal Areas PWM technique which was introduced in [1], [2]. This method expands the opportunities of digital online implementation in a wide range of applications since from the algebraic matching of the volt/second areas, less computational effort is needed. The findings of the implementation of EAPWM in multilevel inverters are critical since this method can also be used as a reference method for performance comparison to other digital PWM methods of regular sampling. The computer simulations showed that EAPWM switching scheme can synthesize a sinusoidal waveform with less computational effort. Further work to verify the performance of the EAPWM technique will be carried out by experiments based on a prototype multilevel inverter expanding the operation of the multilevel inverter to the overmodulation region by modifying the basic algorithm of EAPWM.

In order to optimize the operation of the multilevel inverter, regarding the modulation index, this thesis presents the development of a modified algorithm based on Algorithm B discussed in Chapter 4. This modification algorithm, able of introducing values of $m_a>1$, will be illustrated in Chapter 6.

CHAPTER 6

Modified Algorithm of EAPWM for the Over Modulation Region in Multilevel Inverters

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Introduction

In this chapter the basic algorithm of the Equal Areas PWM for multilevel inverters is being modified to allow the operation of the multilevel inverter to enter the overmodulation region. The basic algorithm developed by the implementation of the equal areas theory in multilevel inverters is able to produce pulse width modulation for a range of modulation indices limited to one. This restriction comes to foreground due to the overlapping of pulses when the modulation ratio exceeds one ($m_a>1$). In Chapter 3, this limitation has been evident to the EAPWM for three-level conventional voltage source inverters. In Chapter 4, it was addressed that three modified algorithms where developed to overcome this limitation by rearranging the areas for the implementation of the equal areas criteria by resetting the modulation ratio for those pulses that tend to overlap. The algorithms are able to overcome the modulation ratio limitation by utilizing three different ways of rearranging the "volt/second" areas, to fulfill the equal areas criteria. In the case of multilevel inverters, one modified algorithm is produced using the same approach to overcome the limitation, and discussed in this chapter. Simulation and experimental work has been carried out to validate the algorithm performance.

6.1 Overmodulation of Cascade H-Bridge Multilevel Inverters

To determine the behavior of multilevel cascaded H-bridge inverters in the overmodulation region, for naturally sampled and regular sampled modulation schemes, the equations of the switched output have to be recalled. While these

equations are quite complex, their complexity is mainly based on the different amplitudes of the harmonic terms. The new harmonic components are created in the baseband region at frequencies of $[2n-1]\omega_0 t$. That means that in a similar fashion as in the overmodulation of the conventional inverter case, these harmonics can be identified as low-order harmonics created by the overmodulation procedure, as the reference waveform approaches a square wave [1]. Moreover, by cascading H-bridges into a multilevel inverter, it is known that harmonic cancellation of the side band harmonics can be achieved. The importance of this observation is that since *m* cascaded H-bridges are used for a (2*m+1)*-level multilevel inverter, this harmonic cancellation is not affected by overmodulation. Hence, it is expected to achieve the same harmonic benefits of cascaded full-bridges for any modulation index. This characteristic of the Cascade topology is one more criterion that this thesis took into consideration for choosing this topology for the implementation of the proposed PWM scheme. In Figure 6.1 the harmonic spectra of a *5-level* cascaded inverter for a modulation index of $m_a=1.2$ is illustrated. It is evident that the cancellation of the sidebands again occur up to the fourth carrier multiple in the same manner as in the linear modulation region [2].

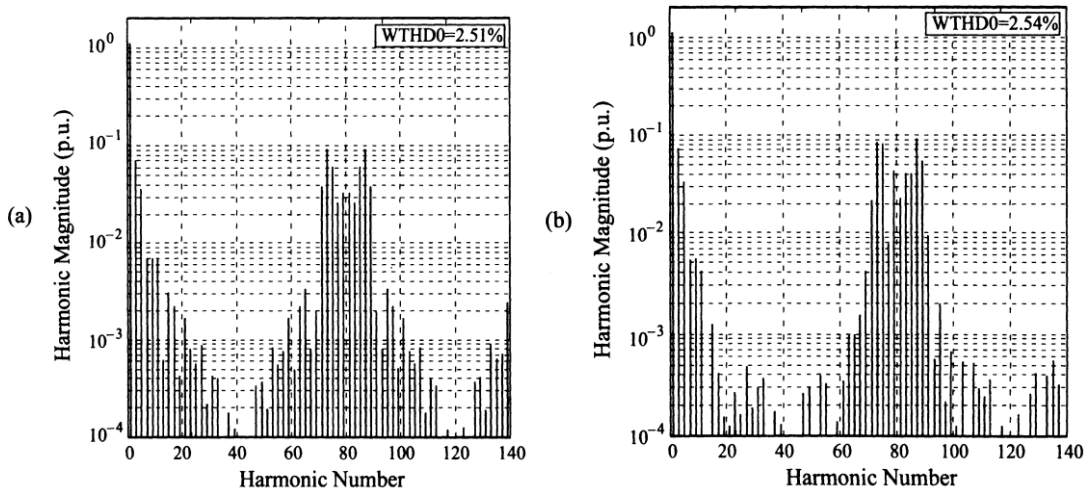
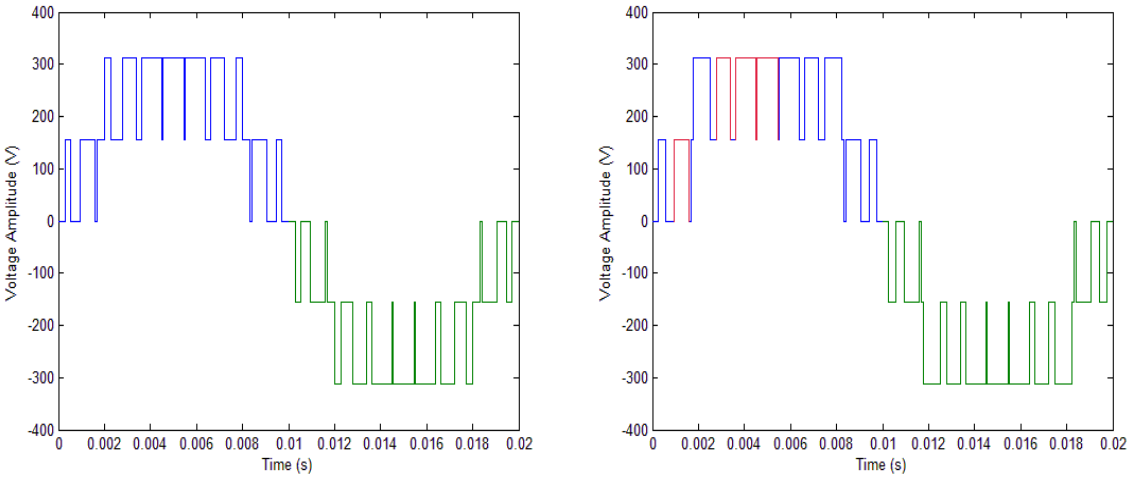


Figure 6.1 Theoretical Spectra of a 5-level cascaded inverter under, (a) naturally sampled and (b) asymmetric regular sampled, modulation $m_a=1.2$.

6.2 EAPWM Modified algorithm for Multilevel Inverters

This modified algorithm is aimed to introduce modulation ratios higher than one expanding the linear region of the multilevel inverter. As developed in Chapter 4, the modified algorithm will use the space between the pulses as a freedom of pulse positioning within the time interval. The criteria to implement the positioning of the pulse would be the avoidance of pulse overlapping due to the increase of the modulation ratio. When the modulation ratio increases at values higher than one, the pulses tend to widen further than the time interval that is set from the user at the beginning. If for example in a 5-level inverter with $A_p=2$ number of pulses in the first level ($f_{sw}=1.145\ kHz$), and a modulation ratio of $m_a=1.4$ introduced, then 4 pulses have to be recalculated since they have been out of boundaries. The algorithm will reduce the width of those overlapped pulses recalculating its width replacing the modulation ration to its marginal value in the linear region, which is one. Then the algorithm, if no other overlap occur will continue with the remaining pulses to be calculated using the initial modulation ratio $m_a=1.4$. In Figure 6.2 the above case is illustrated showing the switched output for both modulation ratios, $m_a=1$ and $m_a=1.4$. The highlighted pulses are the pulses which have gone out of boundaries and have been recalculated. It is important to remember that the calculations take place until $\pi/2$ so, only pulses 2, 4, 5, 6 need to be recalculated. Pulses 1 and 3 are calculated using $m_a=1.4$. This technique as shown in Chapter 4, for the conventional three-level inverter, can extend the linear region of the inverter before entering the overmodulation region. This method can be used in applications where the need for excessive voltage amplitude on the fundamental harmonic is what matters as in an asynchronous motor drive. Simulation and experimental results have been carried out validating the modified algorithm. Figures 6.3 to 6.6 illustrate the simulation and practical work for two cases of multilevel inverters. The first case is of a 5-level inverter and second case for a 7-level inverter. The MATLAB code developed to produce

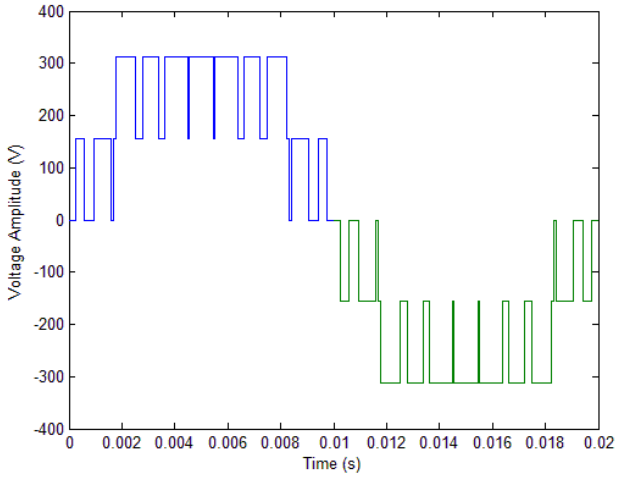
the time switching instants for the modified EAPWM for multilevel inverters is presented in [B4].



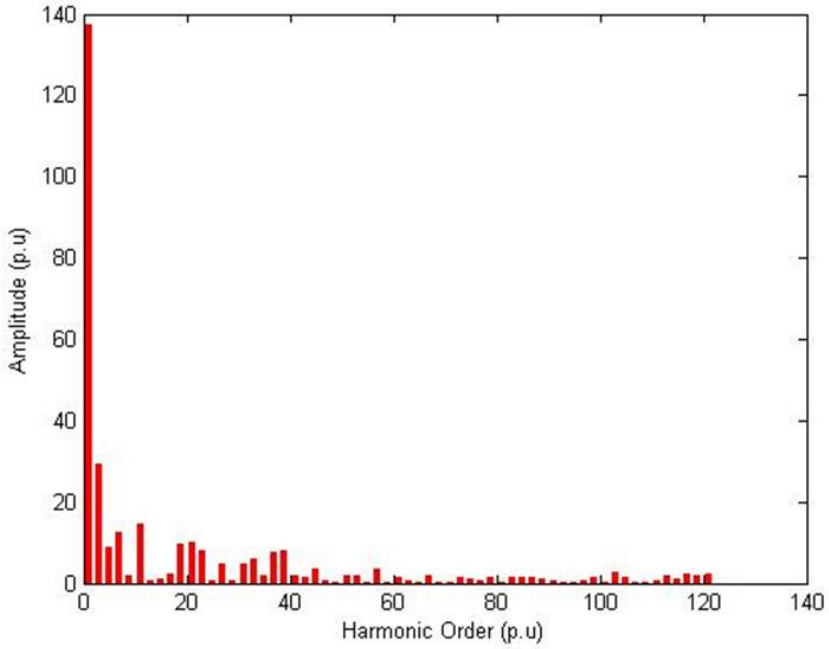
(a) (b)

Figure 6.2 5-level switched output for (a)m_a=1 and (b) m_a=1,4.

Simulation Results have been acquired for 5-level and 7-level inverter with modulation ratio m_a=*1.4* at a switching frequency of f_{sw}=*1.145 kHz* and f_{sw}=*1.713 kHz* respectively. The total harmonic distortion for each inverter case has been calculated until the 120th harmonic component. For the first case THD is 27.22% and for the second case it is 17.81%.

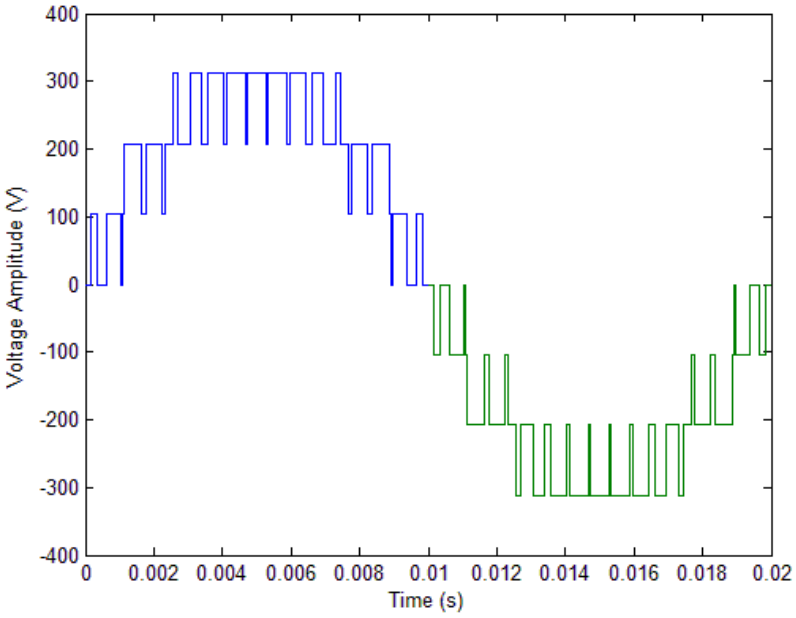


(a)

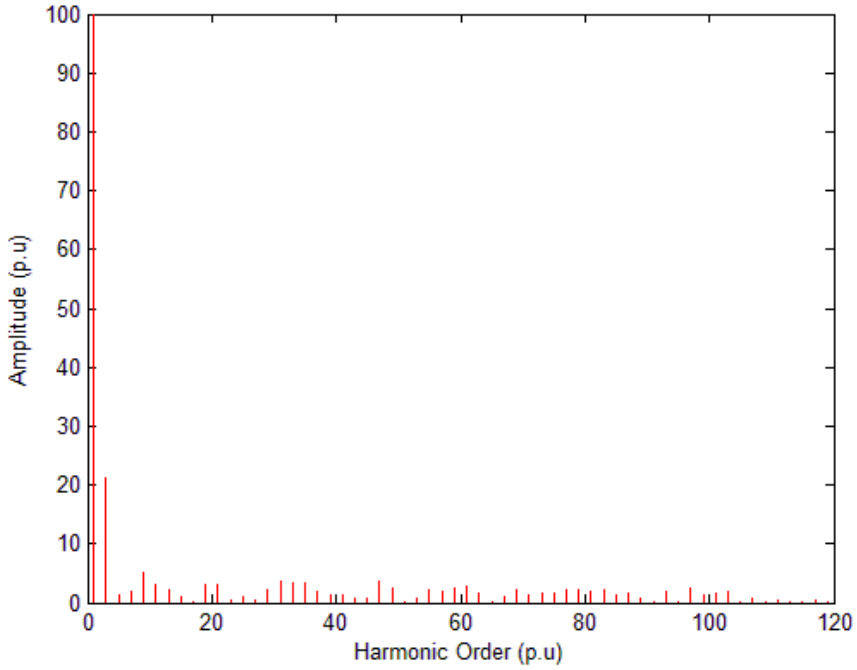


(b)

Figure 6.3 Simulation results for the 5-level inverter with m_a=1.4 and f_{sw}=1.145 kHz. (a)switched output, (b) harmonic spectra of the output.



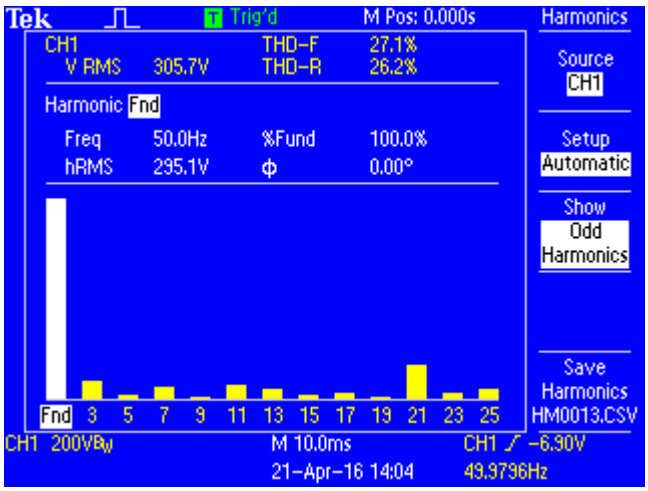
(a)



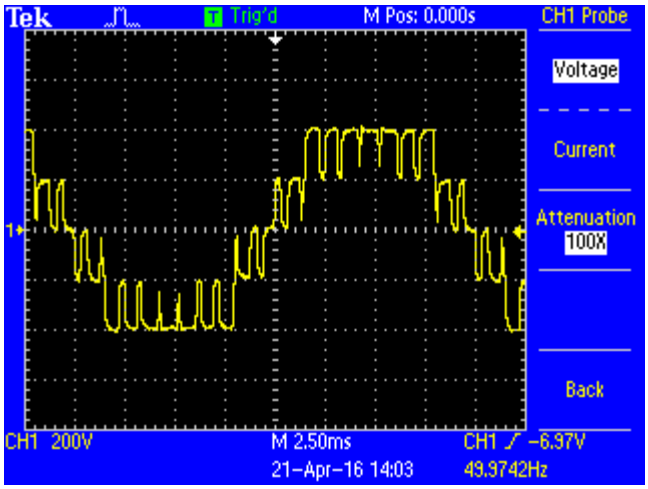
(b)

Figure 6.4 Simulation results for the 7-level inverter with m_a=1.4 and f_{sw}=1.713 kHz. (a)switched output, (b) harmonic spectra of the output.

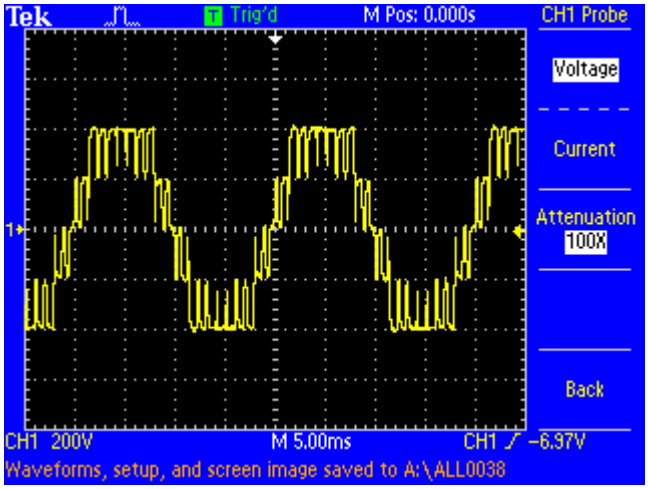
Experimental results for 5-level and 7-level inverter with modulation ratio m_a=1.4 at a switching frequency of f_{sw}=1.145 kHz and f_{sw}=1.713 kHz respectively.



(a)



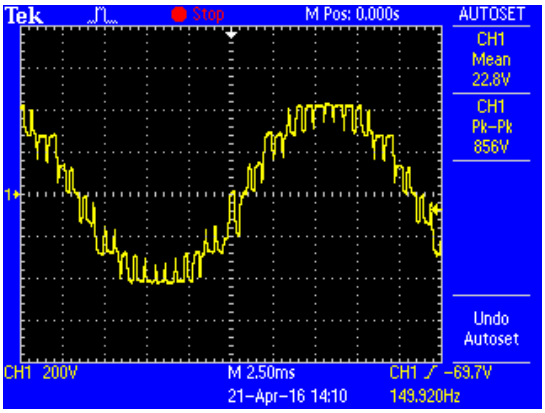
(b)



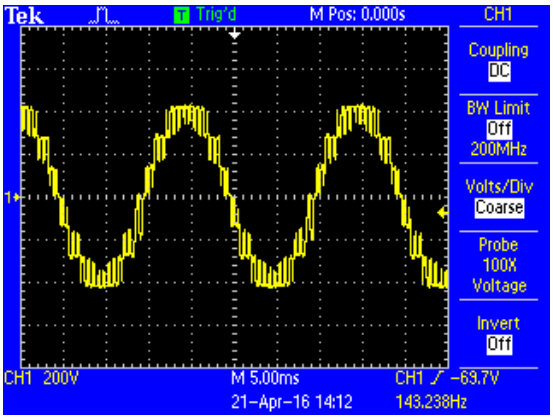
(c)

Figure 6.5 Experimental results for the case of 5-level inverter with m_a=1.4 and f_{sw}=1.145 kHz. (a)harmonic spectra of the output, (b)switched output, (c) switched output (2T).

(a)



(b)



(c)

Figure 6.6 Experimental results for the case of 7-level inverter with m_a=1.4 and f_{sw}=1.713 kHz (a)harmonic spectra of the output, (b)switched output, (c) switched output (2T).

6.3 Evaluation and conclusions of the implementation of the proposed method EAPWM in Multilevel Inverters

The proposed PWM method for multilevel inverters presented in this thesis is quite different than other carrier-based PWM schemes as far as the frequency ratios are concerned. Carrier-based PWM methods for Multilevel inverters, utilize carrier frequencies at integer multiples of the fundamental frequency. The carriers applied for all levels of an m-level inverter are always on the same frequency. Phase disposition and phase shifting of these carriers are then used to create different schemes for the pulse width production. In this method, each level is treated in a separate manner. For example in EAPWM in Figure 6.7, the duration of each level of a 7-level inverter is being defined by the cross section of each V_{dc} source with the reference waveform (sinus) in a half period. The cross sections of the equal V_{dc} sources with the sinus waveform define the fundamental switching times for each level. Then, the user sets the number of pulses for the first level, i.e. $A_p=2$. That means that, the time duration of the first level is going to be divided by 2 creating two equal time intervals for the pulses to be centered. As described in chapter 5, the number of pulses for the next levels is going to be distributed in an analogous way. Since the number of pulses for each level (A_{pe}) is now known, the equal areas criteria are then utilized to define the width of each pulse and the generated pulse is centered at the time interval (d_e) created in each level's duration (D_e). For the 7-level inverter the distribution of pulses in each level is shown in Figure 6.8 and the analysis of the time intervals for the first half of the reference waveform in Table 6.1.

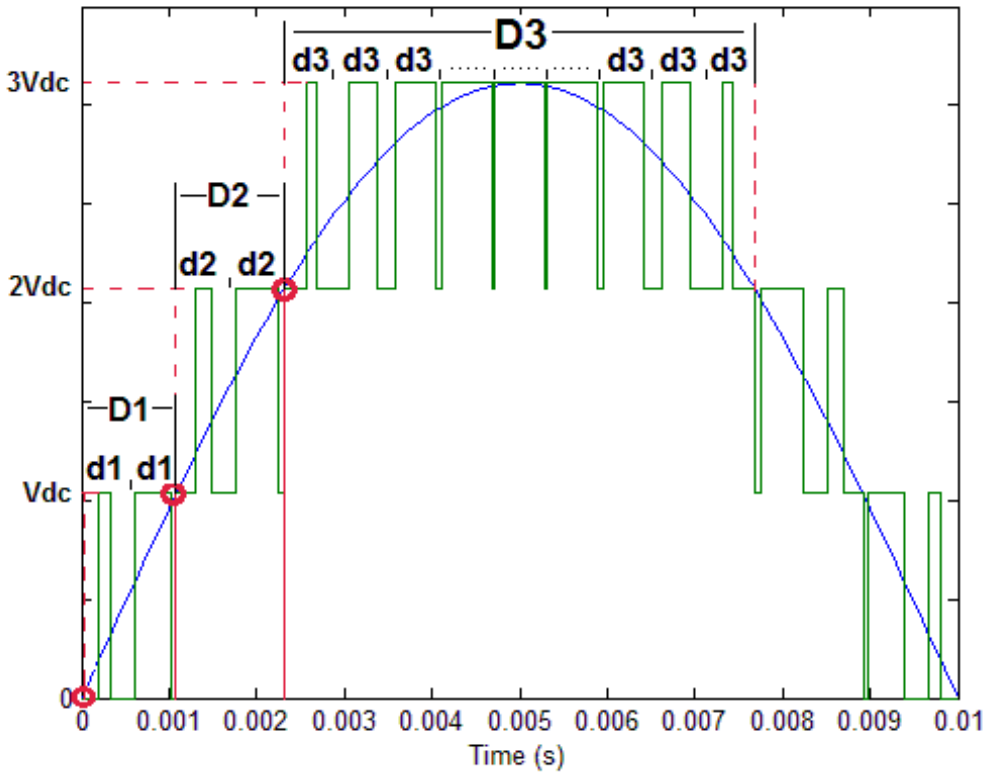


Figure 6.7 The duration of each level and corresponding time intervals for a 7-level inverter.

Table 6.1. Analysis of time intervals and frequency levels for a 7-level inverter.

Level	A_p	Level duration D_e (ms)	Time (carrier) interval $d_e=De/A_p$(ms)	Level freq. $1/d_e$ (kHz)
1	2	1.0817	0.5409	1.8489
2	2	1.2411	0.6205	1.6115
3	9	5.3544	0.5949	1.6809

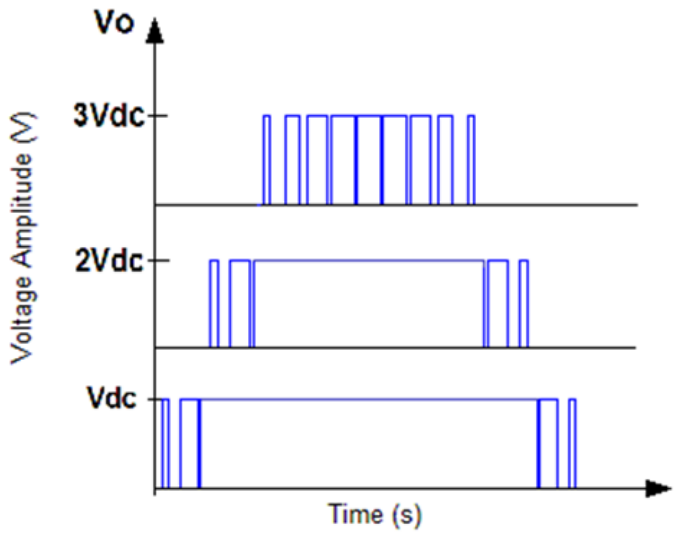


Figure 6.8 Distribution of pulses in each level for a 7-level inverter with EAPWM.

From what has been discussed thus far it becomes apparent that this method creates non-integer frequency ratios. This affects the harmonic spectra of the switched output of the multilevel inverter, especially for low frequency ratios. In some of literature reviewed, non-integer frequency ratios are claimed to introduce sub-harmonics below the fundamental harmonic component. However, simulation and practical work showed that any harmonics that may occur in this region are only low order "carrier" sideband components. The amplitudes of these sideband harmonics are negligible after the first few components. The selection of the appropriate frequency ratio can become complex for more sophisticated PWM strategies. Essentially the choice depends mostly on how fast the sideband harmonics from the first frequency ratio (m_f) group roll off in magnitude away from the switching frequency. This can be seen in Figures 7.4 and 7.5 where the harmonic spectra of the switched output of the 7-level inverter for low and higher switching frequencies are illustrated. In Figure 6.9 the switching frequency is f_{sw}*=1.7137 kHz* and the ratio is m_f*= 34.27* where in Figure 6.10 the frequency ratio is m_f*=94.29* and f_{sw}*=4.7145 kHz*. The side band harmonics appear in the region of the switching frequency ratio m_f, considering also that this method is a discontinuous PWM.

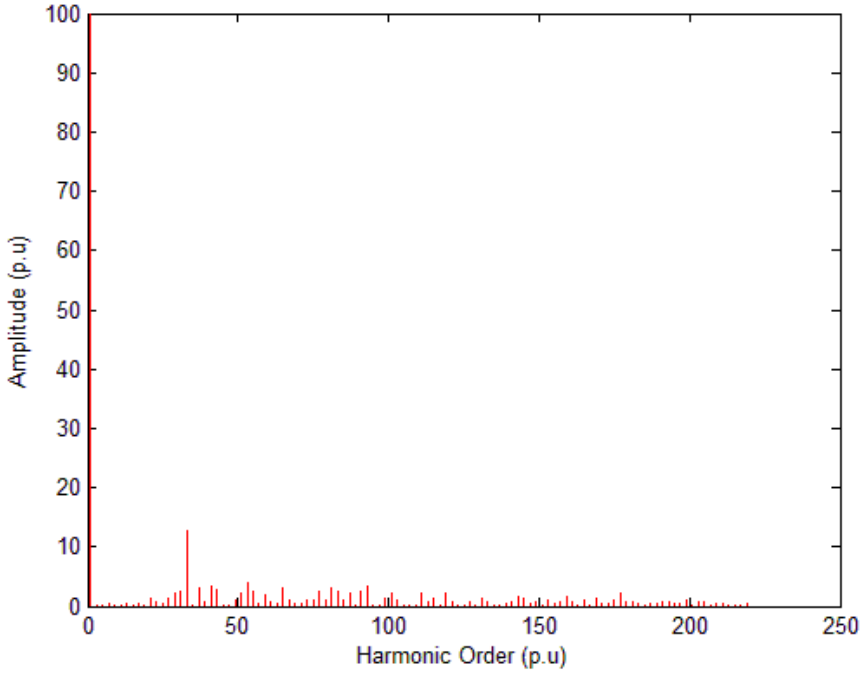


Figure 6.9 Harmonic spectra for the switched output of a 7-level inverter with A_{p1}=2 and m_f=34.27, THD=18.6%.

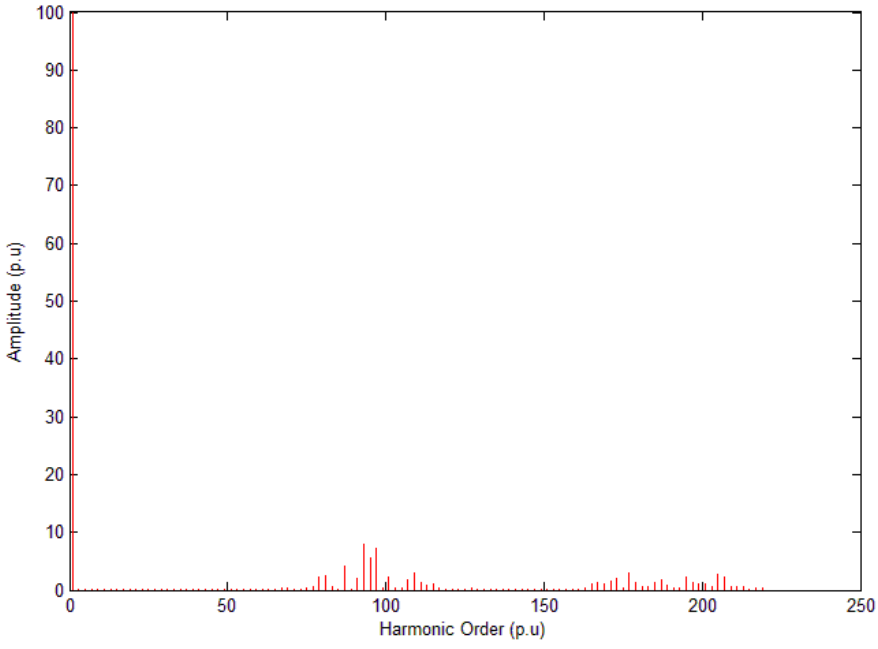


Figure 6.10 Harmonic spectra for the switched output of a 7-level inverter with A_{p1}=5 and m_f=94.29, THD=15.7% .

A 5-level inverter was chosen for comparison with other methods since same conditions where easier to meet. Significant reduction in THD occurred from the proposed EAPWM as shown in Table 6.2. A significant advantage is that even with lower switching frequency f_{sw}, EAPWM presents lower THD results against the two main PWM schemes used for the cascaded H-bridge topology as illustrated in Table 6.3.

Table 6.2 THD of carrier-based PWM schemes for a 5-level Cascaded Single-phase Inverter.

Modulation index	5-level Cascaded Single-phase Inverter, fsw=1050Hz, f0=50Hz, THD calculated until the 40th Harmonic				
Ma=0.8	**PD**	**POD**	**APOD**	**PS**	**EAPWM**
THD%	39.85	39.86	39.85	40.06	32.21
Ma=1	**PD**	**POD**	**APOD**	**PS**	**EAPWM**
THD%	27.97	27.5	27.98	28.18	22.79

Table 6.3 THD of carrier-based PWM schemes for a 5-level Cascaded Single-phase Inverter.

f0=50Hz, fsw=3050Hz	THD% (200th Harmonic)		
Ma=1	**PD**	**PS**	**EAPWM**
7-level	18.47	17.29	16.97 (2.7kHz)
9-level	13.40	13.86	13.37 (2.5kHz)
11-level	11	11.48	10.58 (3.1kHz)

6.4 Summary

In this chapter the modified algorithm produced for a conventional inverter to expand the linear operation of the converter, was implemented to a single-phase cascaded H-bridge multilevel inverter. In particular, algorithm B was explained and analyzed showing more interest since, by its implementation transposition of the linear operation after each recalculation point, was occurred. Moreover, comparison results showed the advantage of the proposed method against the main PWM schemes used in multilevel inverters, in terms of THD and switching frequency.

CHAPTER 7

Conclusions and Further Work

The concept of using the equal area criteria in order to determine the switching angles for a PWM converter is not new. On August 1987, Yoone Ho Kim and Mehrad Ehsani [1], proposed a new direct pulse width modulation method. Their proposed method, described the technique where, the pulse widths are determined by equating the incremental areas of the reference signal with the output pulse areas. The authors claimed that their method achieved less harmonic distortion than natural and regular sampling methods. On December 1988, Sidney R. Bowes [2] published a discussion to demonstrate that the so-called new direct PWM method was in fact a reinvention of the conventional regular-sampled PWM technique, which has been widely used for research and industrial applications for over the past 20 years. The discussion paper demonstrated some crucial omissions made by Yoone Ho Kim and Mehrad Ehsani regarding the calculation of the THD numerically, which led to incorrect conclusions on the harmonic performance of the method. On the other hand, the literature reviewed in this thesis, showed that this direct PWM method has been classified as one of the three significantly different alternatives for determining the converter switch on times for fixed-frequency modulation systems. This debate, which was a critical incentive for this thesis, was the starting point to evolve and research the initial idea of equal areas method not only to conventional inverters but also to the up to date trend of multilevel inverters. The method proposed relied on the formulation of more analytical

mathematical equations for the determination of the switching angles. The EAPWM method proposed in this thesis used only odd numbers for the half-fundamental cycle, in contrast to the work carried out by Yoone Ho Kim and Mehrad Ehsani, where only even values of pulses were introduced. The choice of odd number of pulses per half cycle was selected firstly because, the maximum energy of the target sinus waveform is concentrated in the middle of the waveform where the maximum amplitude is and on the other hand, in order to produce even frequency modulation ratios m_f to meet the bipolar PWM harmonic benefits of the harmonic outcome on the switched output of the inverter. Moreover, the implementation of the proposed method was extended to the overmodulation region, an aspect that was missing from the authors' published work in 1987. An alternative method was then developed and applied to multilevel inverters, using the initial theory of equal areas criteria. This alternative method was also extended to the overmodulation region.

Furthermore, in this thesis, multilevel inverter modulation methods were discussed and examined focusing on the cascade multilevel inverter topology. Emphasis was given to carrier modulation techniques since in low-voltage applications, when PWM of the inverters' output is required; these methods hold a dominant place in the market. These methods were used for simulation and comparative reasons as well. Reference modulation methods were also discussed as Space Vector PWM (SVPWM) is preferable in high voltage applications. In SVPWM, a set of trigonometric equations have to be solved in order to control the fundamental component, eliminate several low-order harmonics and reduce the switching losses. Large looking-up tables must be stored using a large amount of memory to hold the solutions of the trigonometric equations sets, making this method hard for on-line implementation, especially when a high value of levels is required.

Multi carrier modulation methods come up against all the prementioned problems in a more holistic manner and are more suitable for on-line implementation. In this thesis, an alternative method for conventional and

multilevel VSIs is proposed based on classic carrier techniques and their fundamental concepts without the need of an actual carrier, using simple sets of trigonometric equations derived by the simplicity that Equal Areas theory offers. Furthermore, operation of the proposed modulation methods in the overmodulation region was taken in consideration in the analysis.

The proposed EAPWM for conventional inverters is a direct technique based on algebraic equations which make it suitable for on-line implementation in a voltage source inverter. The analysis of the simulation and practical results showed that except of the ease of digital implementation, no particular benefits were derived in the linear modulation region while harmonic analysis showed similar outcomes to regular sampling techniques. The investigation in the overmodulation region produced three modified algorithms that are able to penetrate in the overmodulation region. Especially algorithm B, showed great interest since linear segments appeared in the overmodulation region. The modulation ratio was raised to control the fundamental at higher levels but keeping also the frequency ratio steady without the PWM pulse train converging to a square wave waveform.

The main outcome of this thesis is the proposed EAPWM in multilevel inverters. Equal areas theory was used for each level of an m-level inverter for better representation of the sinus target waveform. This approach resulted in non-integer values of frequency ratio where, according to literature, sub-harmonics may occur at low frequency ratios. The main advantage of this method is that most of the harmonic energy is concentrated at the “carrier” frequency which can be then eliminated between the phase-legs of a three-phase cascaded multilevel inverter. The simulation and experimental results showed less THD compared to the two main carrier-based PWM techniques PSCPWM and PDPWM for cascaded multilevel inverters for the single phase-leg voltage output.

Moreover, as in EAPWM for the conventional inverters, a modified algorithm was produced in order to investigate the multilevel inverters' behavior in the overmodulation region. Experimental and simulation results where produced and illustrated in this thesis. Due to time limitations and excessive work load that is required, this thesis could not include detailed analysis of the modified algorithm in three-phase cascaded H-bridge inverter. This analysis is subject to future work.

Further work will be carried out also in investigating the implementation of the proposed EAPWM in all other topologies of the multilevel inverter along with the microcontroller implementation, focusing on optimized programming of an online digital micro-processor based system.

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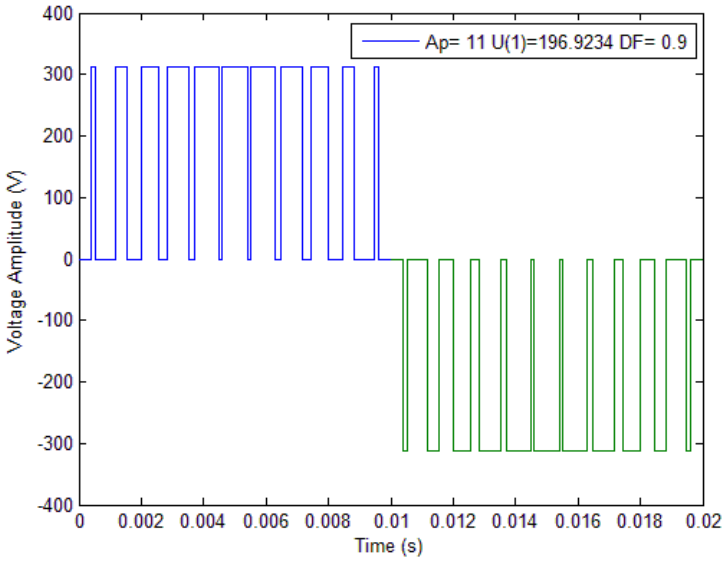
Appendices

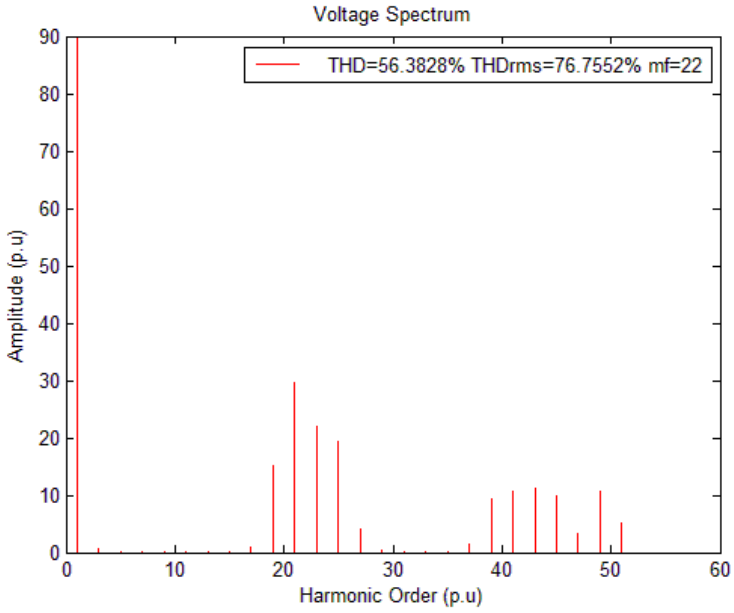
A. EAPWM Switching instants for Conventional and Multilevel inverters.

A.1 Switching instants implementing EAPWM in conventional inverters.

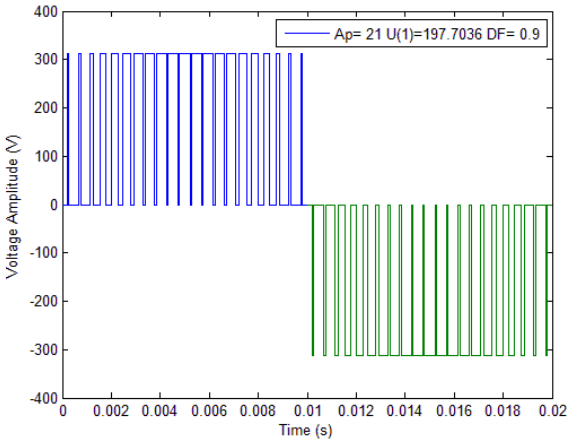
Modulation ratio ma=0.9. (Ap=11, Ap=21)

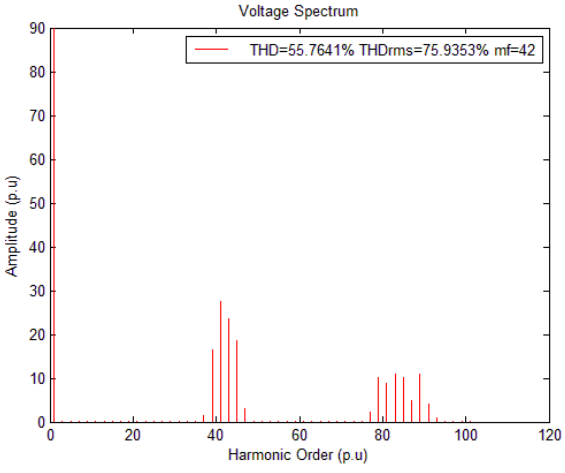
Ap=11	Time (ms)	
	Start	End
Pulse 1	0.397	0.513
Pulse 2	1.194	1.533
Pulse 3	2.006	2.540
Pulse 4	2.839	3.525
Pulse 5	3.700	4.482
Pulse 6	4.592	5.408
Pulse 7	5.518	6.300
Pulse 8	6.475	7.161
Pulse 9	7.460	7.994
Pulse 10	8.467	8.806
Pulse11	9.487	9.603





Ap=21	Time (ms)	
	Start	End
Pulse 1	0.222097	0.254094
Pulse 2	0.666647	0.761924
Pulse 3	1.112262	1.268691
Pulse 4	1.559624	1.77371
Pulse 5	2.009377	2.276338
Pulse 6	2.462112	2.775984
Pulse 7	2.918352	3.272124
Pulse 8	3.378544	3.764313
Pulse 9	3.843044	4.252194
Pulse 10	4.312115	4.735504
Pulse11	4.785914	5.214086
Pulse 12	5.264496	5.687885
Pulse 13	5.747806	6.156956
Pulse 14	6.235687	6.621456
Pulse 15	6.727876	7.081648
Pulse 16	7.224016	7.537888
Pulse 17	7.723662	7.990623
Pulse 18	8.22629	8.440376
Pulse 19	8.731309	8.887738
Pulse 20	9.238076	9.333353
Pulse 21	9.745906	9.777903

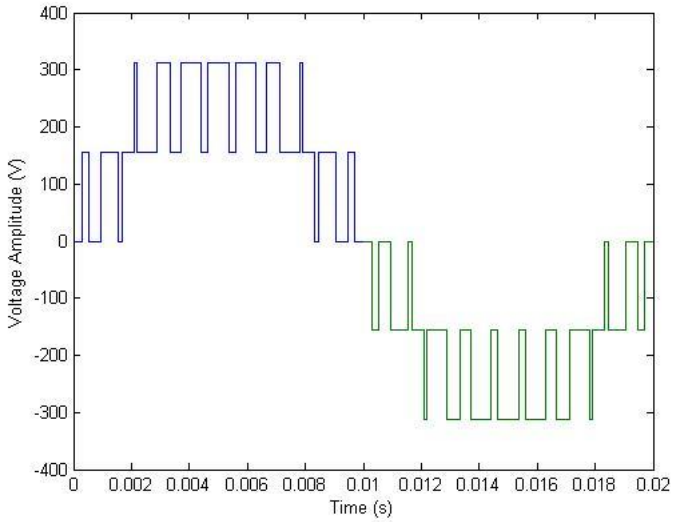


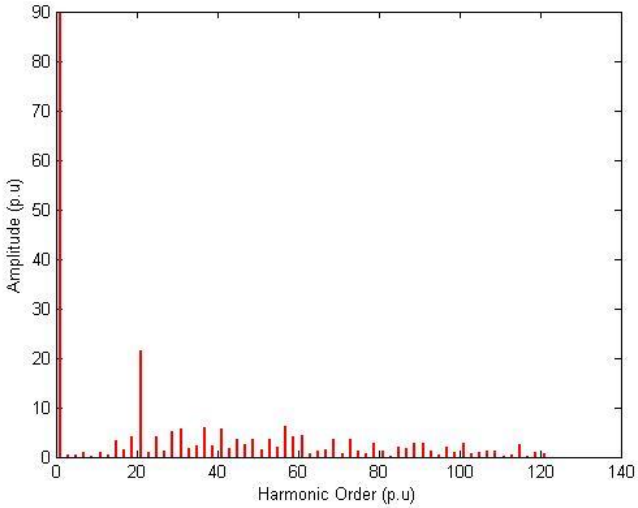


A.2 Switching instants implementing EAPWM in Multilevel inverters.

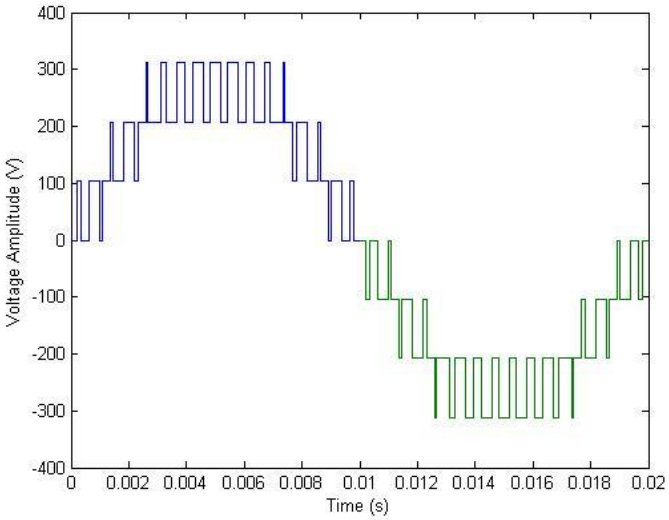
Modulation ratio m_a=0.9 – Ap_1=2 /Angles for 5-Level and 7-level Inverter

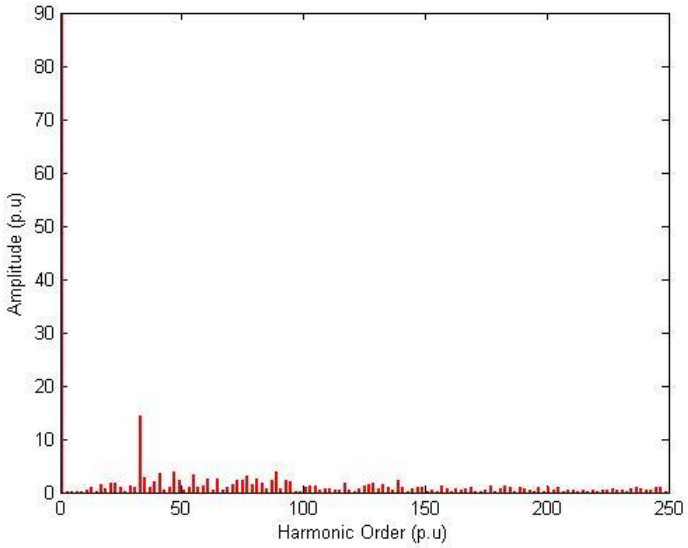
5-level		Time (ms)	
Level	Pulse	Start	End
1	Pulse 1	0.3191	0.5143
	Pulse2	0.9638	1.536
Level Shift		1.6667	
2	Pulse 1	2.087	2.199
	Pulse 2	2.866	3.325
	Pulse 3	3.708	4.387
	Pulse 4	4.622	5.378





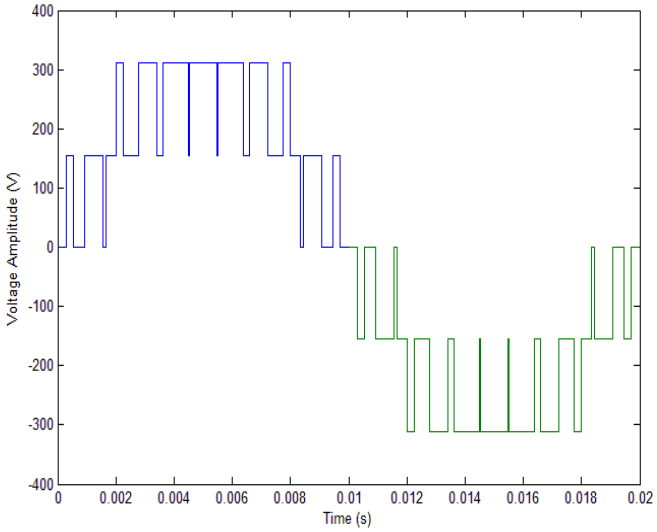
7-level		Time (ms)	
Level	**Pulse**	**Start**	**End**
1	**Pulse 1**	0.2085	0.3323
	Pulse 2	0.6274	0.9952
Level Shift		1.0817	
2	**Pulse 1**	1.348	1.436
	Pulse 2	1.829	2.197
Level Shift		2.322	
3	**Pulse 1**	2.613	2.627
	Pulse 2	3.131	3.299
	Pulse 3	3.658	3.962
	Pulse 4	4.212	4.598
	Pulse 5	4.793	5.207

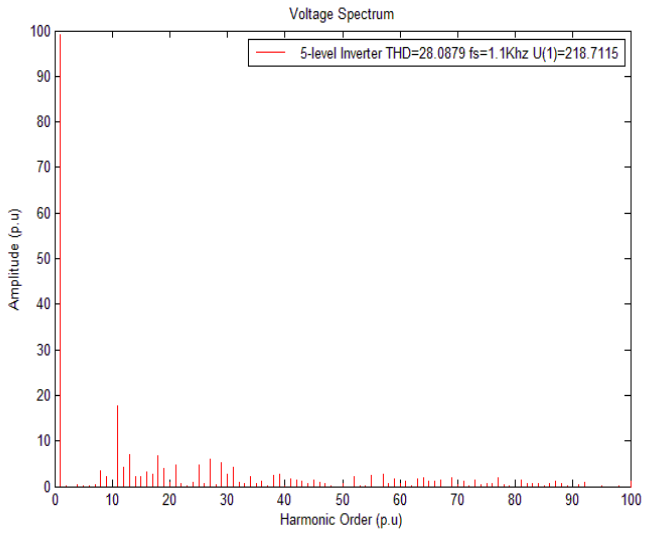




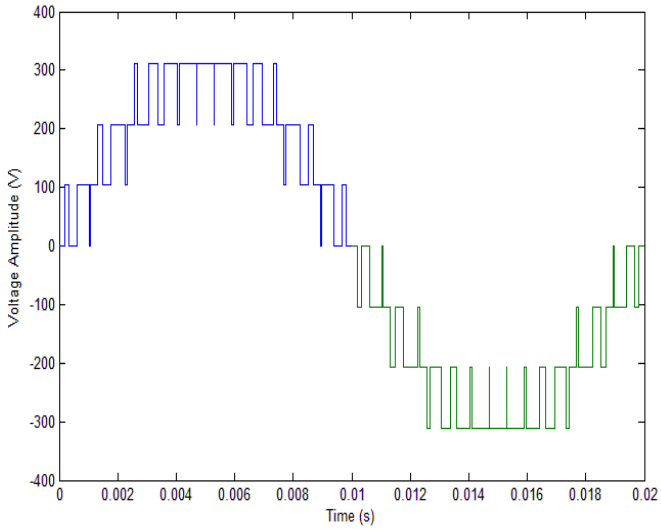
Modulation ratio m_a=1 – Ap_1=2 /Angles for 5-Level and 7-level Inverter

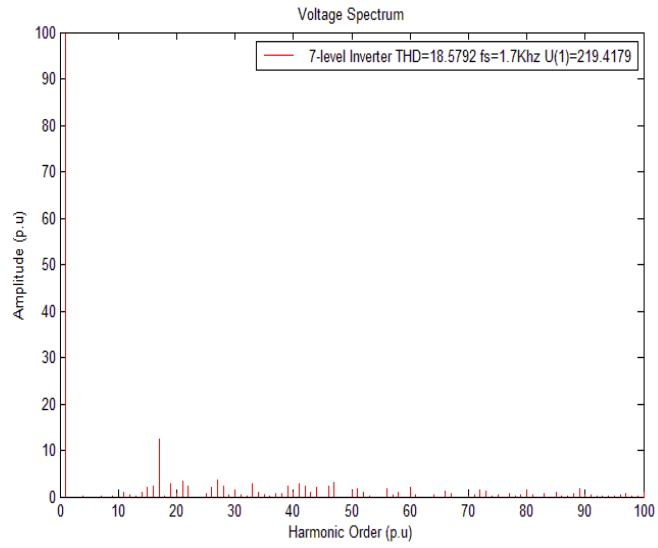
5-level		Time (ms)	
Level	**Pulse**	**Start**	**End**
1	**Pulse 1**	0.3082	0.5251
	Pulse 2	0.9320	1.5680
Level Shift		1.6660	
2	**Pulse 1**	2.0275	2.2583
	Pulse 2	2.7875	3.4030
	Pulse 3	3.6171	4.4781
	Pulse 4	4.5274	5.4726





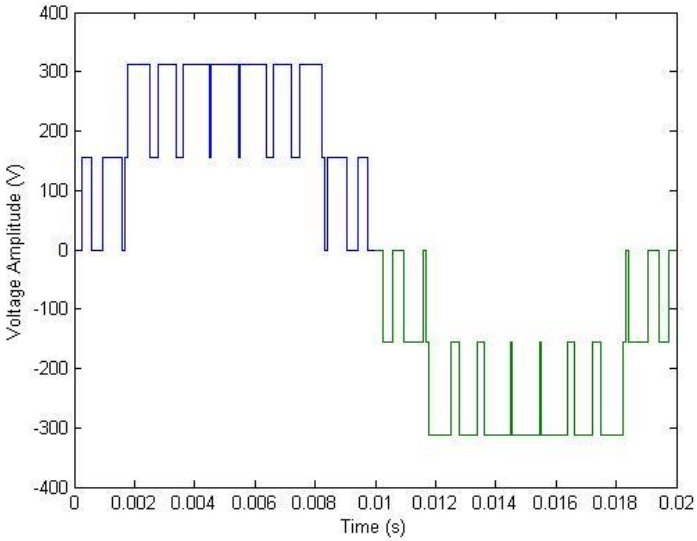
7-level		Time (ms)	
Level	**Pulse**	**Start**	**End**
1	**Pulse 1**	0.2017	3.3920
	Pulse 2	0.6070	1.0156
Level Shift		1.0817	
2	**Pulse 1**	0.0013	1.4753
	Pulse 2	1.7736	2.2515
Level Shift		2.3220	
3	**Pulse 1**	2.5617	2.6788
	Pulse 2	3.0555	3.3749
	Pulse 3	3.5755	4.0448
	Pulse 4	4.1244	4.6857
	Pulse 5	4.7038	5.2962

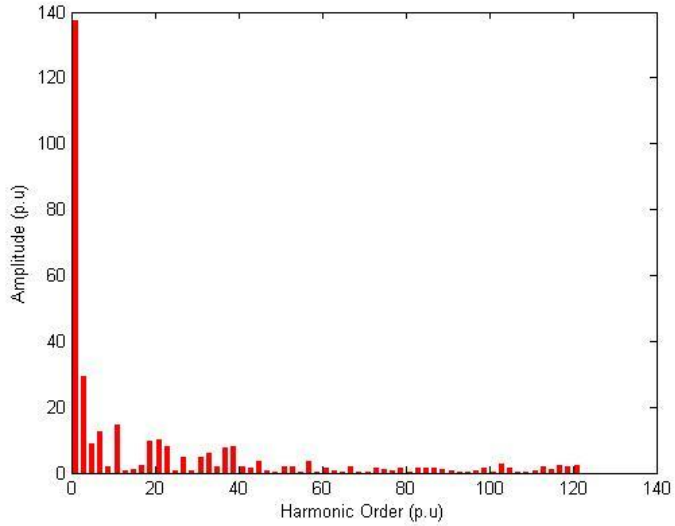




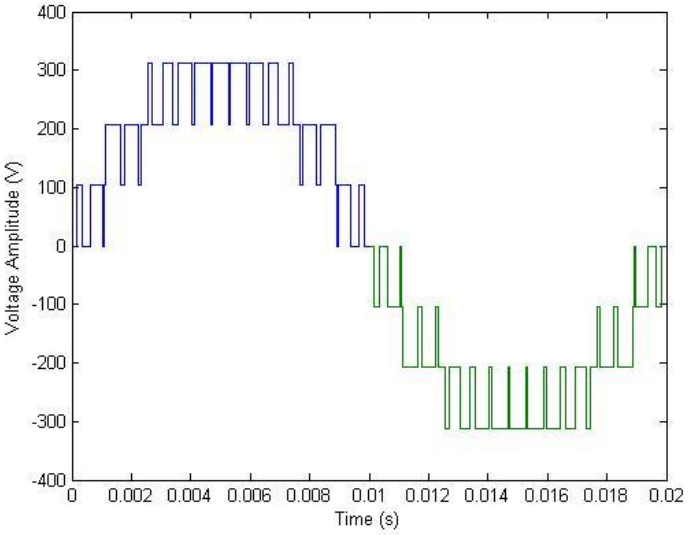
Modulation ratio m_a=1.4 – Ap_1=2 /Angles for 5-Level and 7-level Inverter

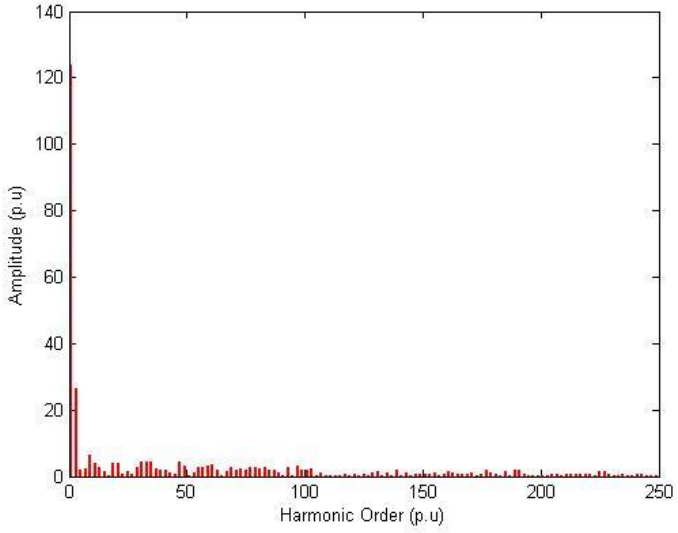
5-level		Time (ms)	
Level	**Pulse**	**Start**	**End**
1	**Pulse 1**	0.2648	0.5685
	Pulse 2	0.932	1.568
Level Shift		1.6660	
2	**Pulse 1**	1.791	2.495
	Pulse 2	2.787	3.403
	Pulse 3	3.617	4.478
	Pulse 4	4.527	5.473





7-level		Time (ms)	
Level	**Pulse**	**Start**	**End**
1	**Pulse 1**	0.1742	0.3667
	Pulse 2	0.6070	1.0160
Level Shift		1.0817	
2	**Pulse 1**	1.1510	1.6330
	Pulse 2	1.7740	2.2510
Level Shift		2.3220	
3	**Pulse 1**	2.5617	2.6788
	Pulse 2	3.0555	3.3749
	Pulse 3	3.5755	4.0448
	Pulse 4	4.1244	4.6857
	Pulse 5	4.7038	5.2962





B. EAPWM MATLAB codes for Conventional and Multilevel Inverters

B.1 EAPWM - MATLAB code for Conventional Inverters (Basic-algorithm)

```
clear;
hold off

E=1;
DF=0.9; %-setting the duty factor or modulation ratio
Ap=21;
f1=50;
T=1/f1;
d=(0.5)*T/Ap;
w=2*pi*f1;
Usmax=1*DF;
Up=1;
Umax=220*sqrt(2);
Udc=Umax;
fs=2*Ap/T;
mf=fs/(f1);
m=(Usmax/Up); %- modulation ratio

t(1:E)=(asin(((1:E)-1)/E))/w;
t=[t 0.01-fliplr(t)];
%-----------------Calculation of Switching Instants-----------------

for i=1:4*Ap

g(i)=(1+2*i+(-1)^(i+1))/4;
Tp(g(i))=(m/w)*(cos((g(i)-1)*w*d)-cos(g(i)*w*d));
Te(g(i))=((g(i)-1)*d+(0.5)*(d-Tp(g(i))));
Tk(i)=Te(g(i))+((1+(-1)^i)/2)*abs(Tp(g(i)));

 end

Tt=[];

for i=1:Ap
Tt=[Tt Te(i)+abs(Tp(i))];
end


b=[];
U=[];
%--------------------Harmonic Calculation for FFT------------------
for n=1:2:101

   for i=1:Ap

       e(i)=((-1)^i)*cos(n*w*Tk(i));
       z=sum(e);
```

```
   end

   b=[b abs((-4*Udc/(n*pi))*z)];
   U=b./sqrt(2);
   THD=100*sqrt(sum((b(2:end)/b(1)).^2));
   THDrms=100*sqrt((sqrt(2*Umax/pi)*sqrt(Udc)/U(1)).^2-1);
 end

%------------ Printing harmonics spectrum (Amplitude p.u) ----------
 figure(1)
    temp1=((b./Udc)*100);
    x=linspace(1,n,numel(b));
    stem(x,temp1,'red','marker','none','linewidth',1);
    temp2=['Ap=',num2str(Ap),' fs=',num2str(fs/1000),'kHz
THD=',num2str(THD),' U(1)=',num2str(U(1))];
    temp3=[' THD=',num2str(THD),'% THDrms=',num2str(THDrms),'%
mf=',num2str(mf)];
    disp(temp3)
    hold on

title 'Voltage Spectrum'
xlabel('Harmonic Order (p.u)')
ylabel('Amplitude (p.u)')
legend(temp3)
%------------------------ Voltage output Print ---------------------
x=[];
y=[];
ii=1;

    for i=1:2*E-1
    x=[x t(i)];
    if i<=E
        y=[y ((i-1)*Udc)];
    else
        y=[y ((2*E-i-1)*Udc)];
    end

    for u=1:Ap(i)
        x=[x Te(ii) Te(ii) Tt(ii) Tt(ii)];
        ii=ii+1;
        if i<=E
            y=[y ((i-1)*Udc) (i*Udc) (i*Udc) ((i-1)*Udc)];
        else
            y=[y ((2*E-i-1)*Udc) ((2*E-i)*Udc) ((2*E-i)*Udc) ((2*E-
i-1)*Udc)];
        end
    end
    x=[x t(i+1)];
    if i<=E
        y=[y ((i-1)*Udc)];
    else
        y=[y ((2*E-i-1)*Udc)];
    end
end
figure(2);
plot(x,y,x+0.01,-y);
```

```
temp2=['Ap= ',num2str(Ap),' U(1)=',num2str(U(1)),' ma=
',num2str(m)];
%title 'Voltage Output'
xlabel('Time (s)')
ylabel('Voltage Amplitude (V)')
legend(temp2)
disp(temp2)
```

B.2 Modified EAPWM

MATLAB code for (A-algorithm)

```
clear;
hold off

E=1;

Ap=11;
f1=50;
T=1/f1;
d=(0.5)*T/Ap;
w=2*pi*f1;
Usmax=1;
Up=(Usmax*2*Ap/pi)*sin(pi/(2*Ap)); %-Marginal value for m ratio
Umax=220*sqrt(2);
Udc=Umax;
fs=2*Ap/T;
mf=fs/(f1);
m=(Usmax/Up);
ma=Up/Usmax; %-setting the modulation ratio

t(1:E)=(asin(((1:E)-1)/E))/w;
t=[t 0.01-fliplr(t)];

%-----------------Calculation of Switching Instants-----------------

for i=1:4*Ap

   g(i)=(1+2*i+(-1)^(i+1))/4;
   Tp(g(i))=(m/w)*(cos((g(i)-1)*w*d)-cos(g(i)*w*d));
   Te(g(i))=((g(i)-1)*d+(0.5)*(d-Tp(g(i))));
   Tk(i)=Te(g(i))+((1+(-1)^i)/2)*abs(Tp(g(i)));

end

%----------------Harmonic Calculation for FFT----------------------
b=[];
U=[];

for n=1:2:120

   for i=1:Ap
```

```
        e(i)=((-1)^i)*cos(n*w*Tk(i));
        z=sum(e);
    end

    b=[b abs((-4*Udc/(n*pi))*z)];
    U=b./sqrt(2);
    THD=100*sqrt(sum((b(2:end)/b(1)).^2));
    THDrms=100*sqrt((sqrt(2*Umax/pi)*sqrt(Udc)/U(1)).^2-1);
    WTHD0=sqrt(sum((1/(n))*(b(2:end)/b(1)).^2));
end

%--------------Printing harmonics spectrum (Amplitude p.u)---------

temp1=((b./Udc)*100);
x=linspace(1,n,numel(b));
stem(x,temp1,'red','marker','none');
temp2=['Ap=',num2str(Ap),' fs=',num2str(fs/1000),'kHz
THD=',num2str(THD),' U(1)=',num2str(U(1)),' DF=',num2str(1/m)];
temp3=['THDn=',num2str(THD),'% THDrms=',num2str(THDrms),'%
mf=',num2str(mf)];
disp(temp3)
hold on

%title 'Voltage Spectrum'
xlabel('Harmonic Order (p.u)')
ylabel('Amplitude (p.u)')
legend(temp3)
%--------------------Printing Voltage Output----------------------
x=[];
y=[];
ii=1;
Tt=[];

    for i=1:Ap
     Tt=[Tt Te(i)+abs(Tp(i))];
    end

     for i=1:2*E-1
     x=[x t(i)];
     if i<=E
         y=[y ((i-1)*Udc)];
     else
         y=[y ((2*E-i-1)*Udc)];
     end

     for u=1:Ap(i)
         x=[x Te(ii) Te(ii) Tt(ii) Tt(ii)];
         ii=ii+1;
         if i<=E
             y=[y ((i-1)*Udc) (i*Udc) (i*Udc) ((i-1)*Udc)];
         else
             y=[y ((2*E-i-1)*Udc) ((2*E-i)*Udc) ((2*E-i)*Udc) ((2*E-
i-1)*Udc)];
         end
```

```
    end
    x=[x t(i+1)];
    if i<=E
        y=[y ((i-1)*Udc)];
    else
        y=[y ((2*E-i-1)*Udc)];
    end
end
figure
plot(x,y,x+0.01,-y);
temp2=['Ap= ',num2str(Ap),' ma= ',num2str(ma),'
U(1)=',num2str(U(1))];
%title 'Voltage Output'
xlabel('Time (s)')
ylabel('Voltage Amplitude (V)')
legend(temp2)
```

MATLAB code for (B-algorithm)

```
clear;
hold off

E=1;
DF=2.5; %-setting the initial duty factor or modulation ratio
Ap=21;
f1=50;
T=1/f1;
d=(0.5)*T/Ap;
w=2*pi*f1;
Usmax=1*DF;
Up=1;
Umax=220*sqrt(2);
Udc=Umax;
fs=2*Ap/T
mf=fs/(f1); %
m1=(Usmax/Up);

t(1:E)=(asin(((1:E)-1)/E))/w;
t=[t 0.01-fliplr(t)];

%-----------------Calculation of Switching Instants----------------
for i=1:4*Ap
m=m1;

g(i)=(1+2*i+(-1)^(i+1))/4;
Tp(g(i))=(m/w)*(cos((g(i)-1)*w*d)-cos(g(i)*w*d));
Te(g(i))=((g(i)-1)*d+(0.5)*(d-Tp(g(i))));
Tk(i)=Te(g(i))+((1+(-1)^i)/2)*abs(Tp(g(i)));

%time check if duration of pulses exceeds d and recalculation using
the marginal value of Up for the new modulation ratio m

if abs(Tp(g(i)))>d

    Up=(Usmax*2*Ap/pi)*sin(pi/(2*Ap));%
```

```
    m=(Usmax/Up);
    Tp(g(i))=(m/w)*(cos((g(i)-1)*w*d)-cos(g(i)*w*d));
    Te(g(i))=((g(i)-1)*d+(0.5)*(d-Tp(g(i))));
    Tk(i)=Te(g(i))+((1+(-1)^i)/2)*abs(Tp(g(i)));

   end

 end


 Tt=[];
      for i=1:Ap
      Tt=[Tt Te(i)+abs(Tp(i))];
      end


b=[];
U=[];
%----------------Harmonic Calculation for FFT--------------------
for n=1:2:101

   for i=1:Ap

       e(i)=((-1)^i)*cos(n*w*Tk(i));
       z=sum(e);
   end

   b=[b abs((-4*Udc/(n*pi))*z)];
   U=b./sqrt(2);
   THD=100*sqrt(sum((b(2:end)/b(1)).^2));
   THDrms=100*sqrt((sqrt(2*Umax/pi)*sqrt(Udc)/U(1)).^2-1);
end

%---------- Printing harmonics spectrum (Amplitude p.u)-------------
 figure(1)
    temp1=((b./Udc)*100);
    x=linspace(1,n,numel(b));
    stem(x,temp1,'red','marker','none','linewidth',1);
    temp2=['Ap=',num2str(Ap),' fs=',num2str(fs/1000),'kHz
THD=',num2str(THD),' U(1)=',num2str(U(1))];
    temp3=[' THD=',num2str(THD),'% THDrms=',num2str(THDrms),'%
mf=',num2str(mf)];
    disp(temp3)
    hold on

title 'Voltage Spectrum'
xlabel('Harmonic Order (p.u)')
ylabel('Amplitude (p.u)')
legend(temp3)
%------------------ Voltage output Print -------------------------

x=[];
y=[];
ii=1;
```

```
    for i=1:2*E-1
    x=[x t(i)];
    if i<=E
        y=[y ((i-1)*Udc)];
    else
        y=[y ((2*E-i-1)*Udc)];
    end

    for u=1:Ap(i)
        x=[x Te(ii) Te(ii) Tt(ii) Tt(ii)];
        ii=ii+1;
        if i<=E
            y=[y ((i-1)*Udc) (i*Udc) (i*Udc) ((i-1)*Udc)];
        else
            y=[y ((2*E-i-1)*Udc) ((2*E-i)*Udc) ((2*E-i)*Udc) ((2*E-
i-1)*Udc)];
        end
    end
    x=[x t(i+1)];
    if i<=E
        y=[y ((i-1)*Udc)];
    else
        y=[y ((2*E-i-1)*Udc)];
    end
end
figure(2);
plot(x,y,x+0.01,-y);
temp2=['Ap= ',num2str(Ap),' U(1)=',num2str(U(1)),' DF=
',num2str(m1)];
%title 'Voltage Output'
xlabel('Time (s)')
ylabel('Voltage Amplitude (V)')
legend(temp2)
disp(temp2)
```

MATLAB code for (C-algorithm)

```
clear;

E=1;
Ap=3;
DF=1.2;
f1=50;
T=1/f1;
d=(0.5)*T/Ap;
w=2*pi*f1;
Usin=DF*1;
Up=1;
Umax=220*sqrt(2);
Udc=Umax;
fs=2*Ap/T;
mf=fs/(f1);
m=(Usin/Up);
ma=Up/Usin;
```

```
t(1:E)=(asin(((1:E)-1)/E))/w;
t=[t 0.01-fliplr(t)];

%-----------------Calculation of Switching Instants-----------------
for i=1:4*Ap

   g(i)=(1+2*i+(-1)^(i+1))/4;
   Tp(g(i))=(m/w)*(cos((g(i)-1)*w*d)-cos(g(i)*w*d));
   Te(g(i))=((g(i)-1)*d+(0.5)*(d-Tp(g(i))));
   Tk(i)=Te(g(i))+((1+(-1)^i)/2)*abs(Tp(g(i)));

   tt(g(i))=Tp(g(i))+Te(g(i));
end

%Time check if the end of the previous pulse is higher than the
start of the next pulse, if so raise a flag k. if the flag is raised
once that means we reached the limit of modification and DF has to
be set at a lower value for this number of Ap (switching frequency).
k=0;
for i=1:Ap
    if tt(i)>Te(i+1)
        k=k+1;% flag
    end
end
k
Tt=[];
   for i=1:Ap
Tt=[Tt Te(i)+abs(Tp(i))];
end


b=[];
U=[];
%-------------------Harmonic Calculation for FFT------------------
for n=1:2:100

   for i=1:Ap

       e(i)=((-1)^i)*cos(n*w*Tk(i));
       z=sum(e);
   end

   b=[b abs((-4*Udc/(n*pi))*z)];
   U=b./sqrt(2);
   THD=100*sqrt(sum((b(2:end)/b(1)).^2));
   THDrms=100*sqrt((sqrt(2*Umax/pi)*sqrt(Udc)/U(1)).^2-1);%To THD me
tis rms
end
```

```
V=[];
V=[V 100*(U(1)/220)];
%------------- Printing harmonics spectrum (Amplitude p.u)----------

    temp1=((b./Udc)*100);
    x=linspace(1,n,numel(b));
    stem(x,temp1,'red','marker','none','linewidth',5);
    temp2=['Ap=',num2str(Ap),' fs=',num2str(fs/1000),'kHz
THD=',num2str(THD),' U(1)=',num2str(U(1)),' DF=',num2str(m)];
    temp3=[' THDn=',num2str(THD),'% THDrms=',num2str(THDrms),'%
mf=',num2str(mf)];
    disp(temp3)


title 'Voltage Spectrum'
xlabel('Harmonic Order (p.u)')
ylabel('Amplitude (p.u)')
legend(temp3)

%----------------- Voltage output Print -------------------------

x=[];
y=[];
ii=1;

    for i=1:2*E-1
    x=[x t(i)];
    if i<=E
        y=[y ((i-1)*Udc)];
    else
        y=[y ((2*E-i-1)*Udc)];
    end

    for u=1:Ap(i)
        x=[x Te(ii) Te(ii) Tt(ii) Tt(ii)];
        ii=ii+1;
        if i<=E
            y=[y ((i-1)*Udc) (i*Udc) (i*Udc) ((i-1)*Udc)];
        else
            y=[y ((2*E-i-1)*Udc) ((2*E-i)*Udc) ((2*E-i)*Udc) ((2*E-
i-1)*Udc)];
        end
    end
    x=[x t(i+1)];
    if i<=E
        y=[y ((i-1)*Udc)];
    else
        y=[y ((2*E-i-1)*Udc)];
    end
    end

figure
plot(x,y,x+0.01,-y);
temp2=['Ap= ',num2str(Ap),' U(1)=',num2str(U(1)),' DF=
',num2str(DF)];
```

```
%title 'Voltage Output'
xlabel('Time (s)')
ylabel('Voltage Amplitude (V)')
legend(temp2)
```

B.3 EAPWM - MATLAB code for Multilevel Inverters (Basic-algorithm)

```
clear;

E=3;% number of sources
Ap=2; % nymber of pulses in the first level
f1=50;
Usinrms=220; % rms value of target voltage

Usin=Usinrms*sqrt(2);
T=1/f1; % period in seconds
w=2*pi*f1;
Udc=Usin/E;

t=[]; % starting times for each level
D=[]; % duration of each level in seconds
t(1:E)=(asin(((1:E)-1)/E))/w;
t=[t 0.01-fliplr(t)];

D(1:2*E-1)=t(2:length(t))-t(1:length(t)-1);
Ape(1:2*E-1)=round(Ap*D(1:2*E-1)/D(1));



if (mod(Ape(E),2)==0)
Ape(E)=Ape(E)-1;% setting odd number for last level
end

d=D./Ape; % equal d intervals for each D level duration
fs=(2*sum(Ape)+(2*E-2))/(T); % switching freq (for each phase leg)
mf=fs/(f1);
ma=Usin/(E*Udc); % modulation ratio (here is one)
Nsw=2*sum(Ape)+(2*E-2); %number of switchings in one phase leg
J=[];
Je=[];
Jee=[];


for i=1:2*E-1
    for u=1:Ape(i)
        J=[J u];
        Jee=[Jee i];
        if i>E
            Je=[Je 2*E-i];
        else
            Je=[Je i];
        end
    end
end
```

```
%------------Calculation of switching instants----------------------

Tp=[];
Te=[];
Tk=[];
Tt=[];

Umaxaki=round(sum(Ape)/2);
for u=1:Umaxaki
    Tp=[Tp (E/w)*(cos(w*t(Je(u))+(J(u)-1)*w*d(Je(u)))-
cos(w*t(Je(u))+J(u)*w*d(Je(u))))-(Je(u)-1)*d(Je(u))];
    Te=[Te (t(Jee(u))+(J(u)-1)*d(Jee(u))+0.5*(d(Jee(u))-Tp(u)))];
    Tk=[Tk Te(u)+Tp(u)];
    Tt=[Tt Te(u) Tk(u)];
end


 if mod(Ape(E),2)==1

     for u=1:Umaxaki-1
         Tp=[Tp Tp(Umaxaki-u)];
         Te=[Te T/2-Tk(Umaxaki-u)];
         Tk=[Tk Te(end)+Tp(end)];
     end

 else

    for u=1:Umaxaki
        Tp=[Tp Tp(Umaxaki-u+1)];
        Te=[Te T/2-Tk(Umaxaki-u+1)];
        Tk=[Tk Te(end)+Tp(end)];
    end

 end

% -------------------Voltage output Print---------------------------
x=[];
y=[];
ii=1;


for i=1:2*E-1
    x=[x t(i)];
    if i<=E
        y=[y ((i-1)*Udc)];
    else
        y=[y ((2*E-i-1)*Udc)];
    end

    for u=1:Ape(i)
        x=[x Te(ii) Te(ii) Tk(ii) Tk(ii)];
        ii=ii+1;
        if i<=E
            y=[y ((i-1)*Udc) (i*Udc) (i*Udc) ((i-1)*Udc)];
```

```
        else
            y=[y ((2*E-i-1)*Udc) ((2*E-i)*Udc) ((2*E-i)*Udc) ((2*E-
i-1)*Udc)];
        end
    end
    x=[x t(i+1)];
    if i<=E
        y=[y ((i-1)*Udc)];
    else
        y=[y ((2*E-i-1)*Udc)];
    end
end

plot(x,y,x+0.01,-y);
temp2=[num2str(2*E+1),'-level Inverter'];
%title 'Voltage Output'
xlabel('Time (s)')
ylabel('Voltage Amplitude (V)')
%legend(temp2)
```

For the calculation of FFT the code is:

```
clear;

E=3;
Ap=2;
f1=50;
Usinrms=220;

Usin=Usinrms*sqrt(2);
T=1/f1;
w=2*pi*f1;
Udc=Usin/E;

t=[];
D=[];
t(1:E)=(asin(((1:E)-1)/E))/w;
t=[t 0.01-fliplr(t)];

D(1:2*E-1)=t(2:length(t))-t(1:length(t)-1);
Ape(1:2*E-1)=round(Ap*D(1:2*E-1)/D(1));

if (mod(Ape(E),2)==0)
Ape(E)=Ape(E)-1;
end

d=D./Ape; % the time interval for each level (h-bridge)
dm=sum(d)/(2*E-1); % the average time interval for all h-bridges
fs=1/(dm);% the average switching freq. for all h-bridges
mf=fs/(f1);
ma=Usin/(E*Udc);
Nsw=2*sum(Ape); % number of switchings in one phase leg


J=[];
```

```
Je=[];
Jee=[];


for i=1:2*E-1
    for u=1:Ape(i)
        J=[J u];
        Jee=[Jee i];
        if i>E
            Je=[Je 2*E-i];
        else
            Je=[Je i];
        end
    end
end


Tp=[];
Te=[];
Tk=[];
Tt=[];
A=[];
B=[];
C=[];
Z=[];
b=[];
OLO=[];
U=[];

%--------------Calculation of Switching Instants for FFT------------

for n=1:2:220 % number of harmonic components to be included
    Umaxaki=round(sum(Ape)/2);
for u=1:Umaxaki
    Tp=[Tp (E/w)*(cos(w*t(Je(u))+(J(u)-1)*w*d(Je(u)))-
cos(w*t(Je(u))+J(u)*w*d(Je(u))))-(Je(u)-1)*d(Je(u))];
    Te=[Te (t(Jee(u))+(J(u)-1)*d(Jee(u))+0.5*(d(Jee(u))-Tp(u)))];
    Tk=[Tk Te(u)+Tp(u)];
    Tt=[Tt Te(u) Tk(u)];

end

for i=1:E
    if i==1
        s=0;
    B(i)=s*cos(n*w*t(i));
    else
    s=1;
    B(i)=s*cos(n*w*t(i));
    end

end
C=sum(B);

for i=1:sum(Ape)
```

```
    A(i)=((-1)^i)*cos(n*w*Tt(i));
end
Z=sum(A);

OLO=[OLO (-4*Udc/n)*(-C+Z)];

end

% ----------------Harmonic Spectra Printout--------------
b=[b abs(OLO)/pi];
U=b./sqrt(2);


 if mod(Ape(E),2)==1

     for u=1:Umaxaki-1
         Tp=[Tp Tp(Umaxaki-u)];
         Te=[Te T/2-Tk(Umaxaki-u)];
         Tk=[Tk Te(end)+Tp(end)];
     end

 else

    for u=1:Umaxaki
        Tp=[Tp Tp(Umaxaki-u+1)];
        Te=[Te T/2-Tk(Umaxaki-u+1)];
        Tk=[Tk Te(end)+Tp(end)];
    end

 end


% -----------------Calculation of THD-----------------------------

THD=100*sqrt(sum((b(2:end)/b(1)).^2));
WTHD0=100*sqrt(sum((1/(n.^2))*(U(2:end)/U(1)).^2));

% -----------------Printing harmonic Spectra----------------------
temp1=((b./b(1))*100);
x=linspace(1,n,numel(b));
stem(x,temp1,'red','marker','none','linewidth',1);
temp2=[num2str(2*E+1),'-level Inverter',' THD=',num2str(THD),'
fs=',num2str(fs),'Khz',' U(1)=',num2str(U(1))];
%title 'Voltage Spectrum'
xlabel('Harmonic Order (p.u)')
ylabel('Amplitude (p.u)')
%legend(temp2)
disp(THD);
```

B.4 EAPWM - MATLAB code for Multilevel Inverters (Modified-algorithm)

```
clear;

E=3;% number of sources
Ap=2; % nymber of pulses in the first level
f1=50;
Usinrms=220; % rms value of target voltage

Usin=Usinrms*sqrt(2);
T=1/f1; % period in seconds
w=2*pi*f1;
Udc=Usin/E;

t=[]; % starting times for each level
D=[]; % duration of each level in seconds
t(1:E)=(asin(((1:E)-1)/E))/w;
t=[t 0.01-fliplr(t)];

D(1:2*E-1)=t(2:length(t))-t(1:length(t)-1);
Ape(1:2*E-1)=round(Ap*D(1:2*E-1)/D(1));



if (mod(Ape(E),2)==0)
Ape(E)=Ape(E)-1;% setting odd number for last level
end

d=D./Ape; % equal d intervals for each D level duration
fs=(2*sum(Ape)+(2*E-2))/(T); % switching freq (for each phase leg)
mf=fs/(f1);
ma=Usin/(E*Udc); % modulation ratio (here is one)
Nsw=2*sum(Ape)+(2*E-2); %number of switchings in one phase leg
J=[];
Je=[];
Jee=[];


for i=1:2*E-1
    for u=1:Ape(i)
        J=[J u];
        Jee=[Jee i];
        if i>E
            Je=[Je 2*E-i];
        else
            Je=[Je i];
        end
    end
end
%------------Calculation of switching instants---------------------

Tp=[];
Te=[];
Tk=[];
```

```
Tt=[];

Umaxaki=round(sum(Ape)/2);
for u=1:Umaxaki
    Tp=[Tp (E/w)*(cos(w*t(Je(u))+(J(u)-1)*w*d(Je(u)))-
cos(w*t(Je(u))+J(u)*w*d(Je(u))))-(Je(u)-1)*d(Je(u))];
    Te=[Te (t(Jee(u))+(J(u)-1)*d(Jee(u))+0.5*(d(Jee(u))-Tp(u)))];
    Tk=[Tk Te(u)+Tp(u)];
    Tt=[Tt Te(u) Tk(u)];

%--Modification/check if pulse duration Tp exceeds time interval d--
%--If Tp exceeds then recalculate Tp with modulation ratio m=1---

   if abs(Tp(u))>d(Je(u))
    k=k+1;
    m=1;
    Tp(u)=m*(E/w)*(cos(w*t(Je(u))+(J(u)-1)*w*d(Je(u)))-
cos(w*t(Je(u))+J(u)*w*d(Je(u))))-(Je(u)-1)*d(Je(u));
    Te(u)=(t(Jee(u))+(J(u)-1)*d(Jee(u))+0.5*(d(Jee(u))-Tp(u)));
    Tk(u)=Te(u)+Tp(u);
    Tt=[Tt Te(u) Tk(u)];
   end


end


 if mod(Ape(E),2)==1

     for u=1:Umaxaki-1
         Tp=[Tp Tp(Umaxaki-u)];
         Te=[Te T/2-Tk(Umaxaki-u)];
         Tk=[Tk Te(end)+Tp(end)];
     end

 else

    for u=1:Umaxaki
        Tp=[Tp Tp(Umaxaki-u+1)];
        Te=[Te T/2-Tk(Umaxaki-u+1)];
        Tk=[Tk Te(end)+Tp(end)];
    end

 end

% -------------------Voltage output Print---------------------------
x=[];
y=[];
ii=1;


for i=1:2*E-1
    x=[x t(i)];
    if i<=E
```

```
        y=[y ((i-1)*Udc)];
    else
        y=[y ((2*E-i-1)*Udc)];
    end

    for u=1:Ape(i)
        x=[x Te(ii) Te(ii) Tk(ii) Tk(ii)];
        ii=ii+1;
        if i<=E
            y=[y ((i-1)*Udc) (i*Udc) (i*Udc) ((i-1)*Udc)];
        else
            y=[y ((2*E-i-1)*Udc) ((2*E-i)*Udc) ((2*E-i)*Udc) ((2*E-
i-1)*Udc)];
        end
    end
    x=[x t(i+1)];
    if i<=E
        y=[y ((i-1)*Udc)];
    else
        y=[y ((2*E-i-1)*Udc)];
    end
end

plot(x,y,x+0.01,-y);
temp2=[num2str(2*E+1),'-level Inverter'];
%title 'Voltage Output'
xlabel('Time (s)')
ylabel('Voltage Amplitude (V)')
%legend(temp2)
```

For the calculation of FFT the code is:

```
clear;

E=3;
Ap=2;
f1=50;
Usinrms=220;

Usin=Usinrms*sqrt(2);
T=1/f1;
w=2*pi*f1;
Udc=Usin/E;

t=[];
D=[];
t(1:E)=(asin(((1:E)-1)/E))/w;
t=[t 0.01-fliplr(t)];

D(1:2*E-1)=t(2:length(t))-t(1:length(t)-1);
Ape(1:2*E-1)=round(Ap*D(1:2*E-1)/D(1));

if (mod(Ape(E),2)==0)
Ape(E)=Ape(E)-1;
end
```

```
d=D./Ape; % the time interval for each level (h-bridge)
dm=sum(d)/(2*E-1); % the average time interval for all h-bridges
fs=1/(dm);% the average switching freq. for all h-bridges
mf=fs/(f1);
ma=Usin/(E*Udc);
Nsw=2*sum(Ape); % number of switchings in one phase leg


J=[];
Je=[];
Jee=[];


for i=1:2*E-1
    for u=1:Ape(i)
        J=[J u];
        Jee=[Jee i];
        if i>E
            Je=[Je 2*E-i];
        else
            Je=[Je i];
        end
    end
end


Tp=[];
Te=[];
Tk=[];
Tt=[];
A=[];
B=[];
C=[];
Z=[];
b=[];
OLO=[];
U=[];

%--------------Calculation of Switching Instants for FFT------------

for n=1:2:220 % number of harmonic components to be included
    Umaxaki=round(sum(Ape)/2);
for u=1:Umaxaki
    Tp=[Tp (E/w)*(cos(w*t(Je(u))+(J(u)-1)*w*d(Je(u)))-
cos(w*t(Je(u))+J(u)*w*d(Je(u))))-(Je(u)-1)*d(Je(u))];
    Te=[Te (t(Jee(u))+(J(u)-1)*d(Jee(u))+0.5*(d(Jee(u))-Tp(u)))];
    Tk=[Tk Te(u)+Tp(u)];
    Tt=[Tt Te(u) Tk(u)];

%--Modification/check if pulse duration Tp exceeds time interval d--
%--If Tp exceeds then recalculate Tp with modulation ratio m=1---

   if abs(Tp(u))>d(Je(u))
    k=k+1;
    m=1;
```

```
    Tp(u)=m*(E/w)*(cos(w*t(Je(u))+(J(u)-1)*w*d(Je(u)))-
cos(w*t(Je(u))+J(u)*w*d(Je(u))))-(Je(u)-1)*d(Je(u));
    Te(u)=(t(Jee(u))+(J(u)-1)*d(Jee(u))+0.5*(d(Jee(u))-Tp(u)));
    Tk(u)=Te(u)+Tp(u);
    Tt=[Tt Te(u) Tk(u)];
   end

end

for i=1:E
    if i==1
        s=0;
    B(i)=s*cos(n*w*t(i));
    else
    s=1;
    B(i)=s*cos(n*w*t(i));
    end

end
C=sum(B);

for i=1:sum(Ape)
    A(i)=((-1)^i)*cos(n*w*Tt(i));
end
Z=sum(A);

OLO=[OLO (-4*Udc/n)*(-C+Z)];

end

% ----------------Harmonic Spectra Printout---------------
b=[b abs(OLO)/pi];
U=b./sqrt(2);


 if mod(Ape(E),2)==1

     for u=1:Umaxaki-1
         Tp=[Tp Tp(Umaxaki-u)];
         Te=[Te T/2-Tk(Umaxaki-u)];
         Tk=[Tk Te(end)+Tp(end)];
     end

 else

    for u=1:Umaxaki
        Tp=[Tp Tp(Umaxaki-u+1)];
        Te=[Te T/2-Tk(Umaxaki-u+1)];
        Tk=[Tk Te(end)+Tp(end)];
    end

 end
```

```
% -----------------Calculation of THD-----------------------------

THD=100*sqrt(sum((b(2:end)/b(1)).^2));
WTHD0=100*sqrt(sum((1/(n.^2))*(U(2:end)/U(1)).^2));

% -----------------Printing harmonic Spectra----------------------
temp1=((b./b(1))*100);
x=linspace(1,n,numel(b));
stem(x,temp1,'red','marker','none','linewidth',1);
temp2=[num2str(2*E+1),'-level Inverter',' THD=',num2str(THD),'
fs=',num2str(fs),'Khz',' U(1)=',num2str(U(1))];
%title 'Voltage Spectrum'
xlabel('Harmonic Order (p.u)')
ylabel('Amplitude (p.u)')
%legend(temp2)
disp(THD);
```